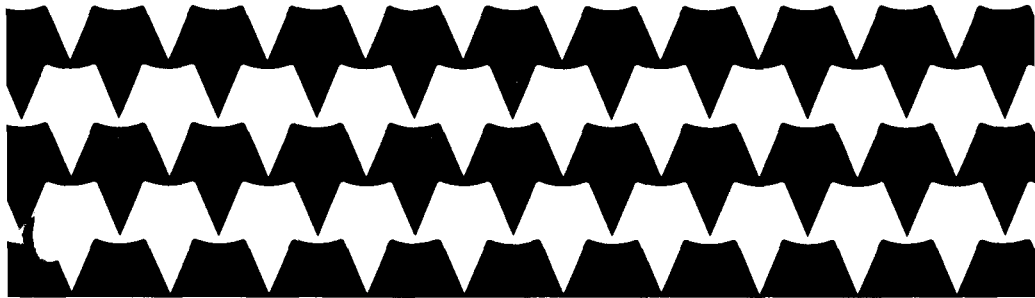


**Deluxe
Graphics Display Adapter
User's Manual**



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This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. Please note that all peripherals must be attached with shielded cables to prevent interference. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures.

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2. Relocate the computer with respect to the receiver.
3. Plug the computer into a different outlet so that the computer and receiver are on different branch circuits.
4. If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions.

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SECTION 1

INTRODUCTION

Features of the Tandy Deluxe Graphics Display Adapter (DGDA)

The DGDA is designed for use with the Tandy CM-1 Color Monitor. The combination provides you with a high quality 640×400 text and graphics display in conjunction with your existing software. Additional graphics modes are available with appropriate software drivers. The DGDA is compatible with drivers written for the Super Res 400 and Graphix Plus II display adapters from STB Systems, Inc.

The DGDA is switch selectable to function as a monochrome/color graphics adapter, or as a color graphics adapter only.

The DGDA can be plugged into any available expansion slot in a Tandy 1200 HD or compatible computer. The configuration switch on the DGDA is factory pre-set for most applications. See Section 4 for optional settings. Consult the owner's manual of your computer for information regarding installation and system switch settings. NOTE: Set the system switches for color.

The DGDA will provide you with the following display capabilities:

Text Display

- High resolution 80 character \times 25 line display with 8×16 character cell.
- Dual 256 character sets in ROM or EPROM.
- Underline, blink, reverse video, hidden and dual intensity character attributes.

Graphics Display

- Supports the following display modes:
320 × 200* × 4 color graphics
640 × 200* × 2 color graphics
- Supports the following display modes with appropriate software drivers:
320 × 200* × 16 color graphics
640 × 200* × 4 color graphics
640 × 400 × 2 color graphics

*Each of the 200 lines are drawn twice in order to fill the full 400 line screen.

The DGDA can be used with a VM-1 Monochrome Monitor. An optional cable is required. The cable is available from Radio Shack National Parts. Ask for Part No. AW-0027.

SECTION 2

PROGRAMMING

THE DGDA

This section of the manual covers material of interest to those who intend to write programs that use advanced features of the DGDA. A basic understanding of the operation of the Tandy 1200's standard video display adapters and ROM BIOS is assumed. Refer to the Tandy Technical Reference Manual for additional programming information.

If you intend to write programs that directly manipulate the DGDA's control registers, be careful of the values you set into the registers.

The DGDA board can be divided into 4 major sections: the mode switch, 6845 CRT controller chip (CRTC), control and status registers, and the 64Kb of video display memory.

DGDA Mode Switch

1	OFF	Board responds as BOTH Monochrome and Color Adapter cards.
	ON	Color/Graphics adapter only
2 & 3	OFF-OFF	High Resolution monitor (25 KHZ H.F.)
	OFF-ON	High Resolution monitor (25 KHZ H.F.)
	ON-OFF	High Resolution monitor (25 KHZ H.F.)
	ON-ON	High Resolution monitor (25 KHZ H.F.)
4	OFF	Vertical Sync Negative (Inverted)
	ON	Vertical Sync Positive
5	OFF	Horizontal Sync Negative (Inverted)
	ON	Horizontal Sync Positive
6,7,8		These 3 switches control which colors are sent to the mono display (6 = red, 7 = green, 8 = blue). ON sends the color, OFF blocks it.

Depending upon the settings of the DGDA's configuration switch (Switch 1), the DGDA can be configured as a color/graphics or as a monochrome and color/graphics adapter.

SWITCH 1	MODE
OFF	Both adapters. Software controls adapter mode.
ON	Color/graphics adapter only.

If the DGDA is set to respond as either adapter, any I/O accesses at the monochrome/printer adapter's 6845 CRT register addresses will switch the board into monochrome adapter mode and any accesses to the color/graphics adapter's CRTC registers will place the board into color/graphics adapter mode.

Throughout the rest of this manual, I/O control register addresses are given as two hex numbers in parentheses:

(MONO/COL)

The first number is the address that the monochrome adapter responds to and the second number is the color/graphics adapter address. Individual register bits are referred to as a 2 hex digit "bit-mask."

CRTC Controller Chip

The 6845 CRT Controller Chip (CRTC) is the main control circuit of the DGDA board. It produces all the timing, control, synchronization, and display addresses for the board.

CRTC Address Register (3B4/3D4)

The CRTC contains 16 control registers. These registers control the timing position and width of the monitor sync pulses, display and text cursor. The registers are accessed by first outputting the number of the register to be accessed (0-15) into the CRTC Address Register. This register is write-only. Its value cannot be read back by software.

CRTC Data Register (3B5/3D5)

Once the CRTC Address Register has been set to the number of the CRTC register to be accessed (0-15), the register's data value is written or read via this I/O address. The registers are described briefly in the following table. For a full description, refer to a 6845 CRTC data sheet.

6845 CRTC Register Definitions

REG	READ/WRITE	FUNCTION
0	Write	HTOTAL — Total number of character cells per scan line minus 1. The MODE register clock rate control bit (01) sets the timing of each character cell on the scan line. This register thus determines the frequency of the horizontal sync pulses and scan lines.
1	Write	HDISP — Total number of characters displayed per character row. Display memory WORDS from 0 to HDISP-1 are displayed. Cells from HDISP to HTOTAL-1 are used for sync pulses and screen border area. HDISP is added to the video RAM display address after each character row has been displayed. In graphics applications each SCAN LINE within the character row temporarily increments the display address 8192 bytes.
2	Write	HSPOS — Contains the character cell location of the start of the horizontal sync pulse. As this register is increased in value the picture is shifted left on the screen.
3	Write	WIDTH — The lower four bits of this register determine the width of the horizontal sync pluse. Its value may range from 0-15 character cells. The character cell time is determined by bit 01 in the MODE register. The upper four bits should be set to 0's.

REG	READ/WRITE	FUNCTION
4	Write	VTOTAL — This register is set with the total number of character ROWS (0-127) per frame of video. VTOTAL together with the MAXSCAN register (R9) determine the coarse frequency of the vertical sync pulses.
5	Write	VADJ — This register sets the number of extra scan lines to add to each video frame (0-31). It is used to “fine-tune” the frequency of the vertical sync pulse.
6	Write	VDISP — This register determines the number of character ROWS (0-127) that are shown on the screen.
7	Write	VSP — This register contains the character row number of the start of the vertical sync pulse (0-127). Increasing the value of this register will move the picture UP on the screen.
8	Write	INTERLACE — For normal, non-interlaced use set this register to the value “2”.
9	Write	MAXSCAN — This register is set with how many scan lines tall each character row is minus 1.
10	Write	CURSOR START — The lower 5 bits of this register should be loaded with the scan line number of the character cell where the text cursor should start (0-31). If the upper three bits of this register are set to “001XXXX” then the cursor is turned off.

REG	READ/WRITE	FUNCTION
11	Write	CURSOR END— This register is loaded with the number of the last scan line of the text cursor (0-31). By changing the values in registers R10 and R11, the shape of the text cursor can be changed from an underline to a block, dash, etc.
12,13	Write	START ADDRESS— These two registers contain the number of WORDS in the display RAM buffer to skip before starting the display. R13 is the lower 8 bits of the WORD (2 byte) count. R12 is the upper 6 bits.
14,15	Read/Write	CURSOR ADDRESS — These two registers contain the WORD offset of the character/attribute word in display RAM where the flashing text cursor should appear. R15 is the lower 8 bits of the WORD count. R14 is the upper 6 bits.

Mode Control Register (3B8/3D8)

The MODE register is a 6 bit register that controls the basic operating mode of the DGDA board. This register is a write only register. The value stored in the register cannot be read back.

BIT	FUNCTION
01	VIDEO CLOCK RATE CONTROL — When set to a “0”, the video data is shifted out as a 11.144 Mhz dot (pixel) rate. The character CRTC character clock rate is .720 microseconds/char. This is used for 40 column text displays and the standard IBM graphics modes. When set to a “1”, the dot clock rate is 22.285 Mhz and the character rate is 0.360 microseconds/char. This is used for 80 column text displays and the high resolution 16 color and 4 color graphics modes.

BIT	FUNCTION
02	<p>GRAPHICS ENABLE — When set to a “0”, the board is in Text mode and the video display is produced via the CHARACTER GENERATOR read-only-memory. When set to a “1”, the video display is produced by the bit-mapped GRAPHICS generator circuitry. If software operates the board at the Monochrome Display addresses, this bit is ignored and the display is forced into TEXT mode.</p>
04	<p>This bit is only used in the 4 color graphics modes. It should normally be set to a “0”. If set to a “1” the CYAN/MAGENTA/WHITE palette is changed to CYAN/RED/WHITE.</p>
08	<p>VIDEO ENABLE — When set to a “0”, the video display are turned off. When set to a “1”, the video display is sent to the active video monitor. The setting of this bit is forced to a “1” whenever software configures the board for 80 column text displays in COLOR/GRAPHICS adapter modes.</p>
10	<p>640 DOT GRAPHICS ENABLE — When set to “0”, the graphics display circuitry is set to display a picture with 320 dots/line. Setting this bit to a “1” produces a 640 dot display. This bit is used only when the GRAPHICS bit (02) is set to a “1”.</p>
20	<p>BLINK ENABLE — When set to a “0”, text characters cannot blink, but can be shown with up to 16 different background colors. When set to a “1” the character background color intensity for all characters is determined by bit 10 of the COLOR register described below and background intensity BIT (80) of the display RAM character attribute byte will control the blinking of the character (if set, the character will blink). This bit is used only when the GRAPHICS bit (04) is set to a “0”.</p>

Color Control Register (3B9/3D9)

This register is a 6 bit write-only register that controls the color processing circuitry.

BIT	FUNCTION
01	Blue — In TEXT modes this bit has no function. In 4-color GRAPHICS modes, this bit controls the color blue of the BACKGROUND color (00) pixels.
02	Green — In TEXT modes this bit has no function. In 4-color GRAPHICS modes, this bit controls the color green of the BACKGROUND color (00) pixels.
04	Red — In TEXT modes this bit has no function. In 4-color GRAPHICS modes, this bit controls the color red of the BACKGROUND color (00) pixels.
08	INTENSITY — In TEXT modes this bit has no function. In 4-color GRAPHICS modes, this bit controls the intensity of the BACKGROUND color (00) pixels.
10	In TEXT modes this bit controls the character background intensity of all the characters on the screen if the BLINK bit (20) is set in the MODE register. In 4-color GRAPHICS modes, this bit controls the INTENSITY of the foreground color set. A “1” selects high intensity colors, a “0” selects normal.
20	In 4-color GRAPHICS modes this bit selects which of two color “palettes” is displayed. When set to a “0” the available colors are BACKGROUND/GREEN/RED/BROWN. A “1” selects BACKGROUND/CYAN/MAGENTA/WHITE. This is ignored in all other modes.

Status Register (3BA/3DA)

This is a 4 bit read-only register that software can check to determine various information about the display.

When read at the MONOCHROME Adapter address (3BA) the following information is returned:

BIT	FUNCTION
01	HSYNC— The current state of the display monitor horizontal sync pulse can be monitored here. A “1” indicates the pulse is active.
02	Always “0”
04	Always “0”
08	VIDEO DOTS— When read as a “1” the display is showing a lighted pixel. When read as a “0” the display is showing an unlighted pixel. This information helps diagnostic programs test the operation of the board.

When this register is read at the COLOR/GRAPHICS address (3DA) the following information is returned:

BIT	FUNCTION
01	DISPLAY INACTIVE— Set to a “1” when the display beam is in the SYNC or BORDER areas of the display. This bit is a “0” during the active portion of the display. <i>Note that the DGDA display memory can be accessed at any time without causing “snow” to appear in the picture.</i> Programs that wait for this bit to be set before accessing the display memory will run much faster if they are modified to NOT wait on the bit.
02	Always “0”
04	Always “1”
08	VSYNC— While this bit is a “1”, the display beam is within the vertical sync area. This information is useful for special animation effects, etc.

Video Display Memory

The DGDA has 64 kilobytes (Kb) of dual-ported video display memory shared between the expansion bus and the 6845 CRTC video display controller. The bus may access the video memory at any time without causing any "snow" to appear in the picture. The board may generate 0-2 wait states depending upon the timing of the memory request. The video display memory supports DMA (direct memory access controller) requests.

Software using the monochrome display adapter accesses the 32Kb of video display memory at segment address B000. Color/graphics adapter software accesses the 32Kb of memory at segment address B800.

The standard Color/Graphics Adapter memory appears to the system as a single 16Kb block of memory duplicated at segments B800 and BC00. The DGDA has independent 16Kb memory blocks at these segments. Software that expects the same data to appear in both 16Kb segments may need to be modified to work with the DGDA's extra memory.

The CRTC sequentially accesses the video display memory, fetching and displaying a 16-bit word of data every 360 or 720ns, depending upon how the CLOCK RATE bit (01) of the MODE register is set. The MODE register also determines how this word of data will appear on the screen.

The DGDA has two modes of displaying the video memory word, **Text and Graphics**. Bit 02 of the MODE register determines the mode.

Text Mode

If bit 02 of the MODE register is low, the board is in TEXT mode and the word of video data is sent to the CHARACTER GENERATOR logic.

The even byte of each word contains the number of the character to display. The standard character set contains 256 unique characters numbered from 0-255.

The odd byte (attribute byte) determines the color of the character dots and their surrounding background. The lower four bits contain the color code of the character's dots. The upper four bits determine the color of the dots in the character matrix that surround the character outline.

Even Byte — Character Code

Bits 7 6 5 4 3 2 1 0
character code 00 - FF

Odd Byte — Character Color

Bits 7 6 5 4 3 2 1 0
I R G B I R G B
BACKGROUND FOREGROUND

Sixteen unique colors are available for the foreground or background. These colors are formed by combining the basic colors Red, Green, and Blue with an optional Intensity bit.

COLOR CODE	SCREEN COLOR
0	Black
1	Blue
2	Green
3	Cyan (pale blue)
4	Red
5	Magenta (purple)
6	Yellow
7	White
8	Dark Grey
9	Bright Blue
10	Bright Green
11	Bright Cyan
12	Bright Red

COLOR CODE	SCREEN COLOR
13	Bright Magenta
14	Bright Yellow
15	Bright White

- * Some color monitors ignore the Intensity signal and colors 8-15 appear the same as 0-7.
- * By properly combining foreground and background colors, special effects such as reverse video, hi-lighting, and hidden text can be obtained.

Blinking Text

The background intensity bit (80 or ODD bytes) in the video display word is shared with the character BLINK logic. If bit 20 of the MODE register is "0", then all 16 colors are available for character backgrounds. If the bit is set to a "1", the background intensity bit (80) is changed to be a "BLINK CHARACTER" bit and the background intensity for ALL characters is supplied from bit 10 of the COLOR REGISTER.

Character Generator ROM

The patterns of dots that make up the characters that the DGDA displays in text modes are stored in a computer chip called a read-only-memory or ROM. The character generator ROM actually contains the patterns for the TWO sets of 256 characters. The first 256 characters (4096 bytes) contains the color/graphics adapter characters. The next 256 characters (4096 bytes) are the monochrome display adapter characters. The board automatically switches between the character sets based upon how the 6845 CRT controller chip MAX SCAN LINE register (R9) is programmed. Values less than 10 will select the color graphics set. Values of 10 or above will select the monochrome display set.

The color graphics adapter set shows characters as an 8×8 matrix of closely spaced dots. The monochrome character set is formed in an 8×14 matrix. Each byte in the EPROM contains one scan line of 8 dots for a character. Each character is stored in the EPROM as a 16 byte block; the patterns for each character are aligned in the first 8 or 14 bytes of the 16 byte blocks. Since there is no spacing between adjacent character cells on the screen, continuous line and block graphics characters are easily made.

The contents of the standard ROM supplied with the boards cannot be changed. For applications that require a different or customized character set the standard ROM chip (the 28 pin device on the DGDA labeled CGEN) may be replaced by a user programmable part called an EPROM (Erasable Programmable Read Only Memory). The EPROM used on the DGDA board is an industry standard 2764 type device with an access time of 450ns (nanoseconds) or faster. This type of device contains 8K bytes of data. The contents of an EPROM may be erased by exposing it to ultraviolet light. A device called an EPROM Programmer may be used to write new data into an erased EPROM.

Graphic Modes

If bit 02 of the MODE register is set to a "1" *and* the DGDA is operating as a Color/Graphics adapter, then the video display words are shown on the screen as a series of independently colored dots. Depending upon the settings of the 640 GRAPHICS (10) and CLOCK RATE (01) bits in the MODE register, the DGDA will show these 16 bits in one of four basic ways:

NOTE: If a value greater than or equal to 16 is loaded into the Max Scan Register (09) of the 6845, the DGDA will be placed into a 400 line graphics mode.

MODE REGISTER		Graphics Resolution
Bit 10	01	
1	0	16 pixels of 2 colors ($640 \times 200/352 \times 2$ colors)
1	1	8 pixels of 4 colors ($640 \times 200 \times 4$ colors)
0	0	8 pixels of 4 colors ($320 \times 200 \times 4$ colors)
0	1	4 pixels of 16 colors ($320 \times 200 \times 16$ colors)
1	0	16 pixels of 2 colors ($640 \times 400 \times 2$)
1	1	8 pixels of 4 colors ($640 \times 400 \times 4$ colors)*
0	1	4 pixels of 16 colors ($320 \times 400 \times 16$ colors)*

*Modes not available on the standard Color/Graphics Adapter. These modes use all 64Kb of the display RAM. The standard modes use 16Kb.

Two Color Mode

In this mode, each bit in the word produces one dot on the screen. The dot is always black if the bit is a "0". Bits set to a "1" produce dots of the color indicated by the BACKGROUND bits (08, 04, 02, & 01) of the COLOR register.

EVEN BYTE

Bit: 7 6 5 4 3 2 1 0
C0 C0 C0 C0 C0 C0 C0 C0

ODD BYTE

Bit: 7 6 5 4 3 2 1 0
C0 C0 C0 C0 C0 C0 C0 C0

Sixteen Color Mode

This mode divides each 16 bit word into 4 "nibbles" of 4 bits each. The four bits of each nibble represent the color number (0-15) as shown in the color table in the text section above.

EVEN BYTE

Bit: 7 6 5 4 3 2 1 0
C3 C2 C1 C0 C3 C2 C1 C0

ODD BYTE

Bit: 7 6 5 4 3 2 1 0
C3 C2 C1 C0 C3 C2 C1 C0

Four Color Mode

This mode treats each word as 8 pixels of 2 adjacent bits (C1 and C0). Each pair of bits produce a dot that can be one of four colors. Bit 20 in the COLOR register and bit 04 in the MODE register select one of three available “pallettes” of four colors. Setting bit 10 in the COLOR register will intensify all the foreground colors on the screen.

EVEN BYTE

Bit: 7 6 5 4 3 2 1 0
 C1 C0 C1 C0 C1 C0 C1 C0

ODD BYTE

Bit: 7 6 5 4 3 2 1 0
 C1 C0 C1 C0 C1 C0 C1 C0

REGISTER BITS				COLOR
Color 20	Mode 04	Pixel C1 C0		
0	0	0	0	Color Reg BACKGROUND bits
0	or	0	1	Green
		1	0	Red
		1	1	Brown
1	0	0	0	Color Reg BACKGROUND bits
1	1	0	1	Cyan
		1	0	Magenta
		1	1	White
		0	0	Color Reg BACKGROUND bits
		0	1	Cyan
		1	0	Red
1	1	1	1	White

In 200 line graphics modes, the CRTC chip should be programmed to display either 100 character rows of 2 scan lines per row (for standard resolutions of $320 \times 200 \times 4$ color and $640 \times 200 \times 2$ color), or 50 character rows of 4 scan lines per row (for the extra modes of $320 \times 200 \times 16$ color and $640 \times 200 \times 4$ color).

In 400 line graphics modes, the CRTC chip should be programmed to display either 100 character rows of 4 scan lines per row (for resolutions of $640 \times 400 \times 2$), or 50 character rows of 8 scan lines per row (for resolutions of $640 \times 400 \times 4$ and $320 \times 400 \times 16$).

The CRTC chip produces a series of sequential addresses as it fetches display words for each scan line of the picture from video memory. Note however that each scan line within every character row is offset in the video memory 8192 bytes (2000 hex) from the preceding scan line of the character row.

CHARACTER ROW SCAN LINE NO.	OFFSET FROM START OF BUFFER
00	&H0000
01	&H2000
02*	&H4000
03*	&H6000

* These higher resolution modes require all 64Kb of video display memory.

DGDA Typical Register Values

Resolution: Adapter Mode: Text/Graphics:	80 × 25 Monochrome Text	80 × 50 Monochrome Text	640 × 400 × 2 Monochrome Graphics	640 × 400 × 4 Color Graphics	320 × 400 × 16 Color Graphics	40 × 25 Color Text	80 × 25 Color Text	640 × 200 × 2 Color Graphics	320 × 200 × 4 Color Graphics	640 × 200 × 4 Color Graphics	320 × 200 × 16 Color Graphics
R0-HOR TOTAL	61	61	31	71	71	38	71	38	38	71	71
R1-HOR DISP	50	50	28	50	50	28	50	28	28	50	50
R2-HSYNC POSN	52	52	29	59	59	2D	5A	2D	2D	59	59
R3-HS WIDTH	0F	0F	08	0C	0C	0A	0A	0A	0A	0C	0C
R4-VERT TOTAL	19	2E	6C	3F	3F	1F	1F	7F	7F	3F	3F
R5-VERT ADJ	06	06	06	06	06	06	06	06	06	06	06
R6-VERT DISP	19	32	64	32	32	19	19	64	64	32	32
R7-VSYNC POSN	19	2C	68	38	38	1C	1C	70	70	38	38
R8-INTERLACE	02	02	02	02	02	02	02	02	02	02	02
R9-MAX SCAN	0D	17	13	17	17	07	07	01	01	03	03
R10-CUR START	0B	05	06	0B	0B	06	06	06	06	06	06
R11-CURSOR END	0C	07	07	0C	0C	07	07	07	07	07	07
R12-START (H)	00	00	00	00	00	00	00	00	00	00	00
R13-START (L)	00	00	00	00	00	00	00	00	00	00	00
R14-CURSOR (H)	00	00	00	00	00	00	00	00	00	00	00
R15-CURSOR (L)	00	00	00	00	00	00	00	00	00	00	00
MODE REG VALUE	29	29	1E	1B	2B	2C	2D	1E	2A	1B	2B
MODE REG ADDR	3B8	3B8	3D8	3D8	3D8	3D8	3D8	3D8	3D8	3D8	3D8
COLOR REG VALUE	30	30	2F	30	30	30	30	3F	30	30	30
COLOR REG ADDR	3B9	3B9	3D9	3D9	3D9	3D9	3D9	3D9	3D9	3D9	3D9
CRTC CHIP ADDR	3B4	3B4	3D4	3D4	3D4	3D4	3D4	3D4	3D4	3D4	3D4
VIDEO MEMORY SEGMENT	B000	B000	B000	B000*	B000*	B800	B800	B800	B800	B800	B800
VIDEO MEMORY LENGTH	0FFF	1FFF	7FFF	FFFF	FFFF	3FFF	3FFF	3FFF	7FFF	7FFF	7FFF

Note: All values given in hex.

*These graphics modes require 64K of memory. Therefore, the starting address is at B000.

SECTION 3

SPECIFICATIONS

The display connector on the DGDA is brought out via a 9 pin cable connector located on the DGDA mounting bracket. This connector is used to connect a cable from the DGDA to a Tandy CM-1 Color Monitor. The pinouts of this connector are defined below:

9 PIN "D"	DESCRIPTION
1	Ground
2	Ground
3	Red
4	Green
5	Blue
6	Intensity
7	Composite
8	Horizontal Sync
9	Vertical Sync

POWER CONSUMPTION: 7.5 Watts

OUTPUTS: Video Signals = TTL level, positive polarity
Sync Signals = TTL level, positive polarity
(default)*

*Sync signal polarity is switch selectable.

DIMENSIONS: 13.2" × 4.2"

SECTION 4

DGDA SWITCH/JUMPER SETTINGS

1. Locate the switch box on the DGDA. (See Figure 1.)

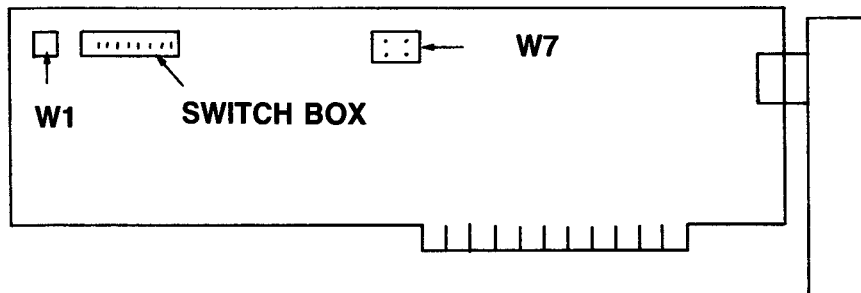


Figure 1 — DGDA Diagram

2. Figure 2 gives you the factory pre-set switch settings. This allows the DGDA to work with a Tandy CM-1 Color Monitor. Check to be sure the switches are set correctly.

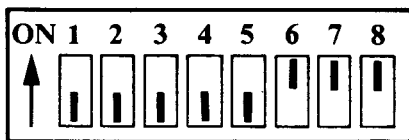


Figure 2 — DGDA Switch Settings

3. Refer to the following switch summary for optional switch settings.
4. Jumper W1 is not connected. Jumper W7 has a shorting plug across the lower two pins.

Switch Summary

1	OFF	Board responds as BOTH Monochrome and Color Adapter boards.
	ON	Color/Graphics adapter only.
2 & 3	OFF-OFF	High Resolution monitor (25 KHZ H Sync)
	OFF-ON	High Resolution monitor (25 KHZ H Sync)
	ON-OFF	High Resolution monitor (25 KHZ H Sync)
	ON-ON	High Resolution monitor (25 KHZ H Sync)
4	OFF	Vertical Sync Negative (Inverted)
	ON	Vertical Sync Positive
5	OFF	Horizontal Sync Negative (Inverted)
	ON	Horizontal Sync Positive
6,7,8		These 2 switches determine which colors are sent to the mono display (6 = red, 7 = green, 8 = blue). ON sends the color, OFF blocks it.

NOTES ON SETTING SWITCHES

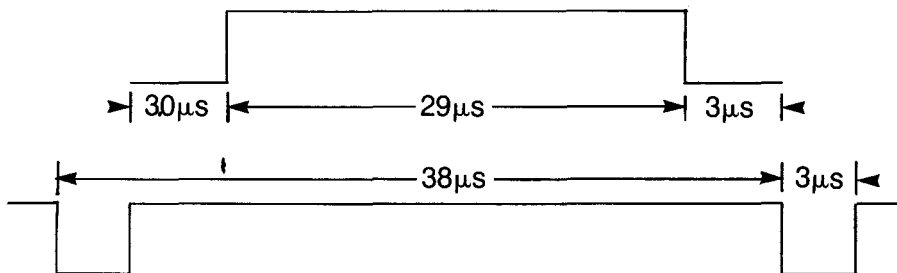
Switches 2 and 3—Leave these switches in the OFF position.

Switches 4 and 5—Consult the spec's of your monitor to set these switches.

SECTION 5

VIDEO TIMING DIAGRAM

Horizontal Sync

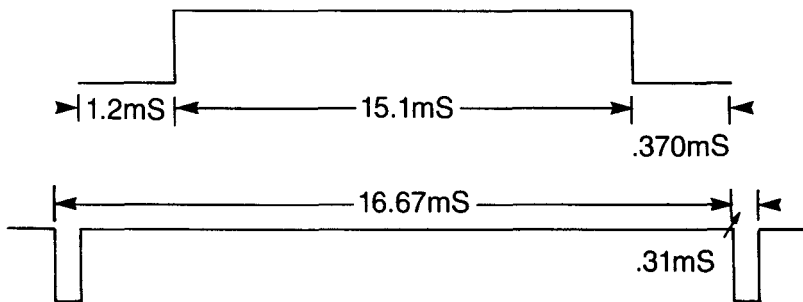


Horizontal Sync Rate may vary.

$$f_h = 26.4 \text{ KHz}$$

$$f_{\text{dot}} = 22.285 \text{ Mhz}$$

Vertical Sync



$$f_v = 60\text{hz}$$

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