2

Detailed System Operation

From the moment power is applied to the IBM PC, the electronics inside this machine synthesize into a functioning system whose purpose is to serve you. To a novice this seems like magic, but to the informed it's total logic–digital logic. This chapter describes the operation of the IBM in detail. Since Chapter 2 complements the SAMS COMPUTERFACT schematic diagrams, it will be helpful if you have these before you as you read the chapter. Some of the circuit schematics in the COMPUTERFACT are simplified in this text for ease in understanding a particular signal or data flow. References to COMPUTERFACT pages will be indicated as "CF page xx."

FOREWORD

The schematic symbols used in this book were adopted from those found in SAMS COMPUTERFACT CSCS2. A box enclosing a number represents a common test point. Because printing the "not" bar over signal labels is awkward in a text such as this, the active low representation of a signal will be indicated by the symbol * following the label. Thus, an active low reset signal will be represented as RESET*. The remaining symbols should be familiar to the reader. A description of the signal labels is provided in *Appendix C*.

THE POWER SUPPLY

When you reach around to the right side of the PC and rock the power switch to the ON position, energy flows from the power supply out across the system board like brightness returning to the earth as a large cloud passes by overhead.

Figure 2-1 is a block diagram of the switching power supply. Rocker switch S1 at the top left of CF page 8 allows 120 VAC across power cord P1 to be applied to the AC input board. It also provides 0.75 amp of filtered 120 VAC to a receptacle at the rear of the power supply for powering the IBM monochrome display. Up to 800 mA of current begins to flow through P2-J2 into the AC input board building a power field around AC line choke L1 (CF page 39) and passing through the primary input voltage protection fuse F1 and RF choke L3. Power is being felt at the J4 and P3-J3 connectors and the

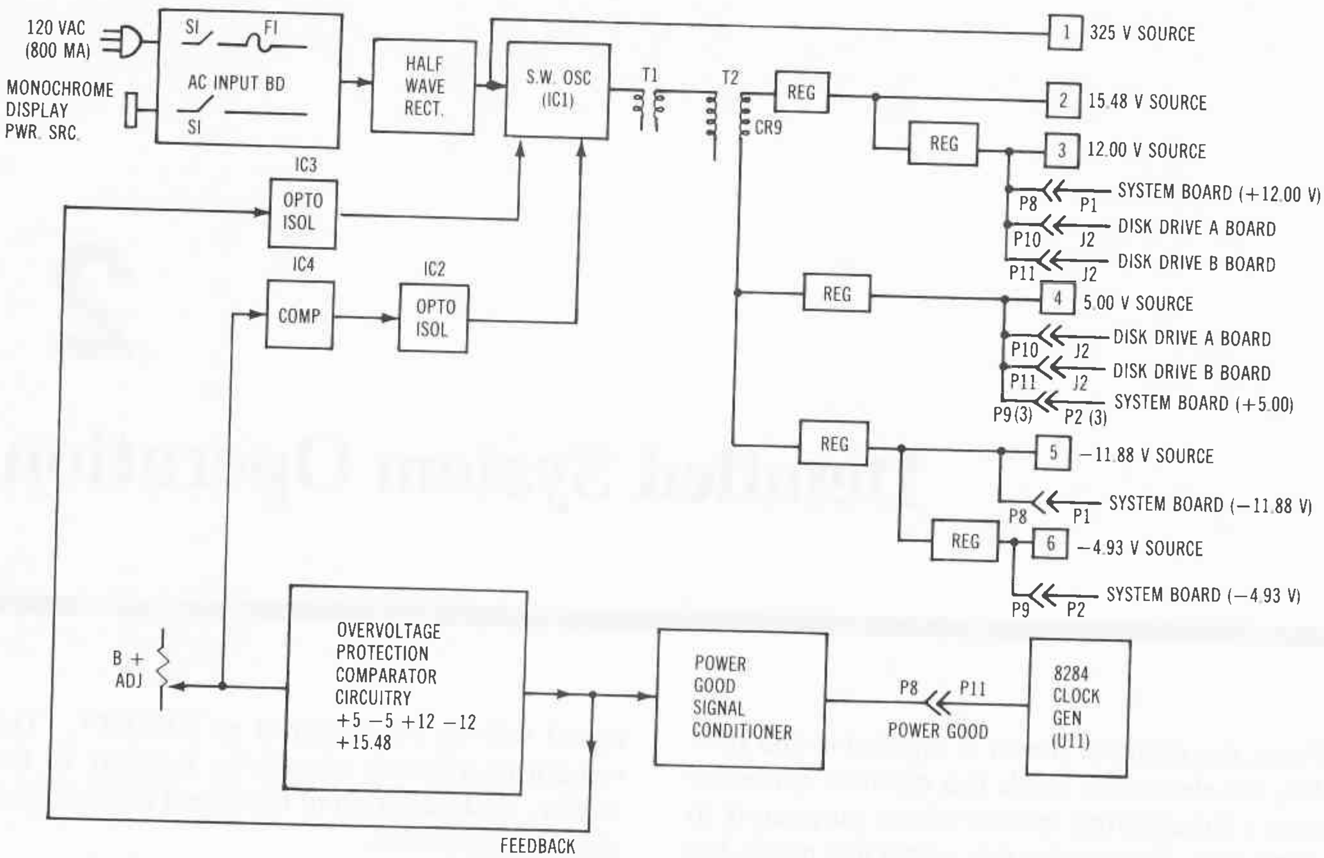


Fig. 2-1. Switching power supply block diagram.

combination of diodes CR1 and CR2 and capacitor C1. A 12 volt sawtooth waveform develops at the intersection of CR1 and C1. This signal becomes the 325V source (top right of CF page 9) that is fed forward as a reference for the oscillator circuitry on CF page 52.

At the same time, current is flowing at the box 35 junction through the ladder network R5, R6, R7, R8, R66, and R67 down CF page 8, across page 53 and up page 52 into the pulse transformer circuitry near T2. Current is also flowing horizontally from box 35 across the RC network of C2, C1, R69, R70, R71, R72, R73, R74, R75, and C10 into pin 1 of oscillator IC1.

Switching oscillator IC1 begins to conduct generating a 1 volt rectangular wave signal that is passed out pin 15 (CF page 53) to the base of oscillator driver Q2 causing Q2 to conduct producing an inverted signal on its collector. An 80 volt signal is felt across the primary of oscillator transformer T1.

The secondary of T1 is applied through the oscillator output circuitry of CR5 and Q1 to the primary of pulse transformer T2. The difference between the potential at the top and bottom of T2 primary is 143 volts as shown on CF page 52. The tapped secondary of T2 yields several voltage signals that are applied to regulator circuits to produce the switched voltages required by the system.

From the top of the T2 secondary, 37.15 volts (measured from T2 top to ground) is applied across diode CR9 to produce 15.48 volts source potential used by IC4, IC5, IC6, the B+ adjust circuitry, and cooling fan motor M1. This same 15.48 volts is also felt on the collectors of regulator Q7 and regulator driver Q6 producing up to 2.0 amps of current at 12.00 volts source potential at test point TP10 and connectors P8, P10, and P11. This 12 VDC level is used to power the system's dynamic memory and the internal 5¼ inch diskette drive motors.

From another tap, 13.00 volts AC is applied to the anode of CR10 producing a 5.10 volt signal that is felt at AC line choke L1 yielding up to 4 amps of 5.00 volts DC used throughout the PC system. This 5.00 volts is used as a reference by IC4, IC6, and power good driver Q4, and is felt at connectors P9, P10, and P11.

The bottom of T2 secondary is applied to the regulator circuitry of diode CR11, capacitor C27, and resistor R50 to produce a -11.88 volt source used as a reference by IC5 and felt at test point TP11, power-supply-to-system-board-connector P8, and on the input to regulator IC7. This -11.88 VDC is described as -12 VDC. Up to 0.25 amp of -12 VDC can be used with the +12 VDC by the system to power the EIA drivers on the communications adapters.

The -11.88 volt potential is applied to pin 2 of voltage regulator IC7 producing -4.93 volts used as a reference by IC6 and felt at test point TP9. This regulated voltage is the system -5 VDC applied through connector P9 and plug P2 to the system board provide dynamic memory bias voltage. The -5 VDC level tracks the +5 VDC and +12 VDC at power-on. It has a longer decay than the +5 VDC and +12 VDC levels at power-off.

Power supply output source voltages 5.00 volts, 12.00 volts, -4.93 volts, and -11.88 volts are monitored by the overvoltage comparator circuitry of IC5 and IC6. The 15.48 volt source is monitored via its use by the B+ adjust circuitry, and IC4, IC5, and IC6. Should an overvoltage or overload occur, the output of the overvoltage protection (OVP) circuitry of IC5 and IC6 drops to a low value reducing the LED intensity of opto isolator IC3. This shuts down switching oscillator IC1 dropping all source voltages to 0. All four of the primary voltages (+5, -5, +12, -12 VDC) are overvoltage, overcurrent, open-circuit, and short-circuit protected so catastrophic damage doesn't occur on the system or adapter boards should one of these conditions occur. An overvoltage, power-supply shutdown occurs if either the +5 or +12 VDC outputs exceed 200 percent of maximum rated voltage. The supply also shuts down if current through any output exceeds 130 percent of nominal voltage.

POWER GOOD SIGNAL

About 100 ms after the source voltages have reached their minimum sense level, the output of the OVP circuitry shown in Fig. 2-2 is felt on the base of power-good amplifier Q3 (CF page 53) causing Q3 to conduct placing 4.40 volts on the base of power good driver Q4 which also conducts. The collector output of Q4 sequences from 0.0 VDC (0.0 VDC to 0.4 VDC) capable of sourcing 500 μA to a TTL-compatible logic high (2.4 VDC to 5.5 VDC) capable of sourcing 60 μA. This nominal +5 VDC (measured 4.99) signal is called *power good*. Power good is applied through connector P8-P1 to pin 11 of clock generator (U11) on the system board initiating the awakening of the PC electronics. If the source voltages drop too low for Q4 to conduct, power good goes low disabling the clock at pin 8 of U11.

8088-BASED IBM PC SYSTEM

The IBM PC computer is constructed around the powerful 8088 central processing unit (CPU). The Intel 8088 (U3) shown in Fig. 2-3 is a third-generation microprocessor. This chip has 20 address lines so it can directly address 1 million bytes of memory. Sixteen of the address lines are used to access up to 64K of I/O memory. The I/O of the PC is memory mapped for easy access by CPU U3 and by application software.

The instruction/function format of the 8088 is identical to the 8086 microprocessor. The two machines differ in the size of the data bus. While the 8086 has a 16-bit data bus, U3 has an 8-bit external data bus. U3's standard 40-pin dual in-line package can be driven by a single +5 volt power source.

The CPU uses a time-multiplexed address and data bus format that permits several device pins to serve dual functions. During the machine cycle, eight address lines become data lines. Some of the control pins can also serve dual functions as determined by the strapping of the minimum/maximum (MN/MX) pin 33. In the IBM PC, MN/MX pin 33 is strapped to ground

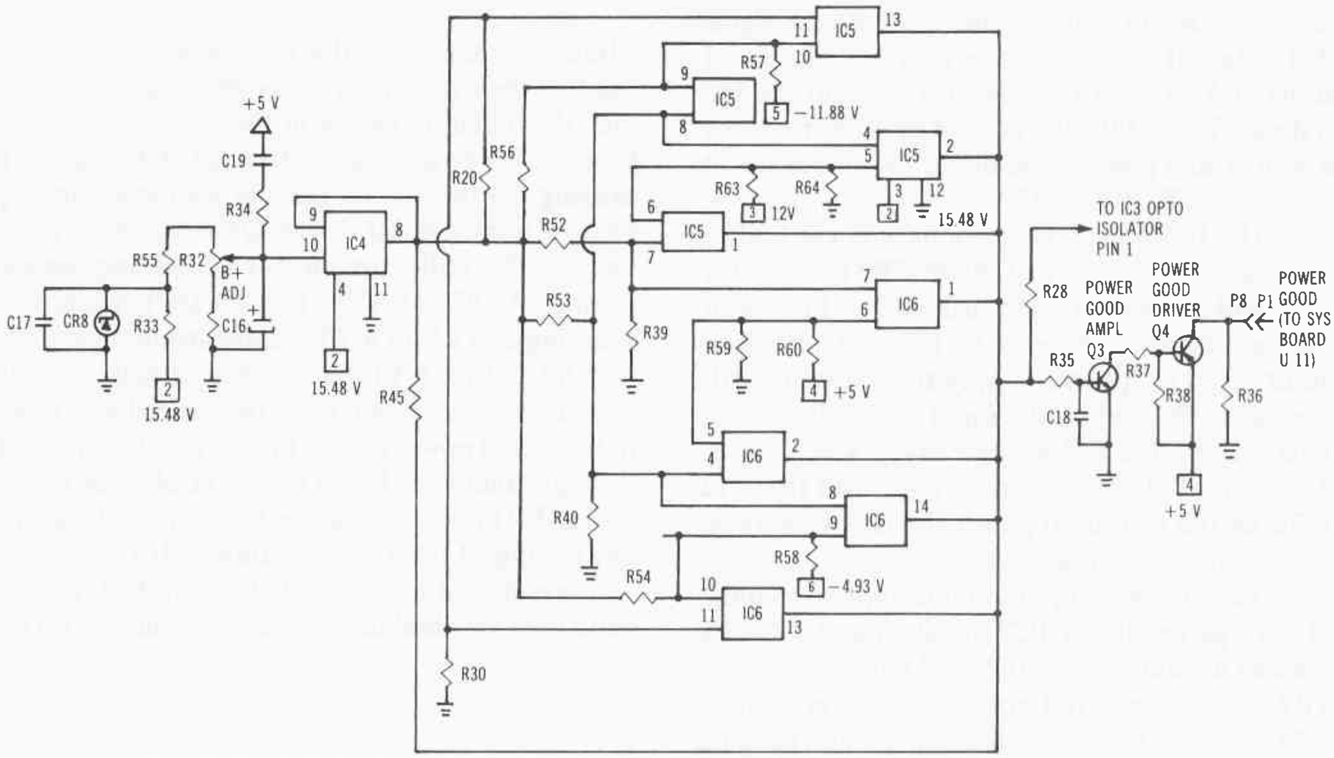


Fig. 2-2. Power good generation circuitry.

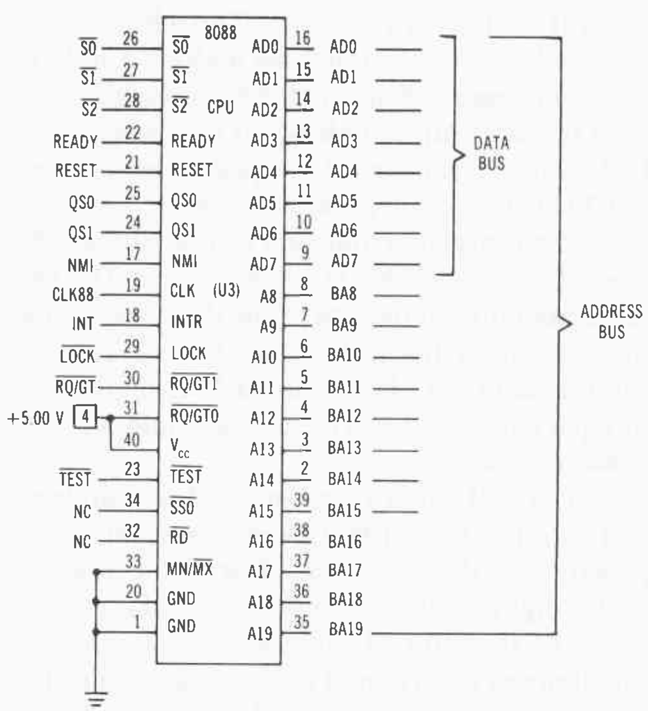


Fig. 2-3. Pin allocation for the 8088 CPU (U3).

placing U3 in maximum mode as shown in Fig. 2-4. In this configuration, U3 can support the 8087 local instruction set extension processor. An 8288 bipolar bus controller provides sophisticated bus control and command functions.

Basic to causing U3 to operate are the CLK88, READY, and RESET signals from the 8284 clock generator (U11).

Clock Generation Circuitry

The IBM PC's CPU requires a clock signal with fast rise and fall times (10 ns maximum). Its low value must be between -0.5 and +0.6 volt, and its high value must be between +3.9 volts and Vcc. The 8088 CPU incorporates dynamic cells. Therefore, a minimum frequency of 2 MHz to the CPU is required to retain the state of the machine.

With the four source voltage potentials being felt across the electronics of the system board and adapter cards, the PC begins to stir (electronically of course). Figure 2-5 shows that a 14.31818 MHz series resonant fundamental mode crystal has been connected across pins 16 and 17 of the 8284 clock generator and driver (U11) to produce the basic operating frequency. This clock crystal oscillates at three times the CPU frequency.

Input F/C (pin 13) is strapped to ground to permit the CPU's clock to be generated by the crystal rather than by an external frequency clock reference.

Because the oscillator will fail if the attenuation of the feedback circuit reduces the loop gain to less than one, series resistors R25 and R22 are connected to the input to the internal crystal oscillator. Resistors R13 and R22 stabilize the 14.31818 MHz reference signal applied to U11's internal crystal oscillator. The 14.31818

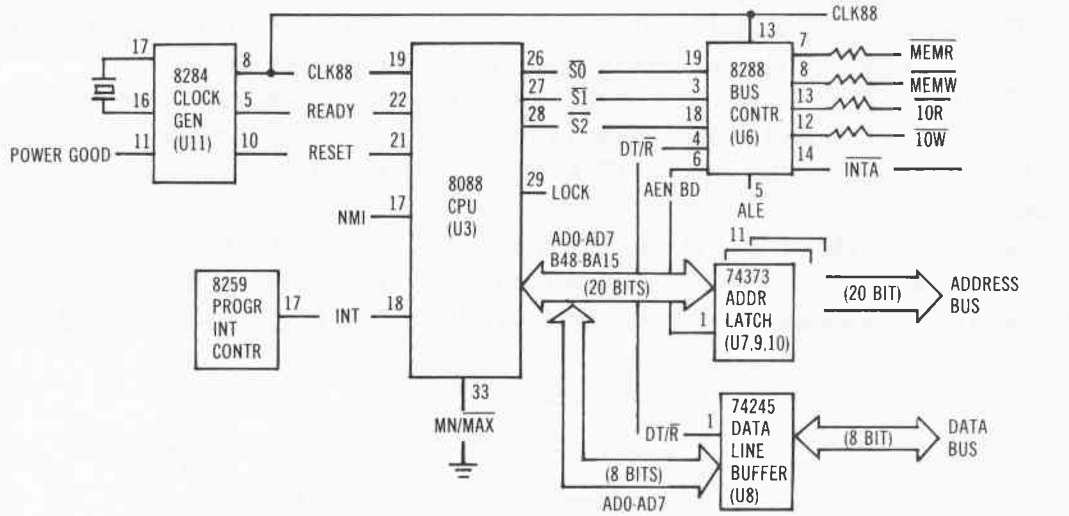


Fig. 2-4. 8088 maximum mode configuration.

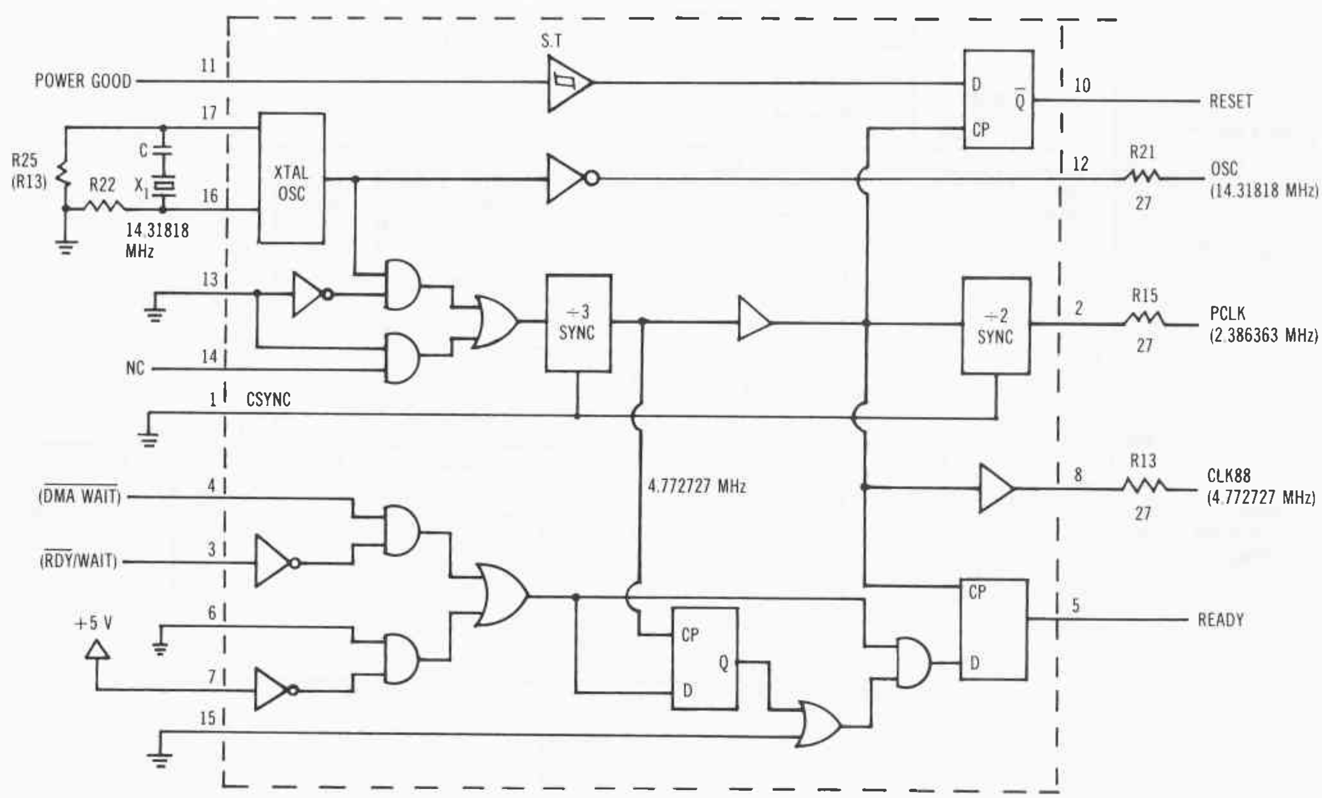


Fig. 2-5. 8284 clock generator (U11) circuitry.

MHz clock pulses coming out of the oscillator are buffered through an inverter and are made available at pin 12 as a 14.31818 MHz system oscillator signal OSC. The OSC clock signals are used by the color/graphics adapter board to develop synchronization and horizontal scan signals.

The output of the internal crystal oscillator in U11 is also applied to AND/OR and divide-by-three logic to produce a 33 percent duty cycle 4.772727 MHz clock signal optimized for the system's CPU at maximum frequency. The 4.772727 MHz clock is used to step the lower D flip-flop in Fig. 2-5 and is also passed through two buffers to become the system's CLK88 signal on output pin 8.

Since the state of U11 is indeterminate at power on, an external sync provides synchronization of the clock signals to the external crystal oscillation. Pin 1 input CSYNC is strapped low, so once the chip and crystal activate, the next positive clock from the frequency source starts the chip output clock generation.

CLK88 is applied directly to the 8088 CPU U3 (hence the label "Clock 88") and the 8087 math coprocessor (U4 on CF page 2), and 8288 bus controller (U6 on CF page 4), as shown in Fig. 2-6. It is also connected to pin 13 of 74LS244 tristate octal buffer (U15 on CF page 59) where it becomes the CLK signal for the expansion slots.

The output of the first buffer after the divide-by-three logic in Fig. 2-5 becomes a clock signal for two D flip-flops and a divide-by-two circuit. The divide-by-two circuit produces a 2.386363 MHz peripheral clock signal, PCLK, at output pin 2. PCLK has a 50 percent duty cycle and is connected to Fig. 2-6 pin 9 of 74LS175

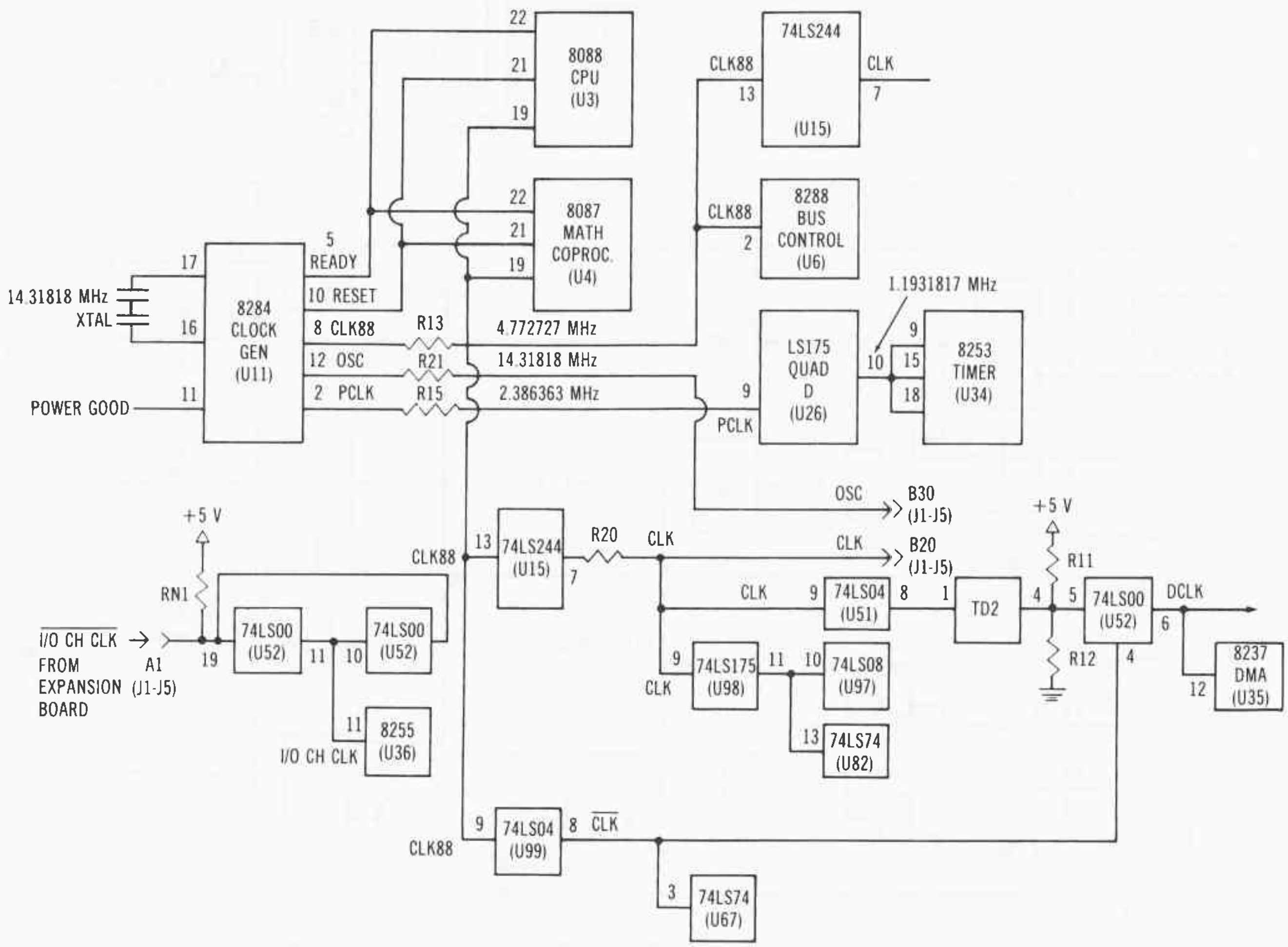


Fig. 2-6. Block diagram of clock circuitry in PC.

quad-D flip-flop (U26 on CF pages 4 and 57) which further divides it down to 1.1931817 MHz and passes it to pins 9, 15, and 18 of the 8253 programmable interval timer (U34).

All three output clock signals (OSC, PCLK, and CLK88) pass through individual 27 ohm series resistors which act to eliminate ringing.

Power good from Q4 in the switching power supply passes through Plug P1 on the system board to pin 11 of U11 (CF page 4). The power good input to U11 is not recognized until it drops at least below 2.6 volts. This input must remain below 1.05 volts for at least 50 μs after Vcc reaches the 4.5 volts minimum supply voltage–the maximum signal period is 124 μs.

Reset

As shown in Fig. 2-5, power good enters the RES* input to the 8284 clock generator and driver U11 to activate an internal Schmitt trigger producing a pulse input to the RESET D flip-flop. The flip-flop is used to synchronize the power good input with the CPU clock to generate the RESET signal to the CPU and a general reset to the entire system. Power good has no effect on the clock circuits within U11.

After the Schmitt trigger has fired, the trailing edge of the next 4.772727 MHz CLK88 pulse clocks the Schmitt trigger output into the flip-flop and shortly thereafter, the Q* output goes high sending a RESET signal out pin 10 to the components shown in Fig. 2-7.

The RESET signal enters the 8255 programmable peripheral interface (U36) on pin 35 clearing its control register and setting all ports to the input mode.

The signal also enters the 8087 math coprocessor (U4) on pin 21 clearing its internal registers and preparing it for 8088 support operations.

When RESET is felt on pin 21 of the 8088 CPU (U3), its internal registers are zeroed, and its code segment (CS) register is preset to 0FFFFH, the initialization address for future operations.

The active high RESET signal enters the 8237 DMA Controller (U35) on pin 13 causing its internal timing and control section to disable all four direct memory access channels, clearing the command status, request, temporary registers, and the first/last flip-flop. It also sets the mask register and places the device in an idle cycle mode. The 8237 programmable DMA controller (U35) will be covered shortly.

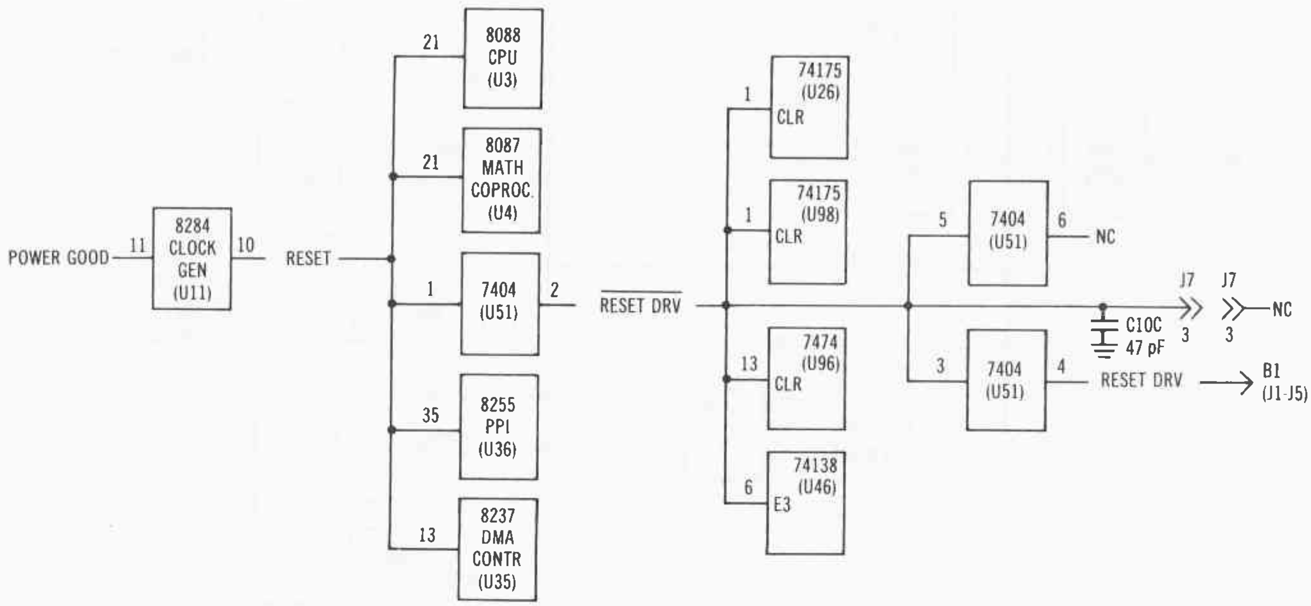


Fig. 2-7. The RESET circuitry.

RESET also passes through pin 1 of a 74LS04 hex inverter (U51) to become the active low reset drive (RESET DRV)* signal at its pin 2 output, as shown in Fig. 2-8. (RESET DRV)* is used to reset or initialize system logic upon power-up or during a low line voltage outage. It is applied to the clear input (pin 1) of two 74LS175 quad D latches (U26 and U98) and to the clear input (pin 13) of 74LS74 dual D latch U96 where it is used to reinitialize the non-maskable interrupt (NMI) circuitry. (RESET DRV)* is also applied to the active high E3 enable input (pin 6) of 74LS138 decoder (U46). (RESET DRV)* is terminated with a 47 pF capacitor (C10C) and is connected to an unused pin of keyboard connector J7.

Finally, (RESET DRV)* from U51 pin 2 is passed back into its pins 3 and 5. The pin 3 input becomes an active high RESET DRV signal pin 4 output and is made available to the expansion boards via pin B2 on J1 through J5. The pin 6 output of hex inverter U51 is not used.

8088 CPU OPERATION

With the system in a reset condition and the clock oscillator running, the machine pulses into action. The key to all the activity is the 8088 CPU (U3).

As shown in Fig. 2-9, the 8088 CPU incorporates two separate processing units: an execution unit (EU) and a bus interface unit (BIU). Standard microprocessors with a sequential CPU architecture execute programs by fetching an instruction, executing the instruction, and then fetching the next instruction in a long time-consuming sequence. The logic in the CPU must wait for the fetch and instruction decoding operations before execution can begin. The control and arithmetic logic must spend a lot of overhead time waiting. Intel eliminated this wasted time by partitioning the 8088 CPU into two independent sections.

Operating in a pipelined fashion, the BIU fetches and temporarily stores instructions in a

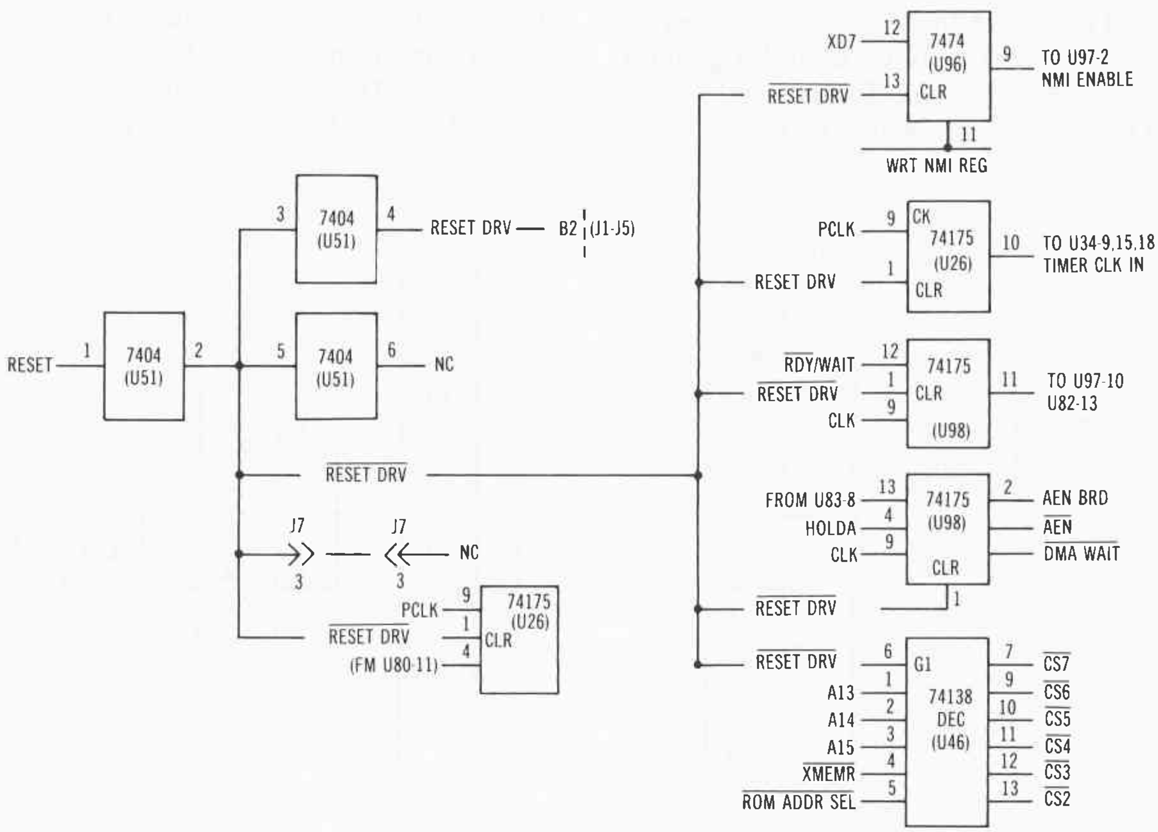


Fig. 2-8. Reset drive circuitry.

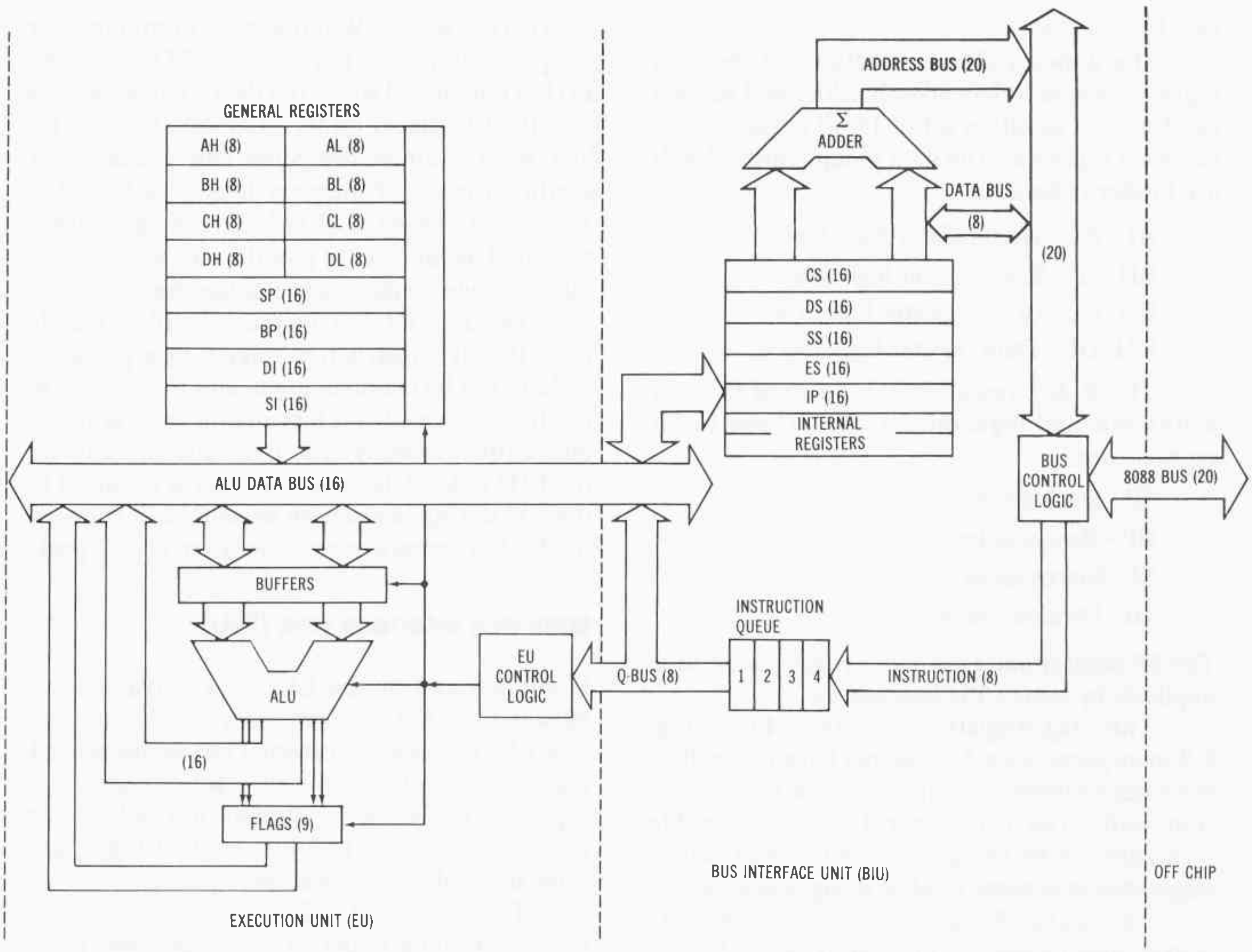


Fig. 2-9. The 8088 microprocessor block diagram.

queue of four registers. It also inputs and outputs data or operands. The EU is isolated from the chip I/O pins by the BIU. The EU executes the instructions read into a 4-byte instruction queue by the BIU. The BIU writes the results. When 1 byte of the BIU instruction queue is empty, the BIU executes an instruction fetch cycle to access one instruction object code byte per bus cycle. If the EU needs the data bus, it issues a request for access to the BIU which completes any instruction fetch cycle and then acts on the EU request.

8088 Execution Unit

The EU executes all the instructions, provides data and addresses to the BIU, and manipulates its general and flag registers. It contains a 16-bit arithmetic logic unit (ALU) that interacts with the instruction operands from the BIU queue and its general registers. The EU also maintains CPU status and control information in a flag register. All the data paths in the EU are 16-bits wide for optimum internal information transfers. The EU interfaces with the BIU via a byte-wide instruction operand O-bus between the BIU instruction queue and the EU control logic. A second interface is via the 16-bit ALU data bus.

Eight 16-bit general registers support the operation of the BIU. Collectively acting as an accumulator, these registers are divided into two sets of four registers: the high and low byte data registers (AH, AL, BH, BL, CH, CL, DH, and DL), and four P & I pointer and index registers

(SP, BP, DI, and SI).

The upper and lower sections of the data registers can be independently addressed so each can function as either a full 16-bit register or as two 8-bit registers. The data group register labels are further defined as

AH, AL - Accumulator high, low

BH, BL - Base register high, low

CH, CL - Count register high, low

DH, DL - Data register high, low

The P & I registers can be used in most arithmetic and logic operations. These 16-bit registers are

SP - Stack pointer

BP - Base pointer

SI - Source index

DI - Destination index

The SP pointer and both index registers are used implicitly by some CPU instructions.

The Flag Register below the CPU in Fig. 2-9 incorporates six 1-bit status flags that reflect conditions following an arithmetic or logic operation, and three 1-bit control flags that enable interrupts to be recognized by the ALU allow single-step operation, or alter string operations.

The status flags can cause certain CPU instructions to execute differently depending on the state of these flags. The six status flags are

OF - Overflow flag

SF - Sign flag

ZF - Zero flag

AF - Auxiliary carry flag

PF - Parity flag

CF - Carry flag

The three control flags are

TF - Trap flag

DF - Direction flag

IF - Interrupt enable flag

With these powerful registers and flags, the EU obtains instructions stored in the BIU queue and performs arithmetic, logic, move, shift, or other operations depending on the code in the instruction word. When access to memory or peripheral devices is required, the EU causes the BIU to obtain and store the data. The addresses that the EU places on its ALU data bus are 16-bits wide. Since the 8088 can access over a million bytes of memory locations (2E20 = 1.048,576), the ALU data bus 16-bit address is relocated by the BIU to give the EU access to the full megabyte memory space of the chip.

The EU fetches instruction object code from the BIU instruction queue, interprets the code in the EU control logic, and then executes the instruction. If no instruction code is in the queue (queue empty), the EU waits patiently for the BIU to load its queue. If data is required by the EU during instruction execution, it requests the BIU to access a memory location or I/O port.

8088 Bus Interface Unit (BIU)

Upon demand by the EU, data is transferred between the BIU and memory or I/O devices. The BIU executes all external bus cycles according to command from the EU. It is comprised of segment registers, a summation adder, an instruction queue, I/O bus control logic, and some internal communication registers.

The adder in the BIU combines segment and offset values to derive 20-bit addresses giving the 8088 a direct access memory space of 1 million bytes.

8088 Instruction Queue

An internal 4-byte microinstruction pipeline storage memory called the "instruction queue" enables the BIU to prefetch and temporarily hold instructions for use by the EU with minimum machine delay. While the EU is busy executing instructions, the BIU fetches more instructions from program memory keeping its pipeline queue full. Whenever the queue has an empty byte location and the EU is not requesting the external bus, the BIU fetches another instruction to keep the queue full. Maximum program execution speeds are achieved because the EU does not have to wait for each fetch operation.

The instructions fetched by the BIU are stored in sequential ascending order in memory. If the EU transfers control to another microinstruction memory location, the BIU resets the queue, passes the new instruction through its queue into the EU, and then begins refilling the queue from that portion of program memory. Fetch operations are suspended whenever the EU requests a memory or I/O access.

8088 Segment Registers

The 1 megabyte memory space of the 8088 CPU is divided into 64K byte logical segments. Four of these segments can be directly accessed by the CPU using four special 16-bit registers. These segment registers are labelled:

CS - Code segment
DS - Data segment
SS - Stack segment
ES - Extra segment

These registers hold the starting locations of four 64K logical segments. Each segment is a logical portion of contiguous memory locations and is independent and separately addressable. A unique base address is assigned to each segment to indicate its starting point in memory space. Segment base addresses begin on 16-byte memory boundaries. Therefore, as long as the boundary base line is maintained, segments can be adjacent, overlapped, or separated by unassigned memory locations.

The CS register holds the base address of the current code segment. The BIU fetches instructions from the 64K-byte portion of memory indicated by the address in the CS register. The SS register points to the top of the stack segment. Register DS points to the current data segment, and ES points to the current extra segment of data storage.

Each of these segment registers is accessible to the programmer. Using the four currently addressable segments, a software engineer can generate a program to access code and data in other segments of memory space by changing the segment registers base addresses. The current base addresses provide 256K bytes of work space–64K for microinstruction code, a 64K deep stack, and 128K of data storage.

8088 Instruction Pointer

A 16-bit program counter called the "instruction pointer" (IP) is updated by the BIU to contain the number of bytes the next instruction is offset from the base address in the current code segment register. Thus, the IP points to the next instruction to be fetched by the BIU. When the IP value is saved on the stack in the SS register, it is first adjusted to point to the next instruction to be executed. Instructions are densely packed into memory. They vary in length from 1 to 6 bytes in length. As the BIU fetches an instruction, the code in the first byte (called an "opcode") identifies the type of instruction and whether there are more bytes comprising the total machine instruction.

PHYSICAL ADDRESS GENERATION

As shown in the 8088 pin allocation diagram of Fig. 2-3, the 20-bit 8088 address bus exits 8088 CPU U3 on pins 2 through 16 and pins 35 through 39. The lower 8 bits of the 8088 output (pins 9 through 16) are bidirectional. During the later half of a machine cycle these pins are bidirectional and contain data. During the address generation part of the cycle, these same pins become part of a 20-bit address bus (pins 2 through 16 and pin 39) over which the CPU communicates with the rest of the IBM PC circuitry. This time multiplexing of bidirectional lines enables larger memory address space using fewer I/O pins.

A physical 20-bit address uniquely identifies each byte in a 1 megabyte memory space accessible by the CPU. With 20 bits in each address word, a physical memory range between 00000H and FFFFFH can be directly accessed in the IBM PC.

The powerful programming capability of the 8088 enables logical addressing using the segment registers and the instruction pointer. Each logical address is comprised of a segment value indicating the first byte in that 64K segment and an offset value defining the distance in bytes from the base address. The 16-bit segment base line address is shifted left 4 bits and combined with a value stored in an offset register to form a 20-bit physical address as shown in Fig. 2-10.

Many different logical addresses can map to the same physical address. In Fig. 2-11, physical address 03B4H can be reached via a segment base address of 03B0H with an offset of 4H and a segment base address of 03ADH with an offset value of 7H.

BIU program memory accesses are achieved by generating a physical address from logical segment and offset values. The segment base address is shifted 4 bits in the BIU summation adder and is then added to the offset value stored in the IP, SP, SI, or DI registers. It can also be an effective address as shown in Table 2-1. The logical address is obtained from different sources depending on the type of memory reference. Instructions are fetched from the current segment base line by the CS register. The IP register contains the offset of the target instruction from the segment base address.

For stack operations, the SS register contains the starting address of the current stack segment. The stack pointer (SP) register in the EU holds the offset value from the top of the stack to the stack segment base address.

Memory operands are assumed to be within the current data segment, but the BIU can access these variables in other currently addressable segments. To reach these, the offset value is calculated by the EU based on the addressing mode indicated by the microinstruction. In this case, the offset is called the operand's "effective address" (EA).

Table 2-1. Sources for Logical Address in the 8088 CPU

Memory Reference Type	Default Segment Base Register	Alternate Segment Base Register	Source for Offset
Instruction fetch operation	CS	none	IP
Stack operation	SS	none	SP
String source	DS	CS, ES, SS	SI
String destination	ES	none	DI
Variable (except following)	DS	CS, ES, SS	effective address
BP used as base register	SS	CS, DS, ES	effective address

Other memory references are possible and other EU and BIU registers can be caused to participate in the generation of a logical address for mapping into a physical address by the BIU summation adder.

THE CPU BUS CYCLE

To understand the multiplexing operation, you must first recognize that the fetch, decode, execute, and data transfer actions occurring in the CPU constitute a machine, or bus cycle. The

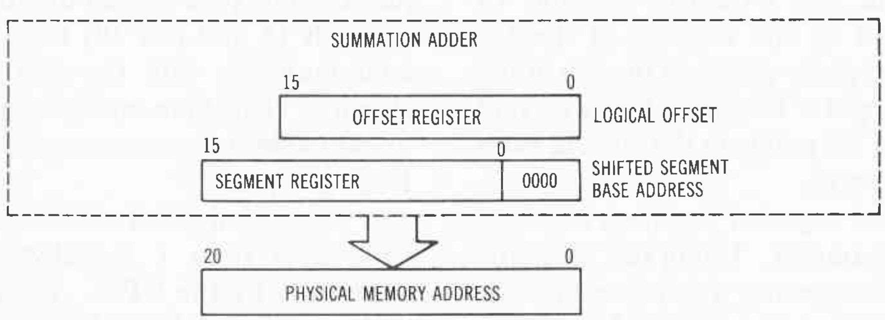


Fig. 2-10. A logical 16-bit address added to an offset 16-bit segment base address produce a 20-bit physical address.

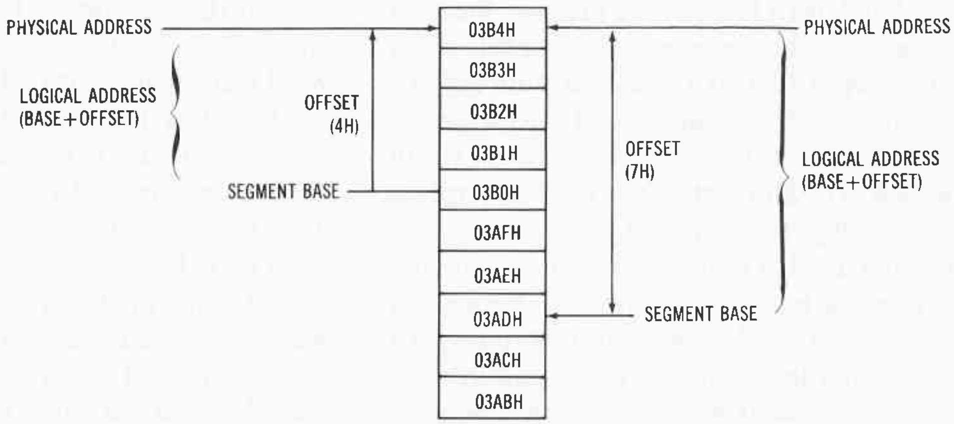


Fig. 2-11. Different logical addresses can map to the same physical address.

minimum bus cycle consists of four 8088 clock cycles. Each cycle of the CLK88 signal is called a "tick" and is represented by the letter "T." Up to six T states can be required for a single bus cycle. If the memory or I/O circuitry cannot transfer data fast enough, the 8088 CPU (U3) introduces special wait states (called TW) to cause the CPU to cycle in place by inserting additional clock ticks into the bus cycle until the selected device (memory or I/O) communicates to U3 that it is ready to continue. Fig. 2-12 shows the bus cycle associated with U3. Notice that the T-state begins on the falling edge of CLK88.

Because the IBM PC uses the 8088 in its maximum mode, any change in the status signals S0*, S1*, and S2* on pins 26, 27, and 28 of U3 during T4 indicates the beginning of a new bus cycle. These status signals start to change during T4 and become valid during T1 and T2. When T3 begins (or during TW if READY is high), these lines return to a passive state and indicate the end of a bus cycle. Status signals S0*, S1*, and S2* are used by the 8288 bus controller (U6) to generate all memory and I/O access control signals.

Once the S0*-S1*-S2* T4 change has been recognized by U3, T1 begins with the falling edge of the next clock cycle. During T1, U3 places an address code on the 20-bit time-multiplexed

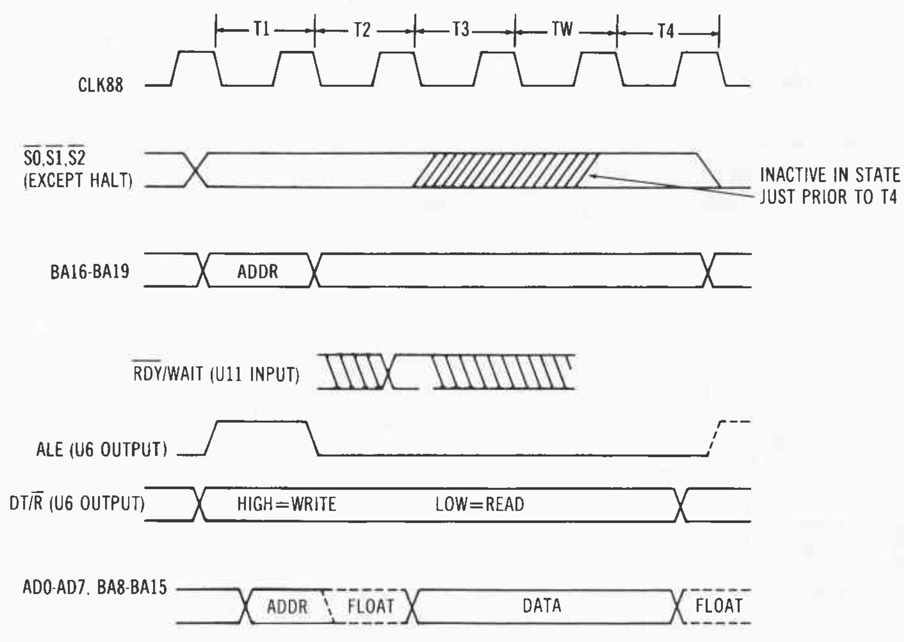


Fig. 2-12. 8088 CPU bus cycle.

address/data bus to identify the memory location or I/O device to be accessed. During this clock cycle, the top 4 bits of the 20-bit address are present on pins 35 through 38 and constitute the most significant part of the address bus (BA16 through BA19). The rest of the address appears on pins 8 through 16 and pin 39.

During T2, U3 issues an activity command on the control bus. The address information which was valid on the lower 16 bits during T1 shifts to a high impedance tristate condition if the control command is to read, or they become valid data for memory or I/O if the command is to write. Data read and write, and interrupt acknowledge control commands are active during T2. Also during T2, the upper four address lines (A16 through A19) contain bus cycle status information.

Read or write commands become valid during T3 guaranteeing sufficient time for data information to settle on the bus before command activation. Status information is present on the top 4 bits of the address bus, and data is valid on the lower 16 address/data bits.

If the memory or I/O device is slower than the 8088 CPU, it causes the READY signal from 8284 clock generator (U11 to U3 input pin 22) to be held low forcing U3 to generate TW wait states until READY returns high. The circuitry shown in Fig. 2-13 is used to generate the READY signal that passes out pin 5 of U11 into 8088 CPU U3. CF pages 2, 4, and 57 apply.

During the last TW state (or during T3 if no wait states are requested) U3 latches data on the bus. When T4 occurs, the command lines are disabled and the bus is released by any external device holding control. From a device view external to U3, the bus cycle is an asynchronous event comprised of an address to select the device followed by a read command or data and a write command. Data is copied onto the data bus by the device during a read cycle and accepted by the device from the data bus during a write cycle. The devices only control over the bus cycle is via TW wait states. The *Intel iAPX 86/88, 186/188 User's Manual* contains additional information on the 8088 bus cycle.

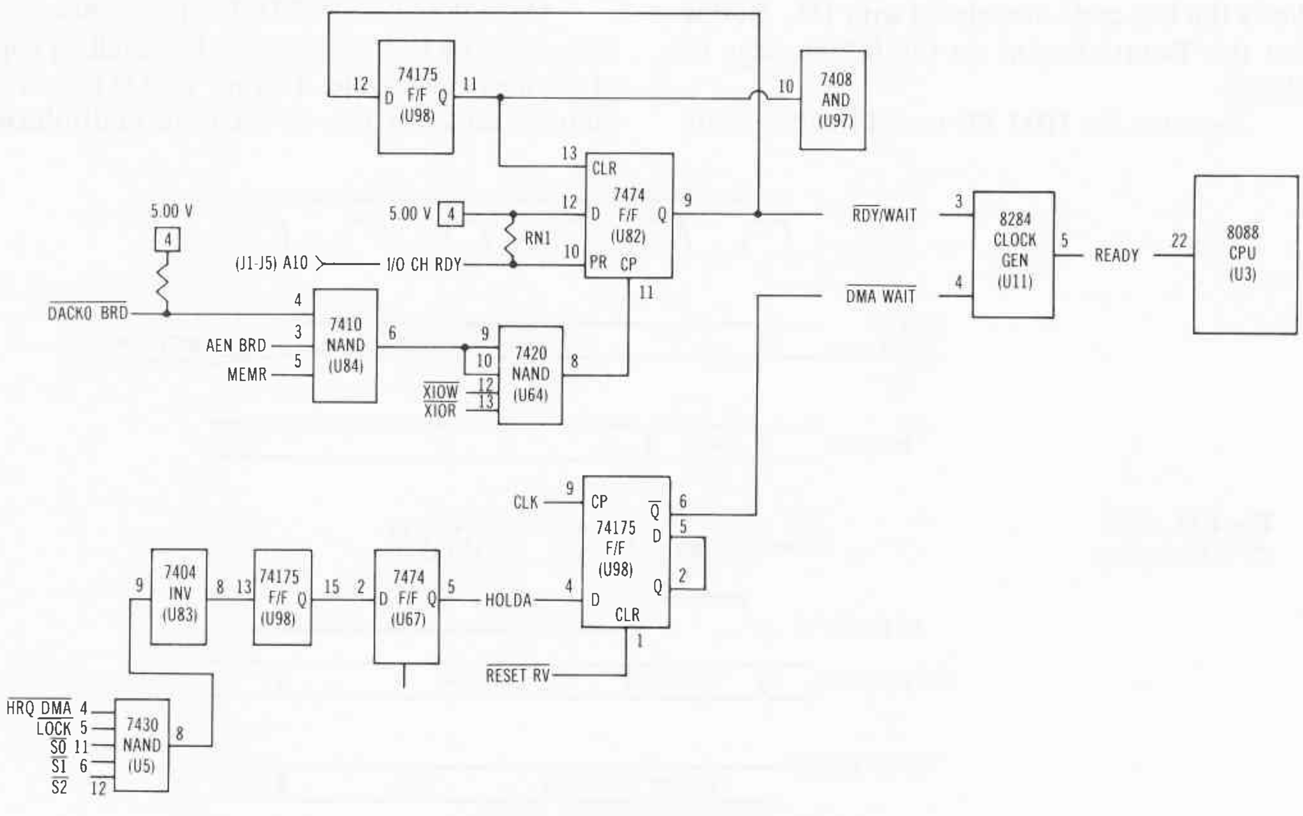


Fig. 2-13. READY signal circuitry.

Critical to the smooth operation of the bus cycle is the 8288 bus controller (U6), shown in Fig. 2-14. The 8288 is a 20-pin bipolar part that provides command and control timing signals and bus drive enable signals to the PC circuitry.

The chip has seven input pins. Pin 1, input/output bus (IOB) mode, is strapped low placing the chip in the system bus mode. In this configuration no command is issued until 155 ns after the AEN BRD line (pin 6) goes low. In this mode both I/O and memory can be shared by the 8088 CPU (U3) and the 8087 coprocessor (U4).

The 8088 status inputs (S0*, S1*, and S2*) on pins 3, 18, and 19 are decoded inside U6 to generate timed command and control signals. Table 2-2 is a decoding of the status bit inputs to U6.

The IBM PC system clock (CLK88) from the 8284 clock generator (U11) enters the 8288 on pin 2. This clock signal is used to establish when the timed command and control signals occur. Figure 2-15 is a block diagram of the bus controller circuitry.

Another input, active low address enable (AEN*) from pin 3 of 74LS175 quad-D flip-flop U98 (Fig. 2-15 and CF Page 4) enters U6 on pin 6. AEN* enables command outputs at least 115

Table 2-2. 8288 Status Bit Decoding

Status Bits S2* S1* S0*			8288 Command Generated	CPU Cycle
0	0	0	INTA/	Interrupt acknowledge
0	0	1	IOR/	Read I/O port
0	1	0	IOW/	Write I/O port
0	1	1	-	Halt
1	0	0	MEMR/	Instruction fetch
1	0	1	MEMR/	Read memory
1	1	0	MEMW/	Write memory
1	1	1	-	Passive

ns after it goes active (low). When this occurs, the command outputs immediately shift to a high impedance state. Figure 2-15 shows that AEN* also connects to pin 6 (G1 enable) of 74LS138 decoder U66 (CF page 3).

The other important input to the 8288 bus controller U6 is an active high address enable board (AEN BRD) control signal (U6 pin 15) from the Q output of U98 (pin 2). AEN BRD is used to enable the outputs of U6. This signal is also applied to one input (pin 15) of 74LS244 tristate buffer U15 to generate an active high AEN on output pin 5. AEN is passed to the A11 pins of socket connectors J1 through J5 (CF page 56) for use by peripheral boards. AEN BRD

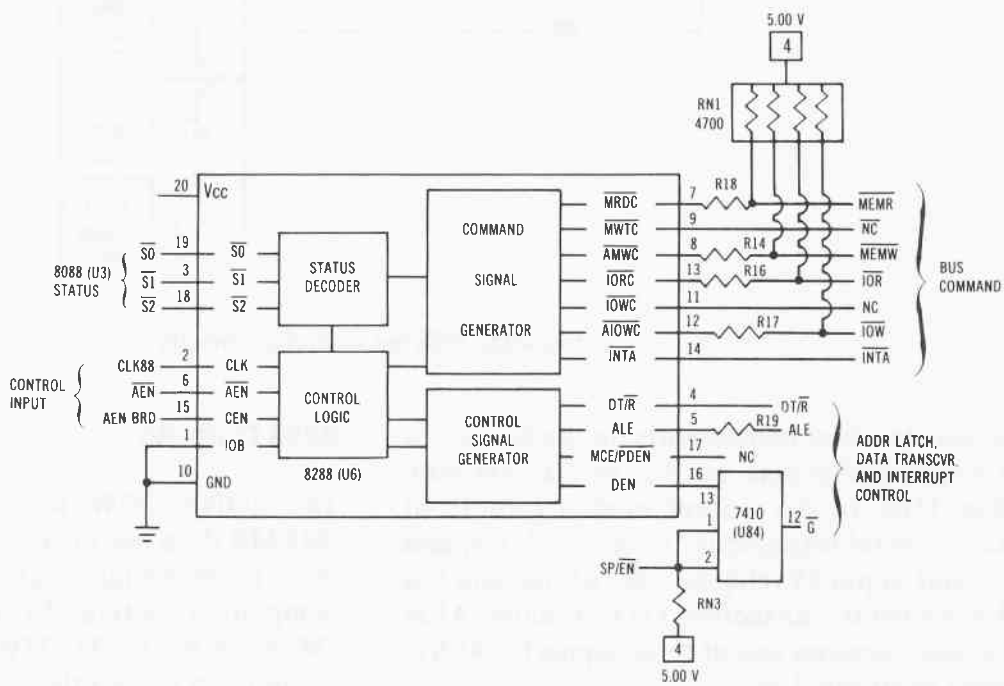


Fig. 2-14. 8288 bus controller (U6).

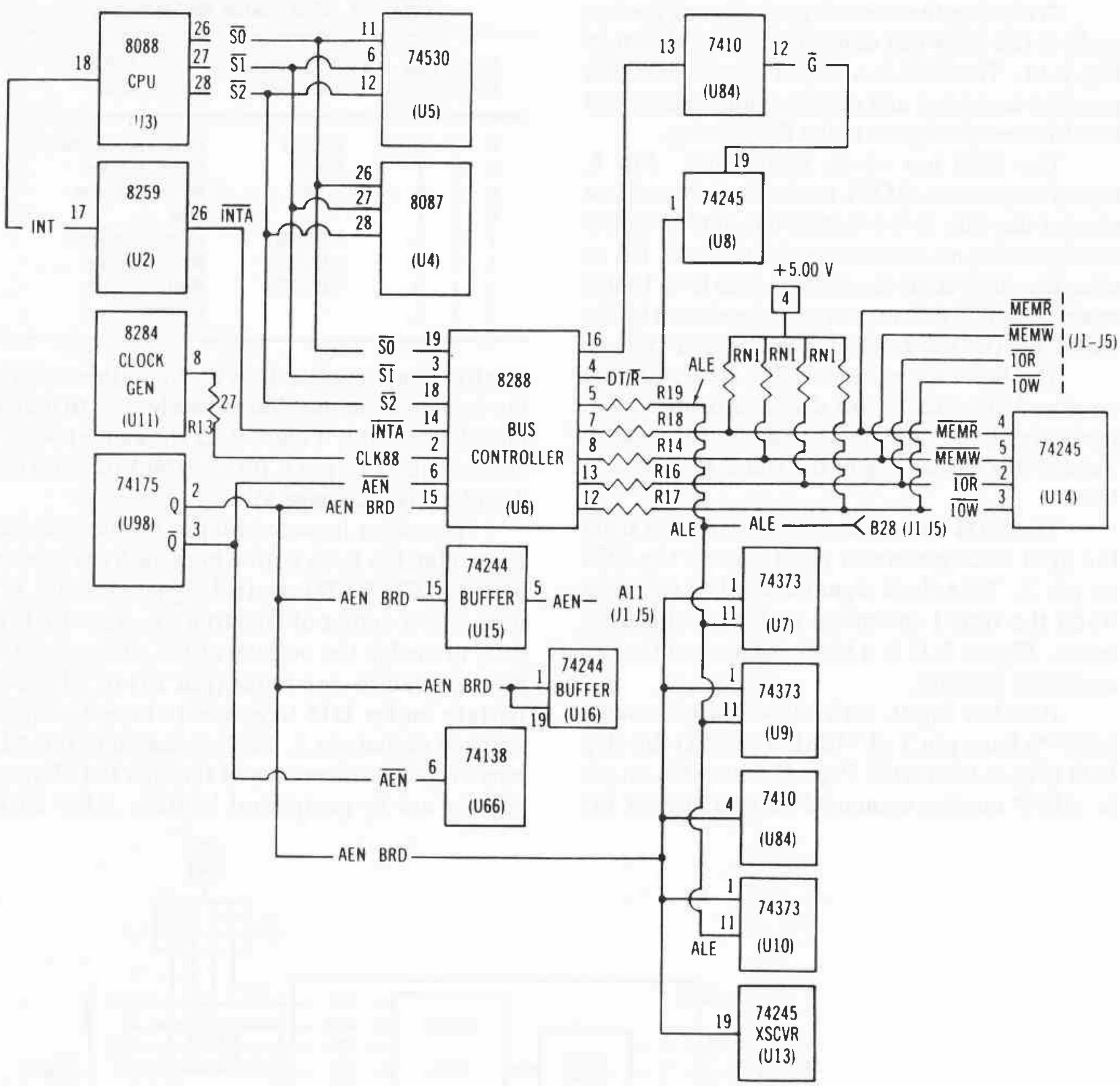


Fig. 2-15. 8288 bus controller circuitry.

connects to other components on the board: to the output enable pins 1 and 19 of 74LS244 octal buffer U16, to the output enable (pin 1) of 74LS373 octal transparent latches U7, U9, and U10, and to pin 19 (chip enable) of the data bus 74LS245 octal transceiver U13. Finally, AEN BRD also becomes one of three inputs to 74LS10 3-Input NAND gate U84.

8288 Outputs

The active LOW Memory Read command (MEMR)* on pin 7 causes the system memory to drive its stored information on the data bus. Its companion active LOW output command (Memory Write) MEMW* on pin 8 causes the memory to record the information now on the data bus. Peripheral devices are controlled using the two active low IOR* and IOW* commands out pins 13 and 12 respectively. These command signals instruct I/O devices to drive data onto or read data from the PC data bus.

Pin 14 is the Interrupt Acknowledge INTA* active LOW output that is connected to input pin 26 of 8259 PIT U2. This signal is used to tell U2 that its interrupt has been recognized by CPU U3 and when U2 should place its vector data onto the data bus.

The outputs on the lower right of Fig. 2-15 are the control signals that interface with the address latches, data transceivers, and interrupt control. Data transmit/receive DT/R* out pin 4 of U6 connects to pin 1 of 74LS245 transceiver U8 where it determines the direction of data bus signal flow through U8. When DT/R* is high, data is sent out (transmit) 8088 U3 to I/O or memory. A low on the DT/R* pin 1 input to U8 causes data to be read from (receive) I/O or memory into U3.

The control signal out pin 5 of 8288 U6 is address latch enable (ALE). This signal is used to strobe an address into the 74LS373 address latches U7, U9, and U10 (shown on the far right of CF page 2 and in the logic diagram for the 8288 bus controller circuitry, Fig. 2-15). This ALE signal is active high and enters all three 73LS373 components on pin 11 (enable). Latching occurs on the falling (high to low) transition of the signal. ALE is also passed from pin 5 of 8288 U6 out to pin B28 of J1 through J5 interface connectors (CF page 56).

The active high data enable output from U6 pin 16 connects to the pin 13 input to 74LS10 three-input NAND U84 (CF page 4) where it is matched with the slave program/enable buffer (SP/EN)* output from pin 16 of 8259 programmable interrupt controller U2 to produce active enable signal G*. Whenever DEN on pin 16 of U6 and SP/EN* on pin 16 of U2 are high, G* is generated and becomes an active low enable to pin 19 (enable input) of 74LS245 address/data bus transceiver U8. Signal G* combines with active low DT/R* to enable signal flow from left to right through U8 as the 8088 CPU U3 or 8087 coprocessor U4 reads data from I/O or memory.

Figure 2-16 shows the timing relationships between the input and output signals of the 8288 bus controller.

The 8288 memory and I/O command signals MEMR*, MEMW*, IOR*, and IOW*, are important in proper functioning of the PC. These signals will be described in detail later in this chapter.

8253 PROGRAMMABLE INTERVAL TIMER

As shown in Fig. 2-17 (see also CF page 57), the D8253C-5 programmable interval timer U34 does three important functions in the IBM PC: it generates a time of day clock tick; it tells the DMA controller when to refresh the dynamic RAM in the system; and it helps produce sound from the machine's speaker.

The nMOS 8253 peripheral device is organized as three independent 16-bit down-counters, each with a count rate up to 2 MHz. The input clock to U34 comes from PCLK in 74LS175 quad D flip-flop U26. This causes U34 to count at a 1.1931817 MHz rate. The three output signals OUT0 (IRQ0), OUT1 (to U67), and OUT2 (TIMER/CNTR2 to U63) occur at a frequency determined by PCLK divided by a software programmable 16-bit number. U34 is used to generate accurate time delays under software control minimizing program overhead.

Upon initialization, each timer in U34 is preconfigured via a unique control word and a count quantity value sent by the 8088 CPU. These data enter U34 on pins 1 through 8 (XD0 through XD7). The initialization software writes out to U34 a *mode* control word and the programmed number of count register bytes desired.

Comprised of 8 bits, the "mode control byte" initializes a particular counter with the desired *mode*. Six modes are available:

Mode 0–Interrupt on terminal count.

Mode 1–Programmable one-shot.

Mode 2–Divide-by-N rate generator.

Mode 3–Divide-by-N square-wave generator.

Mode 4–Software triggered strobe.

Mode 5–Hardware triggered strobe.

The 8 bits of the mode control byte are allocated as follows:

Bit 0–ount in binary if equal to 0, otherwise count in BCD.

Bit 1-3–Defines which mode is desired.

Bit 4,5–Read/load sequence.

Bit 6,7–Defines which counter is to be affected.

Once the mode control word has been received, a count register in each counter is preloaded in the sequence defined by the mode control word. Each counter clocks down to zero so the value loaded into the count register decrements with each input clock pulse. Loading all zeroes into a count register causes that counter to count down from a maximum value (65,536 for binary, 10,000 for BCD). Once programmed, the counting operation is completely independent. Upon count start, the 8253 causes each counter to clock down until the preset delay value reaches zero. At this point, the zeroed counter generates a count-complete output showing it has completed its tasks.

The IBM PC software configures U34 so OUT0 operates in Mode 3 so it produces a symmetric output with equal high and low parts of each cycle. This signal becomes IRQ0, the time of day interrupt. Here, the mode control byte was 00110110 (36H) defining binary count, Mode 3, read/load the low byte, then the high byte, and identifying the counter as counter 0. Inside counter 0, its count register is loaded with the binary value 00000000 (decimal 00, hex 00H). This preset causes a maximum count delay

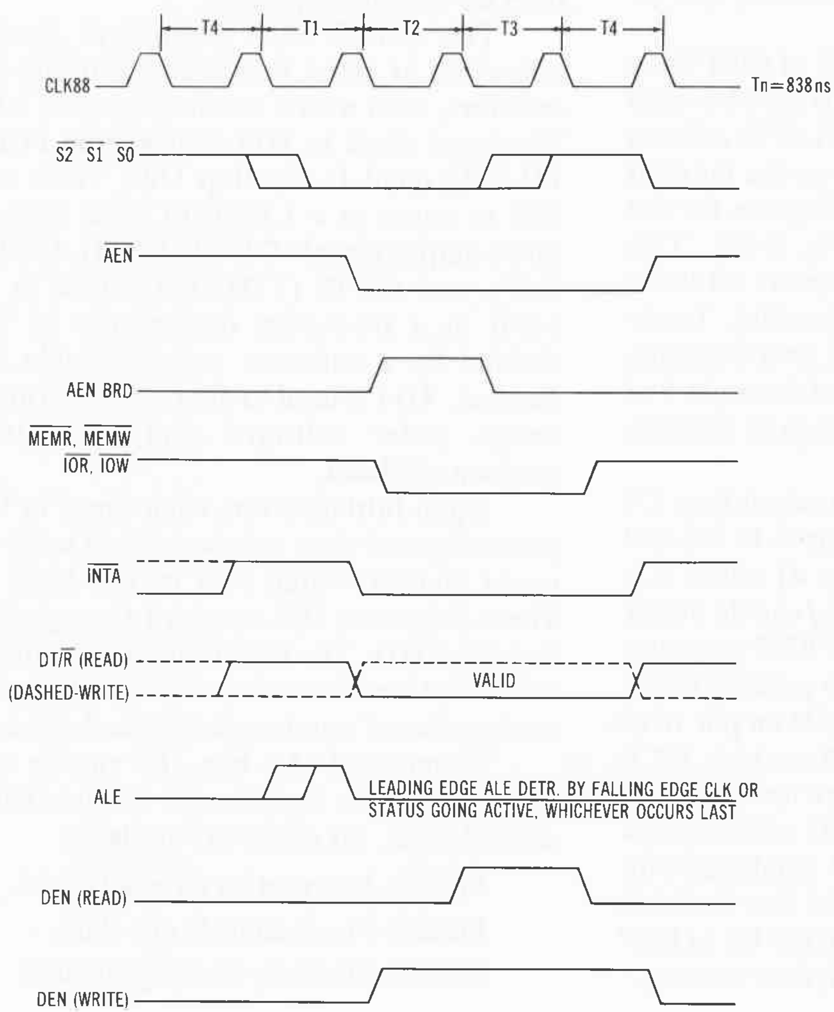


Fig. 2-16. 8288 timing waveforms.

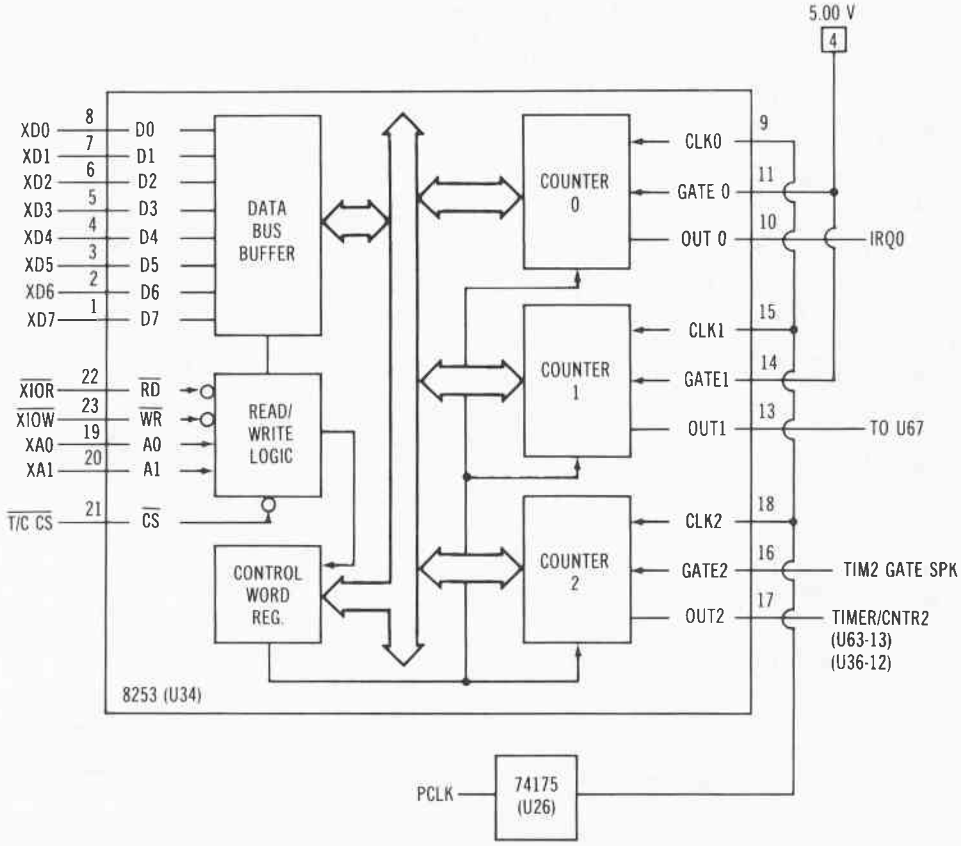


Fig. 2-17. 8253 programmable interval timer.

producing an OUT0 (IRQ0) signal approximately 18.2 times each second (1.1931817 MHz divided by 65,536 = 18.207 cycles per second).

Counter 1 was preset by loading the hex value 54H into the control word register. In binary, this is 01010100 (decimal 84) representing binary counting, Mode 2 (rate generator), read/load a low byte only, and its destination is counter 01. The counter 1 count register is preset with the binary value 00010010 (12H, decimal 18) causing this counter to produce a pin 13 OUT1 signal 66,287 times a second (1.1931817 MHz = 1193181.7 Hz, so 1,193,181.7/18 = 66287.87 cycles per second). The 66.287 kHz OUT1 signal (15 microseconds) enters pin 11 of 7474 D latch U67 (see Fig. 2-18) where it becomes DRQ0 for the 8237 DMA controller U35. DRQ0 is used to tell U35 when to refresh the dynamic RAM every 15 microseconds.

The input to the U34 word control register for counter 2 is the mode control byte 10110110 defining binary count, Mode 3, read/load low byte, then high byte, and set destination as counter 2. The preset value for the counter 2 count register is 0000 0101 0011 0011 (533 hex, 1331 in decimal). This produces an 896 Hz square wave output (1,193,181.7/1331 = 896.455 cycles per second) from pin 17 OUT2 (Fig. 2-18). OUT2 from U34 pin 17 is the TIMER/CNTR2 signal sent back to input pin 12 of the 8255 programmable peripheral interface U36 (Fig. 2-18) and on into pin 13 of 7438 two-input NAND U63. In U63, TIMER/CNTR2 is NANDed with SPKR DATA from pin 19 of 8255 PPI U36 to produce speaker activation signals. To make the speaker beep using the TIMER/CNTR2 896 kHz square wave, pins 18 and 19 of 8255 U36 (TIM2 GATE SPK and SPKR DATA) must be set high for the duration of the sound desired. OUT2 can be varied by presetting the counter 2 count register with different values producing different output frequencies under software control.

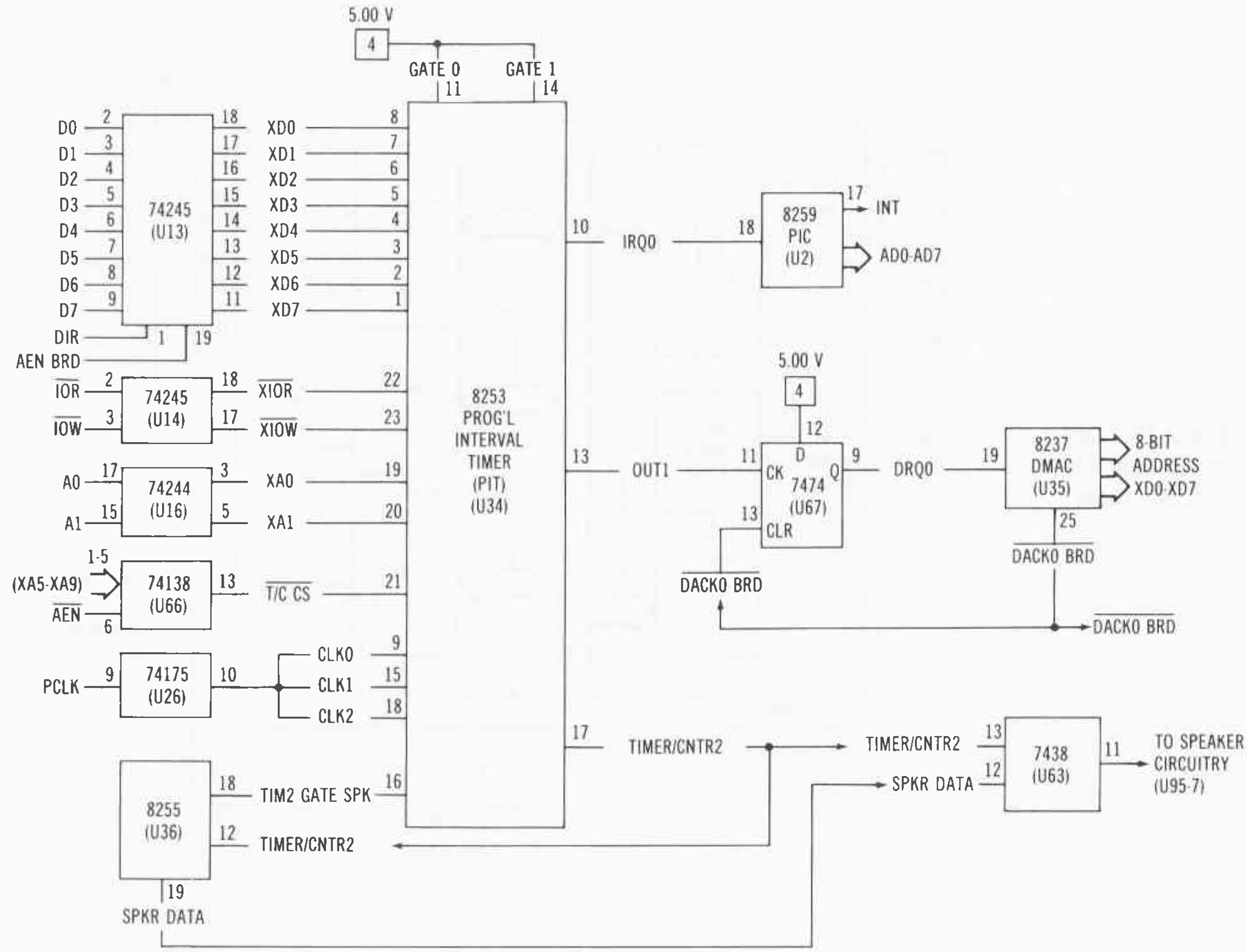


Fig. 2-18. 8253 timer circuitry.

8237 PROGRAMMABLE DMA CONTROLLER (DMAC)

The 8237 multimode direct memory access (DMA) controller (DMAC) (U35) in the IBM PC system is designed to improve system performance by allowing external devices to directly transfer information from peripheral devices (I/O) to memory or between memory and memory in up to 64K-byte blocks. The DMAC is used to suspend normal 8088 CPU operation so it can take over the system address, control, and data buses and conduct a data transfer at rates up to 1.5 megabytes per second. Innovative circuit design ensures that U35 takes bus control only at the end of a machine cycle and when LOCK* is high (not active). When DMA is active, U35 causes the address, control, and data buffers for CPU U3 to go tristate. U35 then causes the 8284 clock generator (U11) to pull READY low forcing U3 to insert wait states in its machine cycle while U35 conducts the DMA transfer.

DMAC U35 contains four independent request/acknowledge channels which can automatically reinitialize to a preprogrammed condition following an end of process (EOP*) signal. Each channel has a 64K address and word count capability. Fig. 2-19 is a block diagram overview of the 8237 DMAC. Inside the block are the vendor labelled pin descriptions. On the outside of the block are the signal labels generated by IBM. Arrows show direction of signal flow.

There are three basic blocks of control logic in Fig. 2-19. The timing and control block

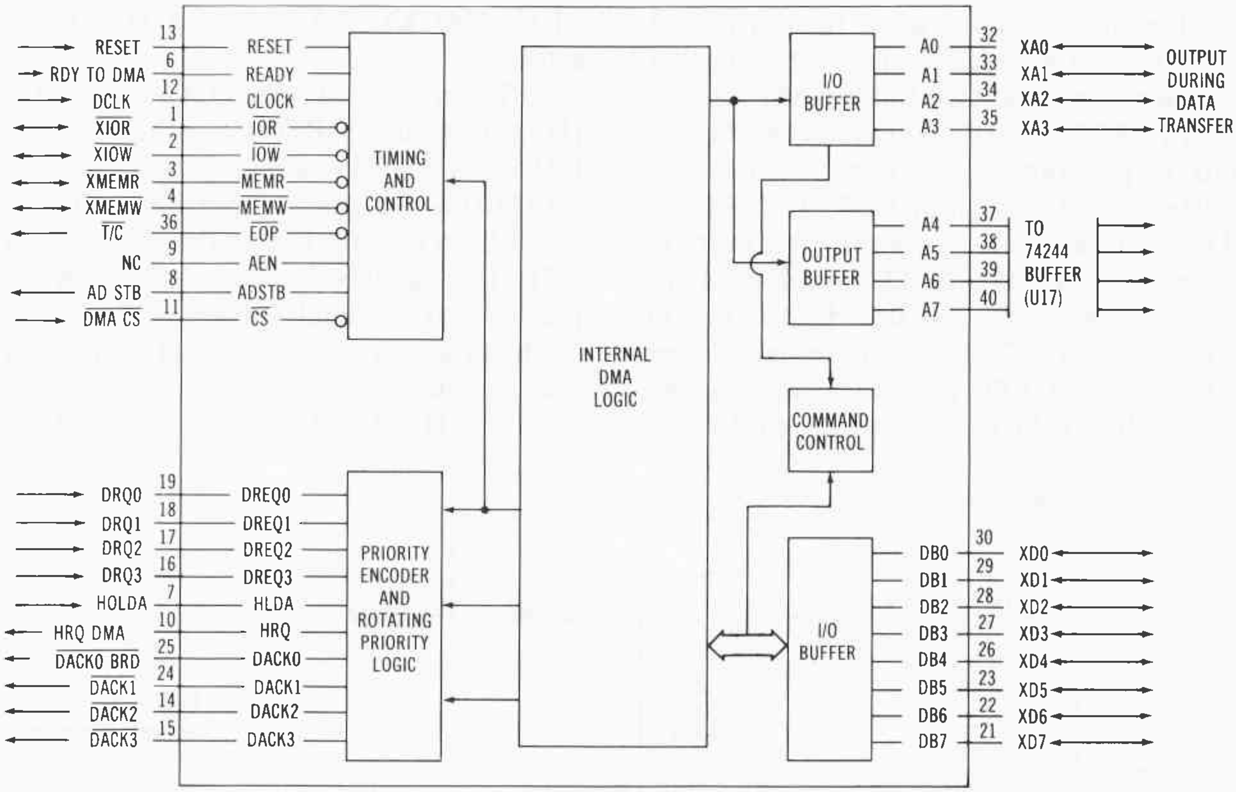


Fig. 2-19. 8237 programmable DMA controller (U35).

generates internal timing and external control signals for the chip. The internal DMA logic block decodes the various commands sent to U35 by 8088 CPU (U3) before servicing a DMA request. This block also decodes a mode control word used to select the type of DMA to be performed. The priority encoder and rotating priority logic block in the lower left of Fig. 2-19 resolves priority contention between DMA channels requesting simultaneous service.

Internal timing in the timing and control block is achieved using the 4.77 MHz DCLK (U35 pin 12) from 74LS00 U52 pin 6 in the PC clock generation circuitry.

The RESET signal on input pin 13 comes from pin 10 of 8284 clock generator U11. Activation of the power good signal from the switching power supply (described earlier) causes U11 to generate the active high RESET signal. When pin 13 goes high, it clears special registers inside the 8237 and a first/last flip-flop. Then the chip goes into an idle state until a valid DMA request arrives.

In the idle state, U35 samples the four DRQx lines (DRQ0, DRQ1, DRQ2, and DRQ3) with each DCLK input pulse to determine if any channel is requesting a DMA transfer. U35 also samples the DMA chip select input (DMA CS)* on pin 11 if the 8088 CPU is attempting to read or write to its internal registers. When (DMA CS)* and HOLDA (pin 7) are low, U35 enters a program state in which the CPU U3 can access the internal registers of U35. Address lines XA0 through XA3 act as inputs to U35 to select which internal registers will be written into or read from. The XIOR* and XIOW* signals on pins 1 and 2 are used to select and time the read or write operations.

In the program state, special software commands can be executed by U35 using sets of addresses and the (DMA CS)* and XIOW* signals. The software commands include clear first/last flip-flop and master clear.

As shown in Fig. 2-20, four DMA request channels connect to U35 (pins 16, 17, 18, and 19). These request lines are individual asynchronous channel request inputs used by peripheral circuitry to obtain DMA service. They are in a fixed priority with DRQ0 holding the highest priority (DRQ3 lowest). The polarity of these signals is programmable. These signals are initialized to active high by RESET. DRQ0 is used to produce a memory refresh cycle every 15 microseconds. DRQ1, DRQ2, and DRQ3 are available on the expansion slots for use in I/O data transfers. DRQ2 is used to initiate floppy disk transfers. DRQx must be held until the corresponding DACKx acknowledge (DACK0 BRD, DACK1, DACK2, and DACK3) goes active.

When one of the DMA request lines (DRQ0 through DRQ3) goes high requesting DMA service, U35 outputs a hold request DMA (HRQ DMA) signal out pin 10 to pin 1 of the 74LS04 hex inverter U99 in the upper left of Fig. 2-21. This signal becomes an active high input to pin 1 of 74LS74 dual-D latch U67 clearing the latch for activation by a signal on pin 2 a few microseconds later.

The HRQ DMA output on pin 3 of U52

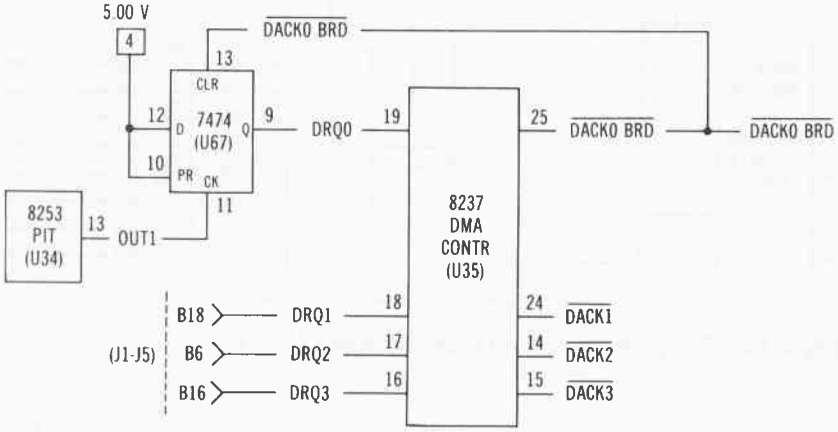


Fig. 2-20. DMA request circuitry.

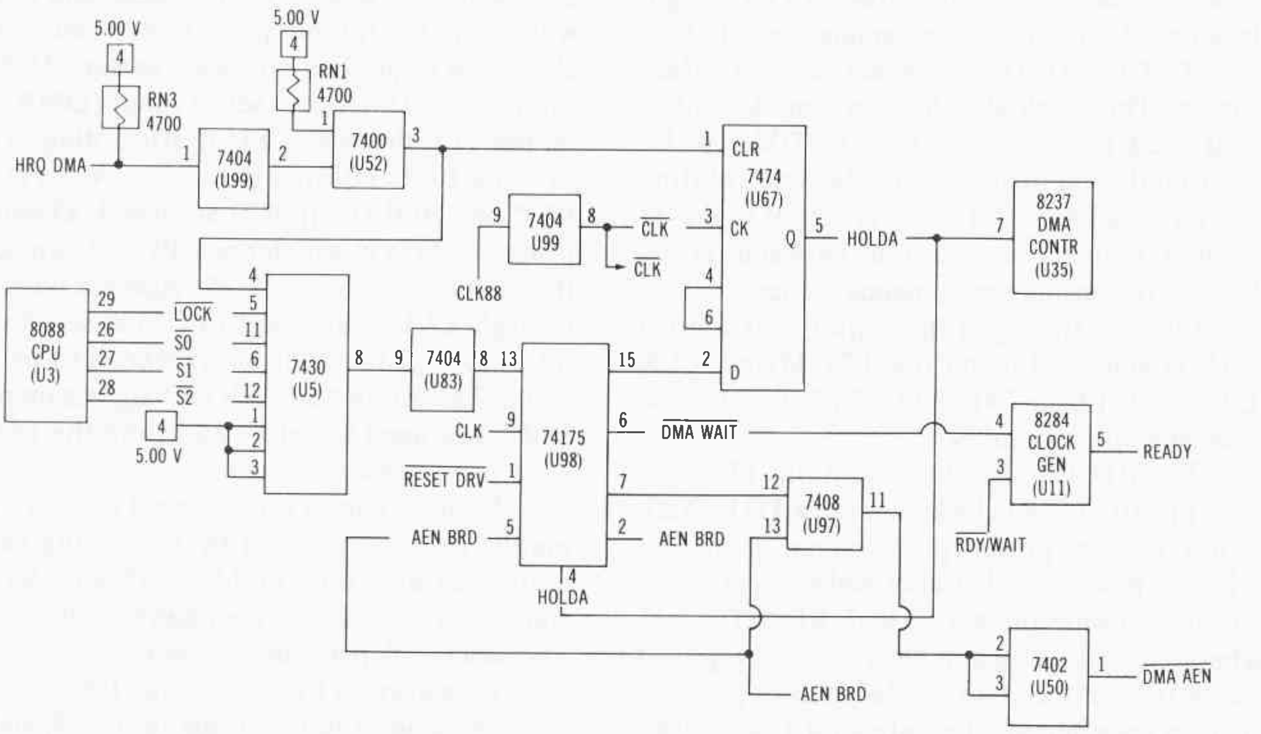


Fig. 2-21. HRQ DMA to HOLDA circuitry.

also becomes one input to 74LS30 eight-input NAND (U5) where it is matched with LOCK*, and the 8088 status signals S0* and S1* from U3 to produce an active high output from pin 8 into pin 9 of hex inverter U83, out pin 8 and into pin 13 (D input) of 74LS175 quad-D latch U98. The Q output from pin 15 of U98 becomes the D input to 74LS74 dual-D latch U67 generating HOLDA out the Q output on pin 5. This causes CPU U3 to tristate its address, data, and control signals giving 8237 U35 control over the address, data, and control buses.

HOLDA feeds back to pin 4, the D input to a latch in U98 generating signal AEN BRD out pin 2. AEN BRD is passed back into the D input (pin 5) of U98 producing (DMA WAIT)* out pin 6. This signal enters pin 4 of 8284 clock generator (U11) to combine with the RDY*/WAIT signal of pin 3 determining the logic state of the READY output from pin 5 into pin 22 of 8088 CPU (U3).

Back to the upper right of Fig. 2-21, HOLDA also feeds out pin 5 of U67 into pin 7 of 8237 U35 indicating that the CPU has relinquished control of the system buses and DMA transfers can proceed.

The first DMA request (DRQ0) comes from the pin 9 Q output of 7474 D latch (U67), shown in Fig. 2-20 and on CF page 57. This signal was developed from the OUT1 signal on pin 13 of the 8253 programmable interval timer U34. Every 72 clock cycles (15 microseconds) programmable interval timer U34 generates OUT1 on pin 13. This signal which clocks a logic high into the D input (pin 12) of U67 producing an active high DRQ0 out pin 9 and input on U35 pin 19.

DRQ0 causes DMAC U35 to produce an output (DACK0 BRD) that causes a memory access that refreshes the charges in the DRAM ICs on the system board. Every 15 microseconds, DMA channel 0 is activated causing a memory access operation. As shown in the upper left of Fig. 2-22, the active high DRQ0 signal in pin 19 causes U35 to generate a (DACK0 BRD)* acknowledge signal out pin 25. This signal is used to clear U67 so another DRQ0 can be generated 15 microseconds later. It also initiates a RAM refresh cycle by activating four row address select (RAS) lines while disabling all memory chip address select (CAS) lines. This also prevents using DRQ0 for anything other than memory refresh.

(DACK0 BRD)* enters pin 13 of 74LS74 U67 to clear this latch and ready it for another OUT1 clock on pin 11. It also goes to pin 6 of 74LS138 decoder U48 where it combines with A18 and A19 to produce RAM address select (RAM ADDR SEL)* out pin 15. (DACK0 BRD)* passes through 74LS244 (U15) to become DACK0* input to the refresh circuitry in the upper right of Fig. 2-22. DACK0* enters pin 1 of 74S00 (U81) to generate (REFRESH GATE)* out pin 3 and to 74LS08 (U49). DACK0* is also passed to pin B19 of expansion slots J1 through J5.

(DACK0 BRD)* also is inverted in 74S04 (U83) to become DACK0, an enable input on pin 4 of 74LS138 decoder U65. Decoder U65 generates the signals that become the active low row address selects (RAS0*, RAS1*, RAS2*, and RAS3*) out pins 3, 6, 8, and 11 of 74LS08 (U49).

Decoder 74LS138 (U47) uses (DACK0 BRD)* on G1 enable input pin 6 to prevent generation of memory column address strobe signals (CAS0*, CAS1*, CAS2*, and CAS3*) out pins 12 through 15). The disabling of all chip address strobe lines ensures that DRQ0 is used only for memory refresh operations.

The other three DMA request channels (DRQ1 through DRQ3) shown in Fig. 2-20 come from pins B18, B6, and B16 respectively on connectors J1 through J5. These request signals cause U35 to generate acknowledge active low signals DACK1*, DACK2*, and DACK3* out pins 24, 14, and 15, as shown in Fig. 2-23. These acknowledge signals tell an individual peripheral that a DMA cycle has been granted. They are used to produce chip select signals to the I/O devices causing the devices to place an input byte on the data bus. The active low DMA acknowledge signal (DACKx through DACK3*) also supplies a memory address and signals the destination to read the address.

Notice that DACK2* and DACK3* are also passed onto pins 4 and 5 of 74LS670 4 x 4 tristate

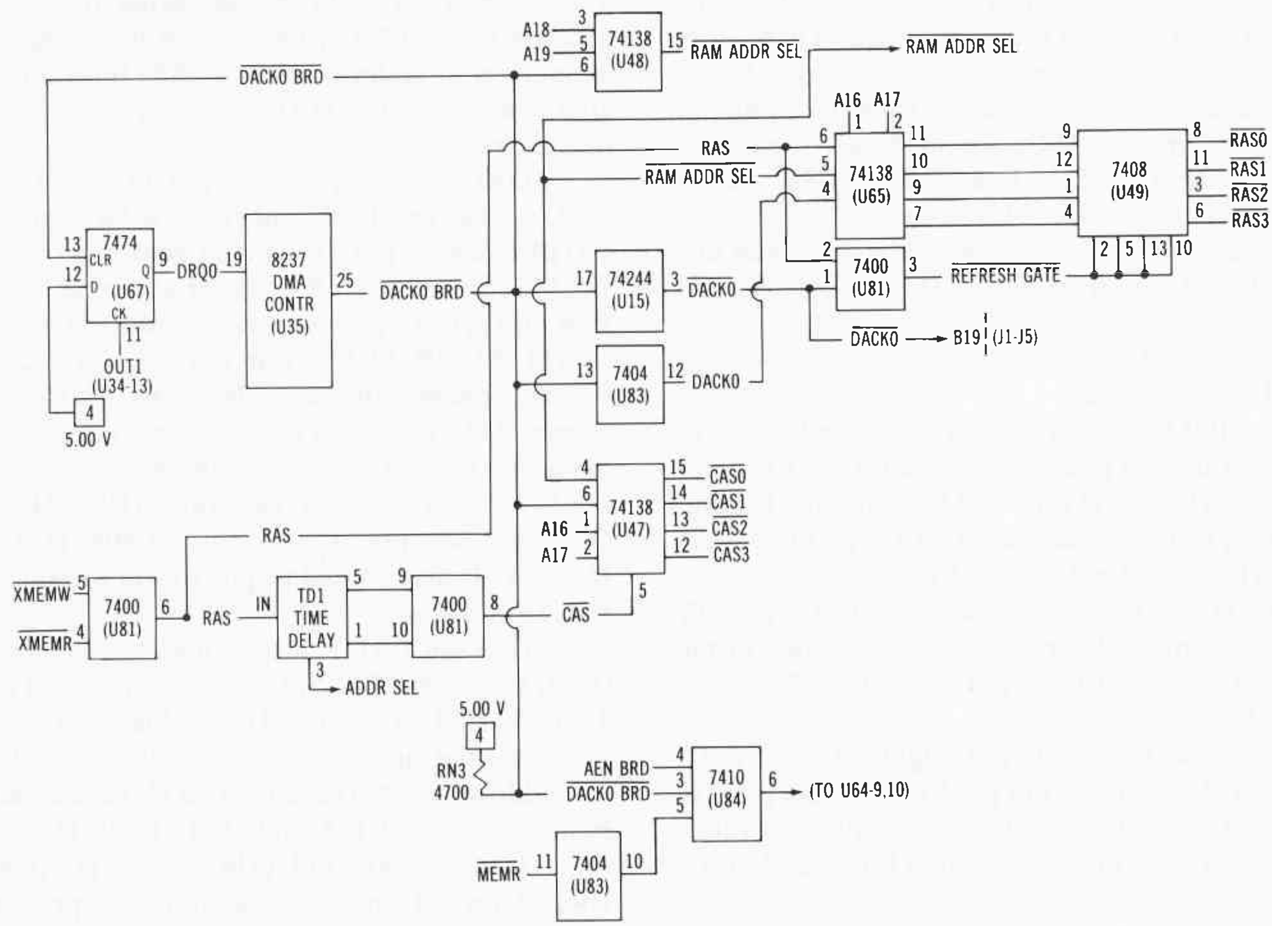


Fig. 2-22. 8237 DRQ0 DMA acknowledge circuitry.

register file (U19). Because DMAC U35 can only handle one 64K memory page at a time, U19 is used as a DMA page register file to increase the DMA capability from 64K to a full one megabyte while retaining the 64K page boundary. U19 is a 16-bit tristate register file organized as four words of 4 bits each. Each word represents a 64K page boundary.

Separate read and write address and enable inputs are available permitting simultaneous reading from one location and writing to another location inside U19. The 4-bit word to be stored is placed on XD0 through XD3 (pins 1, 2, 3, and 15). Write address inputs XA0 and XA1 (pins 13 and 14) determine the location of the stored word. When (WRT DMA PG REG)* on pin 12 goes active low, XD0 through XD3 enter and are latched inside the appropriate word location. This location is transparent to the data while (WRT DMA PG REG)* is low. Data on XD0 through XD3 will be read out in the same logic level as input when the register files are read. The data and write address inputs are inhibited when (WRT DMA PG REG)* is high.

The 64K memory page boundary data that was stored inside U19 is made available on output pins 6, 7, 9, and 10 (A16 through A19) whenever (DMA AEN)* goes active low on input pin 11. This causes the condition of DACK2* and DACK3* to represent an address to one of the four word locations inside U19 copying the data word out as A16 through A19. When (DMA AEN)* returns high, pins 6, 7, 9, and 10 go tristate high impedance. This permits the same address bus segment to use A16 through A19 from the CPU addressing bus circuitry.

Once a DMA request occurs, the DMA active cycle begins. Typically, an active cycle

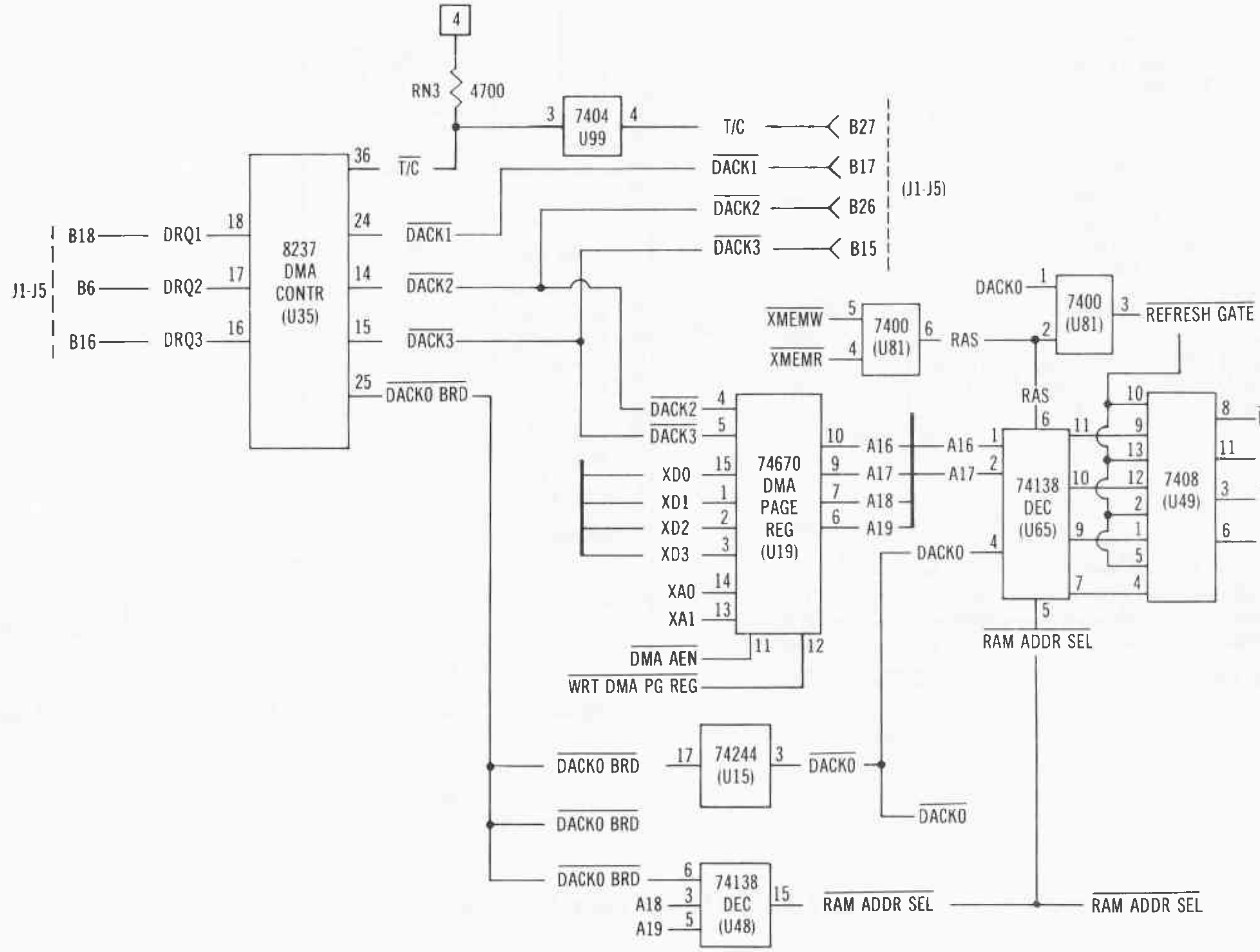


Fig. 2-23. DMA acknowledge circuitry.

requires only five 210 nanosecond clock periods (DMA states), or about 1 microsecond (1.05 μs) of CPU time. This compares quite favorably with the 6 microsecond, 29 clock period typical data transfer time for a CPU memory to memory operation. The memory refresh dummy DMA transfer takes four clocks or 840 nanoseconds.

Figure 2-24 is a snapshot of most of the DMA circuitry. During DMA data transfers, the I/O and memory signals on the lower left are used to control the DMA data direction. If the transfer is from I/O to memory, MEMW*, IOR*, and DACK1*, DACK2*, or DACK3* all go active low. As shown in the lower left of Fig. 2-24, IOR*, IOW*, MEMR* and MEMW* connect to transceiver 74LS245 (U14) to produce XIOR*, XIOW*, XMEMR*, and XMEMW* that connect to 8237 DMAC (U35) on pins 1, 2, 3, and 4. XMEMR* and XMEMW* enter pins 4 and 5 of 74LS00 (U81) and combine to produce the row address strobe (RAS) signal out pin 6 (see Fig. 2-23). To prevent the 8088 CPU buffers (U7, U9, and U10) and the data bus transceiver (U13) from placing addresses and data on the system buses during DMA transfer, the AEN BRD signal from U98 (Fig. 2-21) goes high disabling the outputs of these ICs. (DMA AEN)* from pin 1 of 74LS02 NOR (U50) shown in the lower right of Fig. 2-21 and CF page 57 is brought active low enabling the DMA buffers and latches, and DMA page register permitting high speed data transfers.

From the lower right of Fig. 2-19, you will notice that the 8237 data bus is bidirectional (XD0 through XD7). This data path is multiplexed with the high address byte (A8 through A15) using 74LS373 latch buffer (U18). The XD0 through XD7 output from U35 is

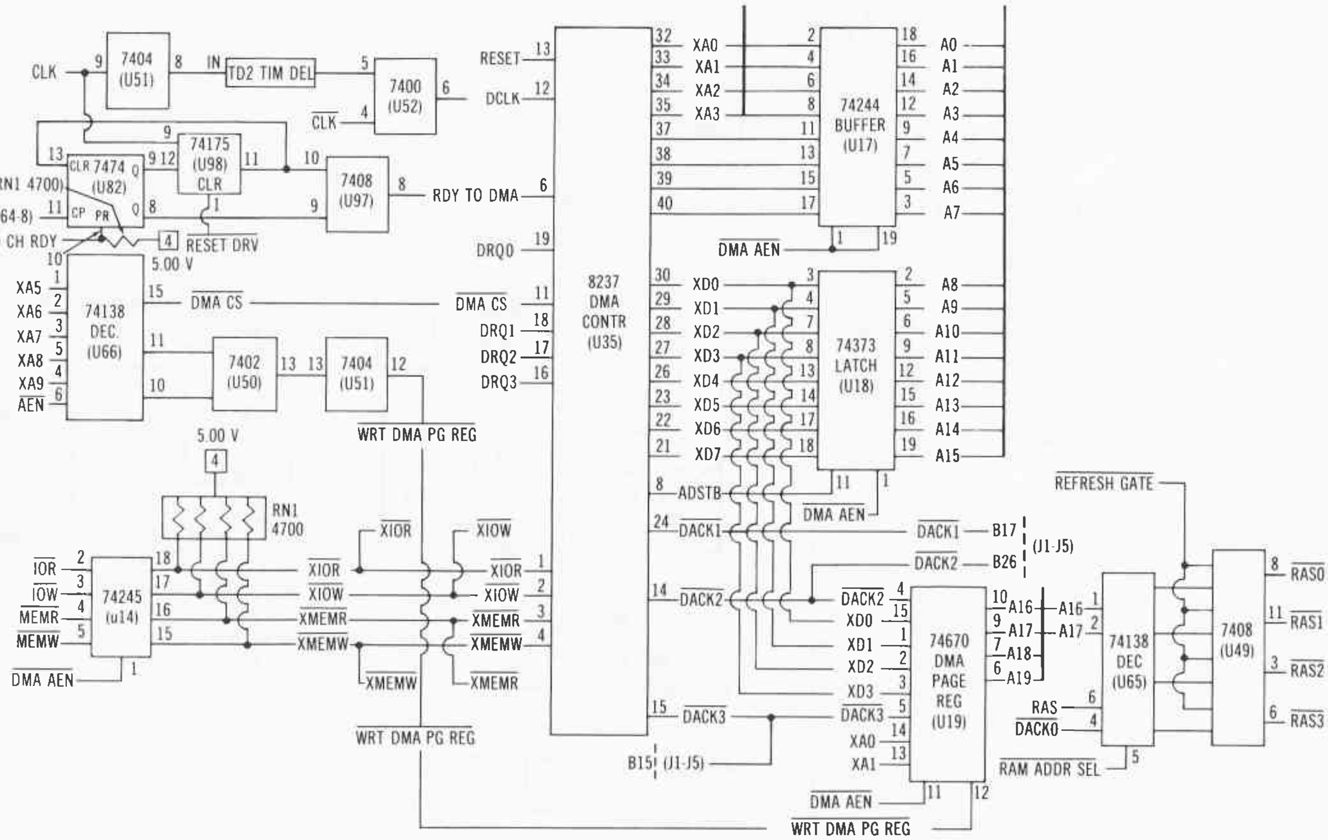


Fig. 2-24. 8237 DMA controller circuitry.

latched in U18 by the address strobe signal (ADSTB) out pin 8 of U35 into enable input (pin 11) of U18. In addition, the normally input lines XIOR*, XIOW* and XA0 through XA3 are actually bidirectional and become output lines during a DMA transfer.

During an active DMA cycle, if more time is required (accessing a slow memory or I/O device), a ready signal (RDY TO DMA) is input to U35 by 74S08 NAND U97 pin 8 inserting wait states in the DMA cycle as shown in Fig. 2-25.

Logic high inputs from inactive (DACK0 BRD)*, XMEMR output of 74LS04 (U83), and AEN BRD enter 74LS10 three-input NAND (U84) produce two inputs to 74LS20 four-input NAND (U64). The other two inputs to U64 are XIOR* and XIOW* on pins 13 and 12 respectively. The pin 8 output from U64 enters the clock input (pin 11) of 74LS74 dual-D latch (U82) latching the condition of I/O CH RDY from expansion connections A10 of J1 through J5 into U82. The Q output from U82 (pin 9) is labelled RDY*/WAIT. This signal is clocked into the D input (pin 12) of 74LS175 quad-D latch (U98) by the CLK signal on U98 pin 9. It is also passed to pin 3 of 8284 clock generator U11 where it is combined with (DMA WAIT)* and used to control the READY signal out pin 5 of U11.

Terminal Count (T/C)

Each time the 8237 DMA internal word count circuitry reaches a count of FFFFH a terminal count signal is generated causing U35 pin 36 to go active low. As shown in Fig. 2-26, the (T/C)* signal out pin 36 is passed through 74LS04 Hex inverter (U99) to produce an active high T/C output signal to pin B27 of the expansion connections J1 through J5. Signal T/C is used to indicate completion of a DMA operation.

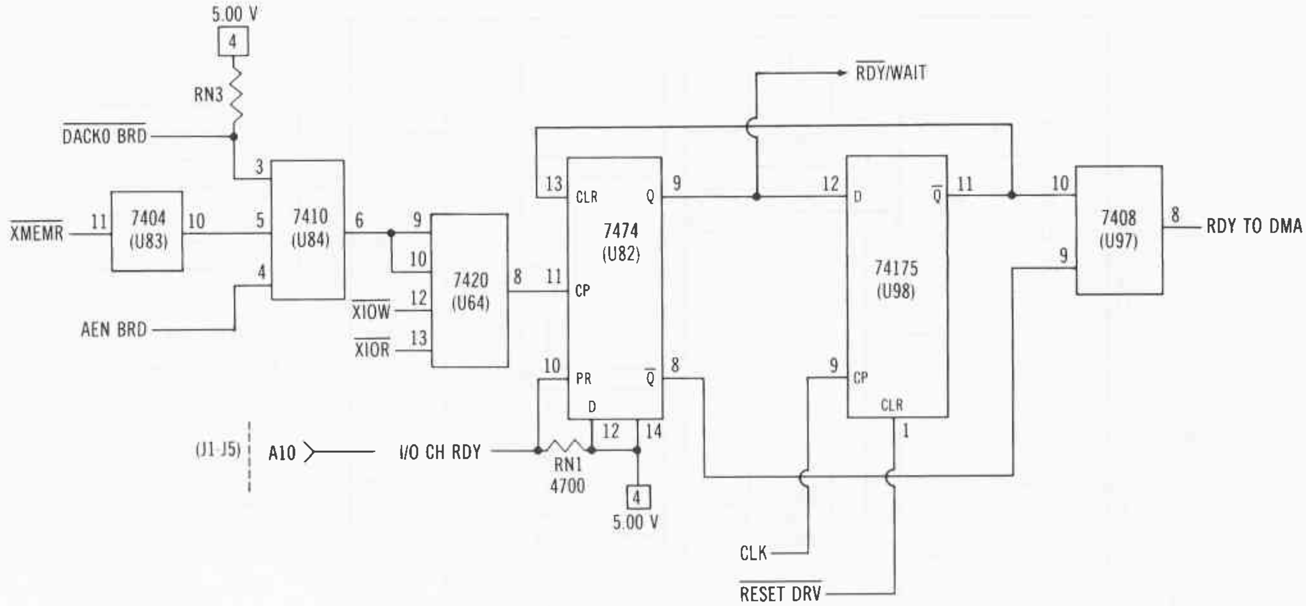


Fig. 2-25. RDY TO DMA circuitry.

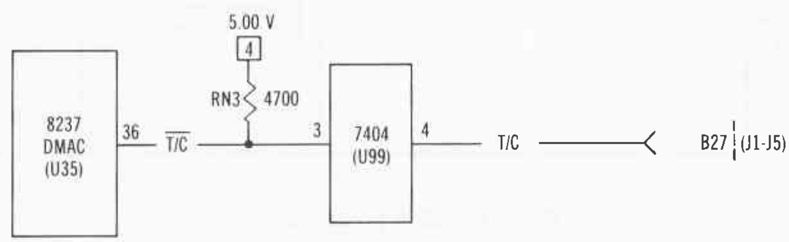


Fig. 2-26. Terminal count circuitry.

T/C should not be confused with the timer controller chip select (T/C CS)* signal out pin 13 of 74LS138 decoder (U66) to the input chip select (pin 21) of 8253 Programmable Interval Timer (U34) shown in Fig. 2-18.

8255 PROGRAMMABLE PERIPHERAL INTERFACE (U36)

One of the most important interconnects on the IBM PC system board is a 40-pin IC called the 8255 programmable peripheral interface (U36). U36 is used to interface peripheral equipment to the 8088 system bus. Figure 2-27 shows that U36 interfaces a bidirectional data bus with three programmable I/O ports under control of specialized read/write control logic. Figure 2-27 is drawn as U36 is configured in your IBM PC.

The functional configuration of U36 is programmed during initialization. The tristate bidirectional buffered data bus XD0 through XD7 connects with U36 on pins 27 through 34. Data is transferred by the buffer under CPU control. PPI control words and status information are also passed back and forth through this data bus buffer.

The read/write control logic accepts six input control signals that manage the operation of this device. An active low XIOR* on pin 5 enables U36 to send data or status information to the CPU (U3) over the data bus. It lets U3 read from U36. An active low XIOW* on pin 36 enables the CPU to write data or control words into U36. XA0 and XA1 on pins 9 and 8 respectively are used with XIOR* and XIOW* to select one of the three I/O ports or internal word control registers. Typically, these four signals are

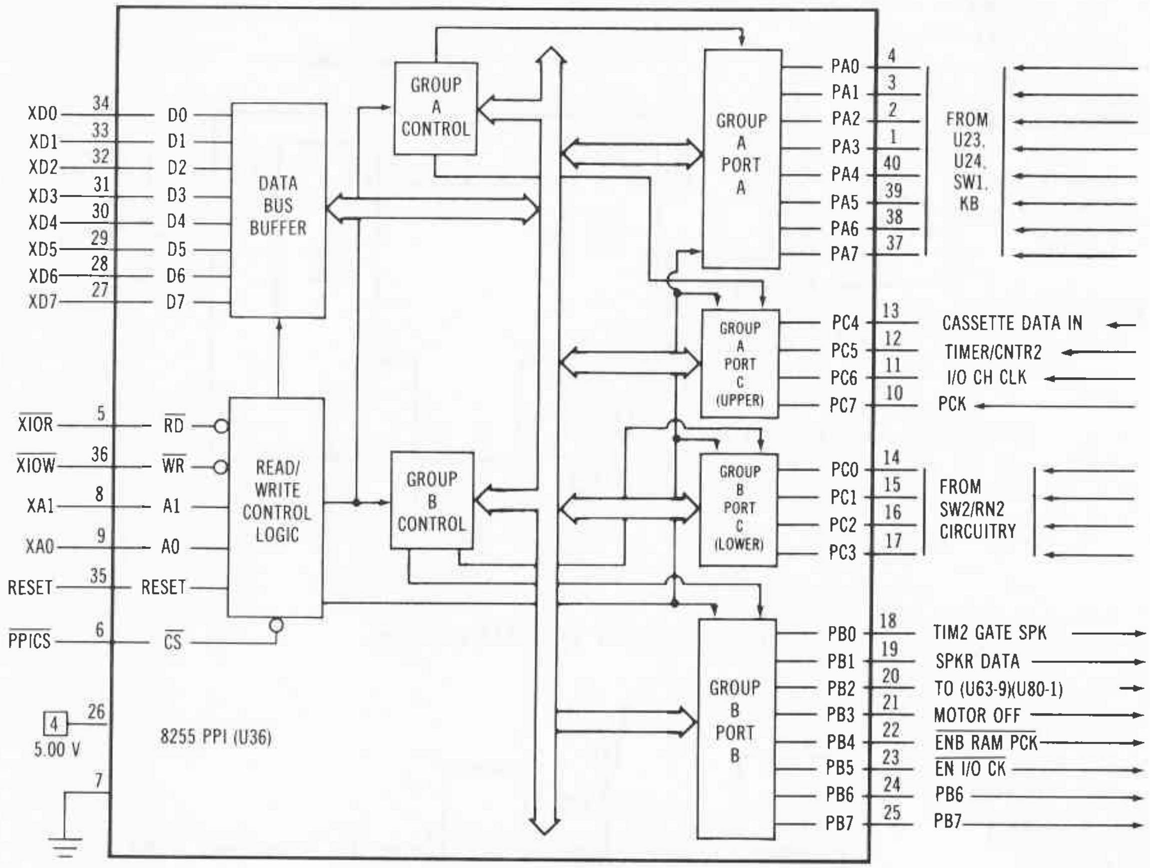


Fig. 2-27. 8255 programmable peripheral interface.

used to cause port A or port C to write to the data bus, and the data bus to pass information out port B. An active high on RESET input pin 35 clears the control register and sets all ports to the input mode. This prevents input circuitry to ports A and C from being damaged if one of these input ports become an output port after initialization. Finally, the active low programmable peripheral interface chip select (PPICS)* signal on pin 6 is used to enable communication between U36 and the CPU (U3).

The Group A and B control blocks accept commands from the read/write control logic, and control words from the data bus buffer to generate proper configuration commands to the I/O ports. Group A controls port A and the upper nibble of port C. Group B controls port B and the lower nibble of port C.

The three 8-bit I/O ports (A, B, and C) can be configured in a wide variety of functional ways, but are configured by design and software to be specific input or output. The port configuration is determined by a control word copied into U36 via the data bus. This control byte (10011001) configures ports A and C as inputs and port B as an output. This basic input/output configuration requires no handshaking for information transfer. Once configuration is complete, a control input to the read/write control logic causes U36 to operate according to an input code on pins 5, 8, 9, and 36 (XIOR*, XA1, XA0, and XIOW*). The chip control signal configuration for operation of each port is shown in Table 2-3.

U36 operates asynchronously. Once the correct code is present and the chip is selected (pin 6), the data transfer direction is predetermined. Figure 2-28 shows that port A is connected to the 74LS322 keyboard bidirectional register (U24) and the 74LS244 buffer (U23).

Table 2-3. Control Logic Input Configuration for Port Operation

A1	A0	XIOR*	XIOW*	FUNCTION
0	0	0	0	Port A to data bus
1	0	0	1	Port C to data bus
0	1	1	0	Data bus to port B
1	1	1	0	Data bus to control logic
X	X	1	1	Data bus to tristate
X	X	X	X	Data bus to tristate

Depending on the status of output port B bit 7 (PB7), port A reads the keyboard or the system board switch (SW1). PB7 high causes port A to read the keyboard input byte. PB7 low causes port A to read the system board DIP switch (SW1).

Port C receives inputs from an attached cassette peripheral, the 8253 programmable interval timer (U34) counter 2 output, the status of the I/O channel, the status of RAM parity checking, and the number of RAM banks in the I/O channel as determined by the position of the memory configuration switch (SW2). This lets the PC recognize up to eight 64K byte memory banks in the I/O channel.

Port B outputs information to the speaker, to the timer (U34), to the cassette motor, and to the parity test circuitry. When PB0 is high, coun-

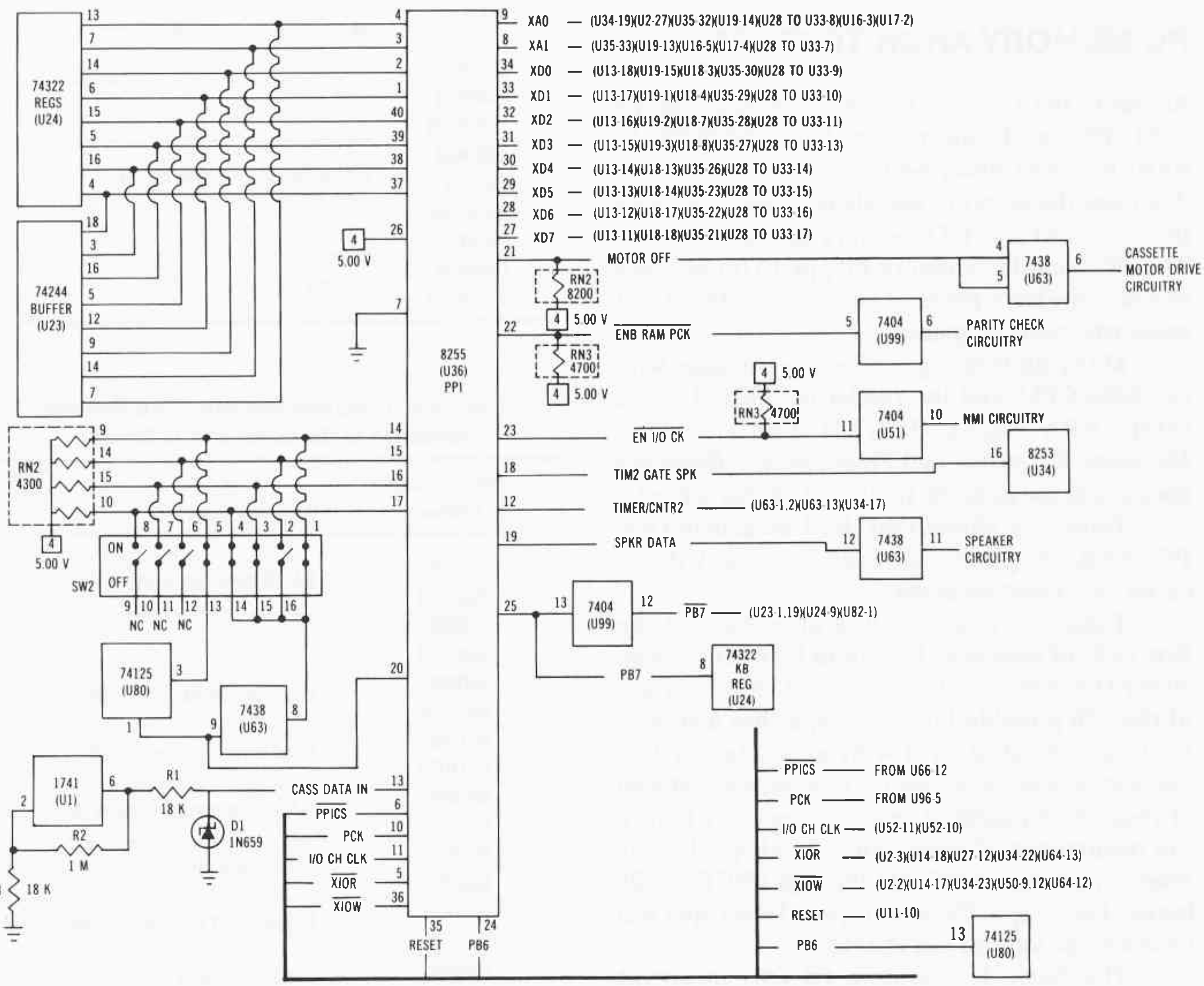


Fig. 2-28. Circuitry associated with 8255 PPI U36.

ter timer 2 in U34 generates a square wave for the speaker and cassette outputs. PB1 is used to send programmed data waveforms to the speaker. PB2 high is passed to 74LS125 quad tristate buffer (U80) and 74LS38 quad two-input NAND (U63) to enable the low nibble of the system board switch SW2 (see Fig. 2-28). When PB3 goes high, the cassette motor is turned off. If PB4 and PB5 are low, RAM parity and the I/O channel status lines read by port C are enabled. Port B PB6 is used to drive the keyboard clock line low (PB6 = 0), and PB7 is used to cause port A to read SW1 (PB7 = 1) or the keyboard data (PB7 = 0).

PC MEMORY ARCHITECTURE

Access to the 1 million byte memory space of the IBM PC, with addresses from 00000H to FFFFFH, was described earlier. This section describes the circuitry and signals associated with the on-board and I/O memory in your machine. The PC includes memory-mapped I/O because devices can have physical addresses within the 1 megabyte memory space.

Many addressing modes are possible with the 8088 CPU, and the reader is referred to the Intel iAPX 86/88, 186/188 *User's Manual Hardware Reference* and *Programmer's Reference* documents for in-depth treatment of this subject.

Table 2-4 shows that the 1 megabyte IBM PC memory space is divided into many dedicated and reserved areas.

Table 2-5 describes the allocation of the first 64K of memory. Locations 00000H through 003FFH are reserved for interrupt vectors. Each of the 256 possible interrupt types has a service routine indicated by a 4-byte pointer in this memory space. The pointer elements are stored at respective places in reserved memory before the occurrence of interrupts. Intel specifically reserves addresses 00000H through 0007FH (128 bytes) for 32 specific interrupts. Interrupts will be discussed later in this chapter.

The basic I/O system (BIOS) interrupt vectors 00 through 1F are contained in addresses

Table 2-4. Memory Allocation for the IBM PC

Hexadecimal Address	16K/64K System	64K/256K System
00000H 0FFFFH	64K RAM on system board	256K RAM on system board
10000H 3FFFFH	576K RAM on expansion cards	
40000H 9FFFFH		384K RAM on expansion cards
A0000H AFFFFH	(A0000H - BFFFFH = 128K reserved for displays)	
B0000H B3FFFH	Monochrome video RAM	
B4000H B7FFFH		
B8000H BBFFFH	Color/graphics video RAM	
BC000H BFFFFH		
C0000H FFFFFH	ROM	

Table 2-5. (16K/64K and 64K/256K Systems) Allocation of the Lower 64K of Memory

Hexadecimal Address	Memory Content
00000H 0001FH	BIOS interrupt vectors 00-1F
00020H 0007FH	
00080H 0009FH	DOS interrupt vectors 20-3F
00100H 001FFH	User interrupt vectors 40-7F
00200H 003FFH	BASIC interrupt vectors 80-FF
00400H 004FFH	BIOS data area
00500H 005FFH	BASIC and DOS data area
00600H 0FFFFH	63.5K user area

00000H through 0001FH. The next set of vectors (DOS interrupt vectors 20 through 3F) are located between 00080H and 0009FH. USER interrupt vectors 40 through 7F reside in locations 00100H through 001FFH. Locations 00200H through 003FFH contain BASIC interrupt vectors 80 through FF. Special BIOS data is stored between 00400H and 004FFH. Then BASIC and DOS data are stored between 00500H and 005FFH. From location 00600H to 0FFFFH is 63.5K of user defined RAM memory space.

Read-only memory (ROM) is designed to reside in the address space bounded by C0000H and FFFFFH. The allocation of these 262,144 locations (256K memory space) in both the 16K/64K and 64K/256K PC systems is shown in Table 2-6.

Table 2-6. ROM Memory Space Allocation

Hexadecimal Address	System Board Chip	16K/64K Systems	64K/256K Systems
C0000H C7FFFH	-	(32K)	192K ROM for system expansion and control
C8000H CBFFFH	-	(16K) Hard disk control	
CC000H EFFFFH	-	(144K)	
F0000H F3FFFH	-	(16K)	
F4000H F5FFFH	U28	(8K)	open ROM socket
F6000H F7FFFH	U29	(8K)	32 ROM CASSETTE BASIC
F8000H F9FFFH	U30	(8K)	
FA000H FBFFFH	U31	(8K)	
FC000H FDFFFH	U32	(8K)	
FE000H FFFFFH	U33	(8K)	ROM BIOS

Memory locations FFFF0H through FFFFFH (16 bytes) are reserved for specific 8088 CPU operations including a jump to the initial program loading routine. When a RESET occurs, the CPU always begins executions at system reset location FFFF0H where a jump instruction must be stored shifting program execution to a special routine.

The I/O space in the IBM PC is separate from the memory space, although I/O devices can also be configured to be addressable within the memory space (memory mapped I/O). The I/O memory space accessible by the 8088 CPU covers addresses 0000H to FFFFH (64K bytes). The allocation of I/O memory is shown in Table 2-7.

Table 2-7. IBM PC I/O Address Map

Hexadecimal Address	Access Function
000-00F	8237 DMA controller (U35)
020-021	8259 programmable interrupt controller (U2)
040-043	8253 programmable interval timer (U34)
060-063	8255 programmable peripheral interface (U36)
080-083	DMA page registers
0A	NMI mask register enable/disable
0C	Reserved
0E	Reserved
0F8-0FF	Reserved for 8088 upgrades
100-1FF	Not usable
200-20F	Game control
210-217	Expansion unit
220-24F	Reserved
278-27F	Reserved
2F0-2F7	Reserved
2F8-2FF	Asynchronous communications (secondary)
300-31F	Prototype card
320-32F	Hard disk
378-37F	Printer
380-38C	Synchronous data link control (SDLC) communications
380-389	Binary synchronous communications (secondary)
3A0-3A9	Binary synchronous communications (primary)
3B0-3BF	IBM monochrome display/printer card
3C0-3CF	Reserved
3D0-3DF	Color/graphics
3E0-3F7	Reserved
3F0-3F7	Diskette
3F8-3FF	Asynchronous communications (primary)

Table 2-7 shows that some of the chips on the system board are directly accessible via an I/O write or read command. Other locations in I/O memory space are reserved by IBM or a chip manufacturer. Intel reserves addresses 000F8H through 000FFH (8 bytes) for future hardware and software products.

The 8088 accesses memory in bytes. Word operands are accessed in two bus cycles. Instructions are also fetched 1 byte at a time.

MEMORY AND I/O ACCESS AND CONTROL SIGNALS

The circuitry that generates the four memory command signals from 8288 bus controller U6 to enable memory read and write operations is shown in Fig. 2-29. Each of the active low signals–memory read (MEMR*), memory write (MEMW*), I/O read (IOR*), and I/O write (IOW*)–originate in the 8288 bus controller (U6). Figure 2-29 shows that these four signals are passed to 74LS245 transceiver (U14) where they become the XMEMR*, XMEMW*, XIOR*, and XIOW* used throughout the system board. They are also passed to pins B11 through B13 on expansion connectors J1 through J5 for use on peripheral boards.

The logic value combination of the CPU status bits S0*, S1*, and S2* forms a code that determines what system operation is to occur. Table 2-8 repeats the Table 2-2 description of the operation that is enabled by each combination of the status code inputs, but includes the pin assignments for each specific memory or I/O command generated.

Therefore, whenever the status bit input into 8288 (U6) in Fig. 2-29 is 001, 010, 101, or 110, an appropriate active low memory or I/O command is generated on pin 7, 8, 12, or 13. These commands are felt on the inputs to 74245 transceiver-buffer (U14) and on pins B11 through B14 of the expansion sockets J1 through J5. On the down side of transceiver U14, the memory and I/O commands assume a new label.

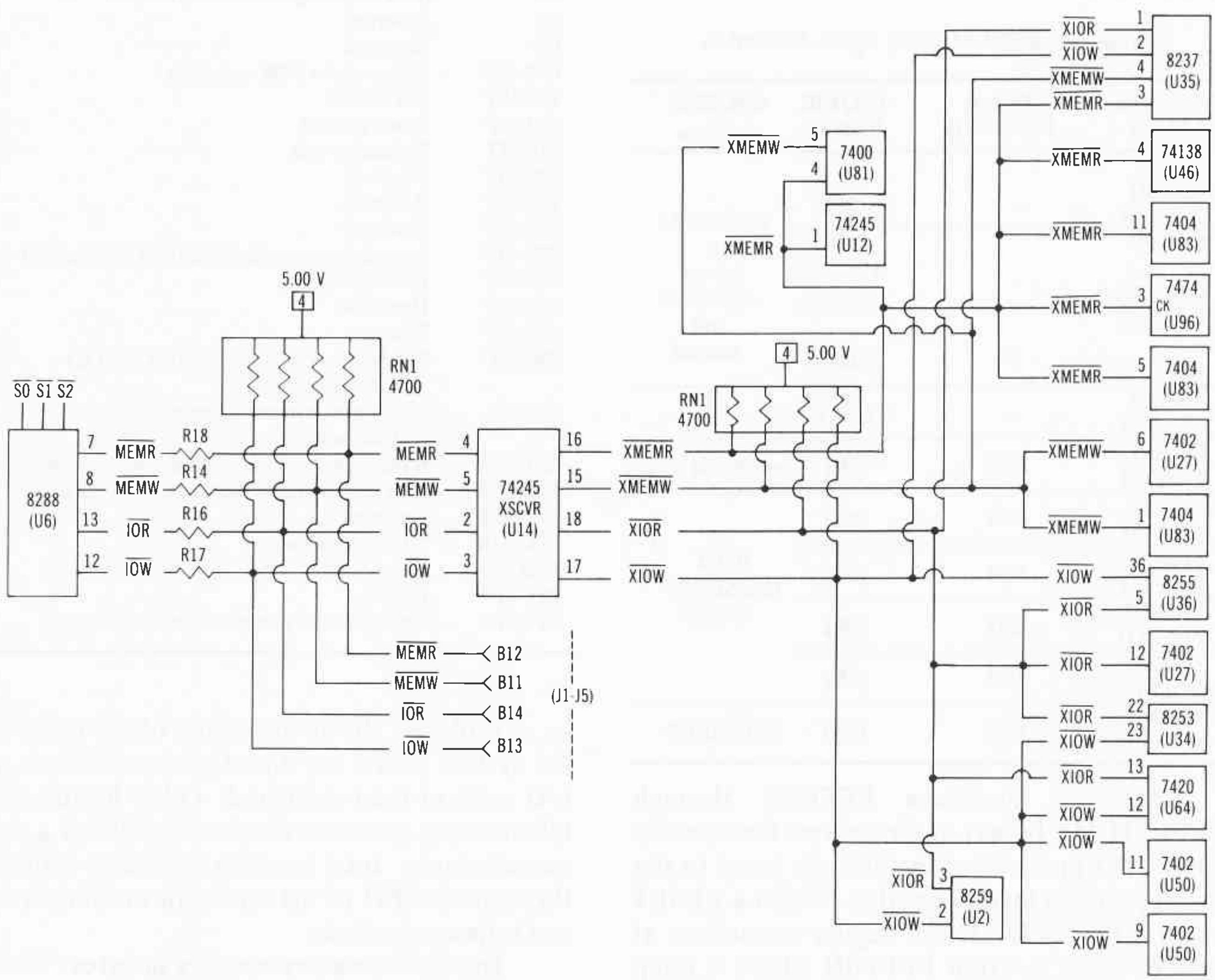


Fig. 2-29. Memory and I/O bus command signals.

Table 2-8. Status Bit Code Allocations

Status Bits S2*	S1*	SO*	Processor State	8288	Command Pin #
0	0	0	Interrupt acknowledge	INTA*	Pin 14
0	0	1	Read I/O port	IOR*	Pin 13
0	1	0	Write I/O port	IOW*	Pin 12
0	1	1	Halt	None	
1	0	0	Code access	MEMR*	Pin 7
1	0	1	Read memory	MEMR*	Pin 7
1	1	0	Write memory	MEMW*	Pin 8
1	1	1	Passive	None	

Memory read (MEMR*) becomes active low buffered memory read (XMEMR*). Memory write (MEMW*) becomes active low buffered memory write (XMEMW*). I/O read (IOR*) becomes active low buffered I/O read (XIOR*). And I/O write (IOW*) becomes active low buffered I/O Write (XIOW*). These signals are passed throughout the system board, as shown in Fig. 2-29. They are typically connected as enable inputs to gates used in memory or I/O operations. In the figures to follow in this section, you will note one or more of these signals used in every memory or I/O operation.

READ ONLY MEMORY (ROM)

The system board in every PC is designed to hold six 8K x 8-bit ROM chips–only five are installed. Figure 2-30 shows the pinout allocation for the 2364 ROM chips installed in your system board. Twelve address lines connect to each chip. A special chip select signal on pin 20 enables that particular ROM so 8 bits of data can be placed on the output pins 9 through 11, and pins 13 through 17.

Of the assigned ROM memory space (C0000H to FFFFFH), locations C0000H to F3FFFH are reserved for future ROM code. If a hard disk is connected, its allocated address space is from C8000H to CBFFFH. Address space F4000H to F5FFFH was reserved for part of the original cassette BASIC code. These addresses are allocated to the single empty socket (U28). The next four ROM chips (U29

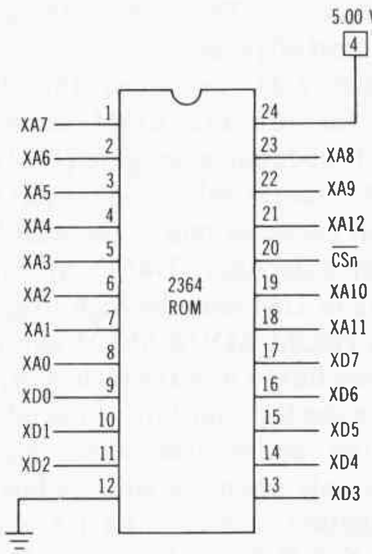


Fig. 2-30. IBM PC ROM chip pin assignment.

through U32), are allocated address space (F6000H through FDFFFH) and contain the 32K cassette BASIC object code. The remaining ROM (U33) has allocated address space FE000H to FFFFFH and contains the PC's basic input/output system (BIOS) routines.

Permanently stored in the 8K ROM BIOS chip (U33) are program codes called "I/O drivers" that enable printer operations and dot patterns for 128 characters to enable graphics display operations. Inside U33 there is also code to control the time of day clock, cassette operations, the power-up self test, and minifloppy disk bootstrap loading. All address locations below C0000H are dedicated for I/O and random access memory (RAM).

The internal ROM-based PC power-up self test occupies 2K of the 8K BIOS ROM and includes a series of 14 tests that occur each time power is applied. These tests check the 8088 CPU (U3), the keyboard, the video display adapter card, the cassette recorder, the floppy disk interface, and the ROM and RAM. The RAM test contains five different write/read operations over the entire RAM memory. Each memory test writes and then reads and checks a different bit pattern in memory. The RAM tests can take as long as 1.5 minutes if your system board is fully populated. The power-up self tests are bypassed if the computer is restarted with power already on. This reduces the initialization time by almost 40 percent.

Figure 2-31 describes the chip select circuitry for the PC ROM memory. The 74LS20N four-input NAND gate (U64) generates the ROM address select signal (ROM ADDR SEL)* that becomes one of the enable inputs to 74138 1-of-8 decoder (U46). All four address line inputs to U64 must be high to generate the active low (ROM ADDR SEL)* output on pin 6. The address lines (A16 through A19) connected to U64 are the top four bits of the address word, causing the active low select signal to be generated only when the address bus contains a bit combination such as: 1 1 1 1 X X X X X X X X X X X X X X X X, placing the ROM enable signal at F0000H or higher.

Decoder U46 has two more enable signals attached: XMEMR* from the circuitry in Fig. 2-29 and (RESET DRV)* from the circuitry in Fig. 2-7. The latter signal is attached to an active high enable input pin, so only when (RESET DRV)* is high will this combination of enables cause U46 to produce an output determined by the address inputs (A13 through A15) on pins 1 through 3. Once enabled, U46 will produce a low on an output line determined by the code on input pins 1 through 3.

Notice that not all outputs are used on U46. The pins 14 and 15 outputs are unused. This means that one of the remaining six outputs (CS2* through CS7*) will become active low whenever A13 through A15 is a combination of 010 to 111. Connecting this combination to our input combination to U64, we discover that a ROM chip will be selected (given the correct enable inputs to the select circuitry) whenever the address bus code is 1 1 1 1 0 1 0 X X X X X X X X X X X X X or an address of F4000H or higher. This correlates nicely with the F4000H lowest address allocated to the empty ROM socket U28.

The CS7* line goes active low whenever A13 through A15 are all high. This equates to an address code of F E X X X H or higher. CS7* enables ROM U33, whose address space is FE000H to FFFFFH. In all ROM enables, the particular ROM that is selected places an 8-bit

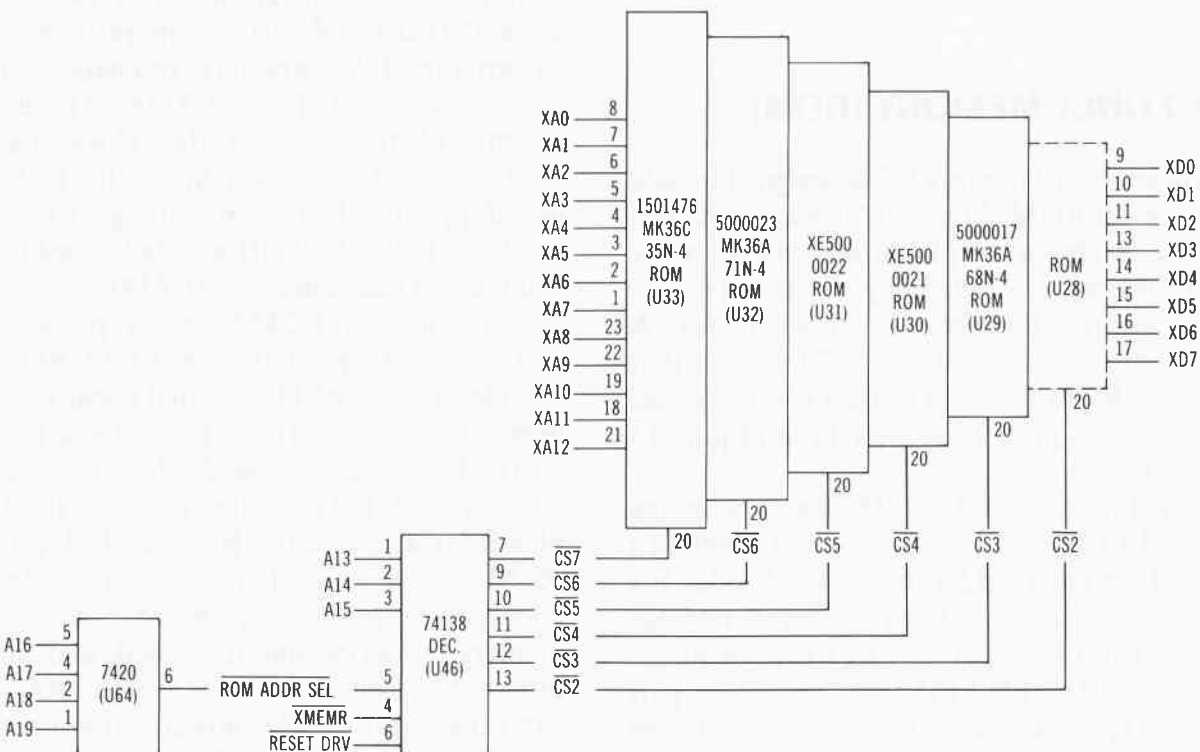


Fig. 2-31. ROM select circuitry.

data word out pins 9 through 17 (XD0 through XD7) determined by the combination of the remaining 12 address bits (XA0 through XA12) on the input (left) side of the memory array in Fig. 2-31.

Figure 2-32 is an example showing the logic levels on the inputs and outputs of the ROM memory circuitry when the address location FE000H is placed on the address bus. This equates to the first address in BIOS ROM U33.

The first 13 address bits are buffered through two 74LS244 buffer chips (U16 and U15) to produce buffered address bits XA0 through XA12. The top 7 bits of the address bus (A13 through A19) are used to generate the appropriate active low chip select signal (in this case CS7*). With the address bus combination shown in the figure, the data stored in location FE000H in U33 is placed on the buffered data bus (XD0 through XD7) between 27 to 39 nanoseconds after CS7* goes low. Access time for ROM is 250 nanoseconds. A memory cycle time is 375 nanoseconds.

The buffered data out of the ROM passes through 74LS245 transceiver U13 to become the data bus (D0 through D7) input for 8088 CPU U3. Figure 2-33 shows how data from a ROM reaches the CPU. When a location is addressed and chip select becomes active low, 8 bits of data become valid on ROM output lines XD0 through XD7 (pins 9 through 11, and 13 through 17). This data is felt on pins 11 through 18 of 74LS245 transceiver U13. Direction signal DIR and enable signal AEN BRD are both low causing

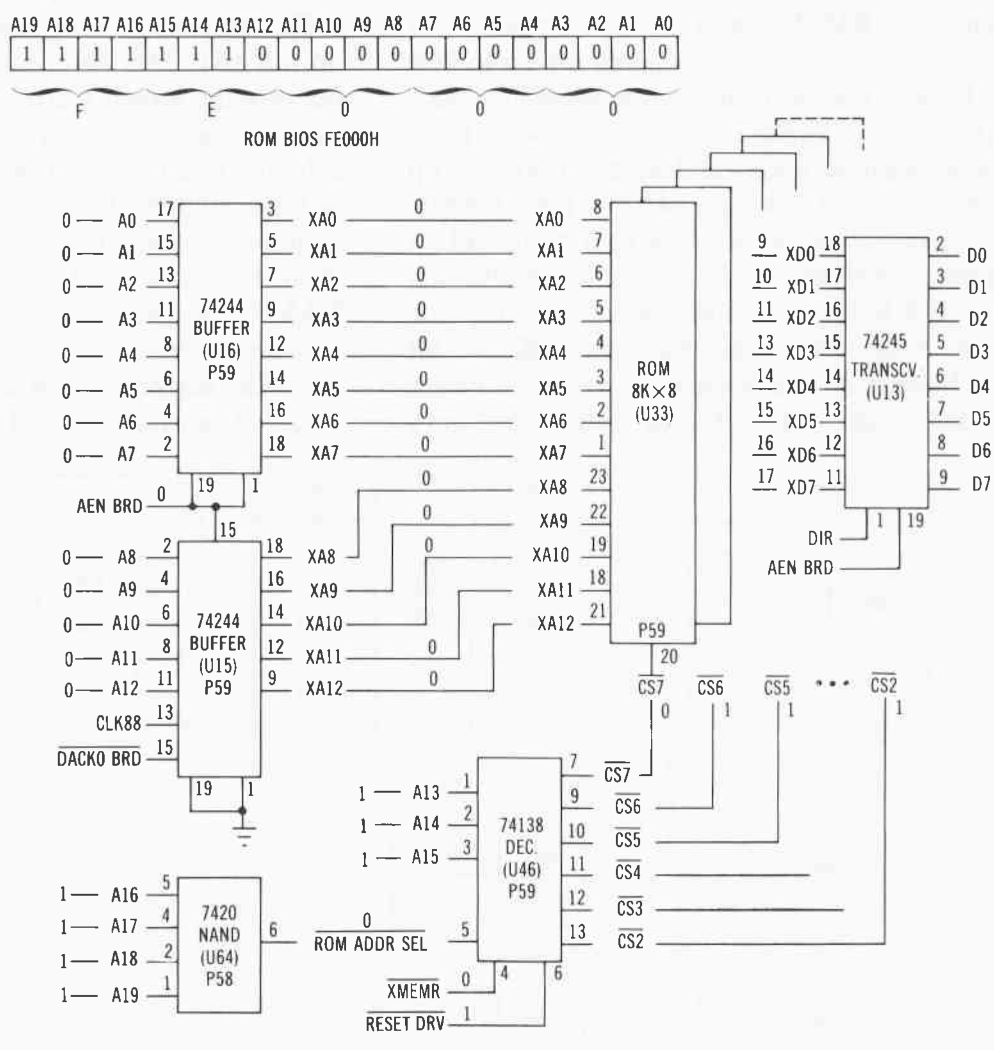


Fig. 2-32. ROM memory circuitry. Accessing the first location in BIOS ROM (U33).

U13 to pass data from the buffered data side (XD0 through XD7) to the data bus side (D0 through D7) on pins 2 through 9.

The output of U13 is passed into 74LS245 transceiver U8 on pins 11 through 18. Data transmit/receive signal DT/R* is active low (the receive condition) as is enable signal G*. This causes U8 to pass data in from pins 11 through 18 and out pins 2 through 9. The output of U8 is the address data bus (AD0 through AD7) which connects directly into 8088 CPU U3 on pins 9 through 16. In this manner, data from any ROM chip can be read into the CPU for action.

RANDOM ACCESS MEMORY (RAM)

When the IBM PC was first introduced, it contained system boards designed for up to 64K of 4116-type 16K by 1-bit random access memory (RAM) chips. These system boards were later replaced with an updated design containing up to 256K of the 4164-type 64K-by-1-bit RAMs. The expansion slots enable a user to install an additional 384K bytes of external RAM allowing up to 640K bytes of available RAM memory in a system. Most users today have the 64K-by-1-bit RAM boards, so this book focuses on the newer system boards. Older board designs are very similar to the system boards described in this book, so you should not have any difficulty following this text and relating the information to your system.

The RAM chips on the system board are mounted in four rows, or banks, of nine chips each. The ninth chip is used to store a parity bit associated with each 8-bit word in that row of RAM. All of the RAM is parity checked during readout. This operation will be described later.

Figure 2-34 describes the pin assignments for a typical MK4564 64K-by-1-bit RAM chip. The RAM access time is 250 nanoseconds, and a memory cycle time is about 410 nanoseconds.

Figure 2-35 is a block diagram of the inside of a 64K-by-1-bit RAM chip. Note that each chip has only eight address lines (MA0 through MA7) connected to it, with a single data input pin (MDn on pin 2), and a single data out line (MDn on pin 14). Only eight address lines are used because the memory array is comprised of 65,536 dynamic memory cells accessed by row and by column. In a memory operation, the row address is entered into the chip first, followed by a column address. Three active low control signal input lines are used to select and enable each RAM chip: row address select (RAS*), column address select (CAS*), and write enable (WE*).

The active low row address strobe (RASn*) on pin 4 is used to begin a memory cycle. The

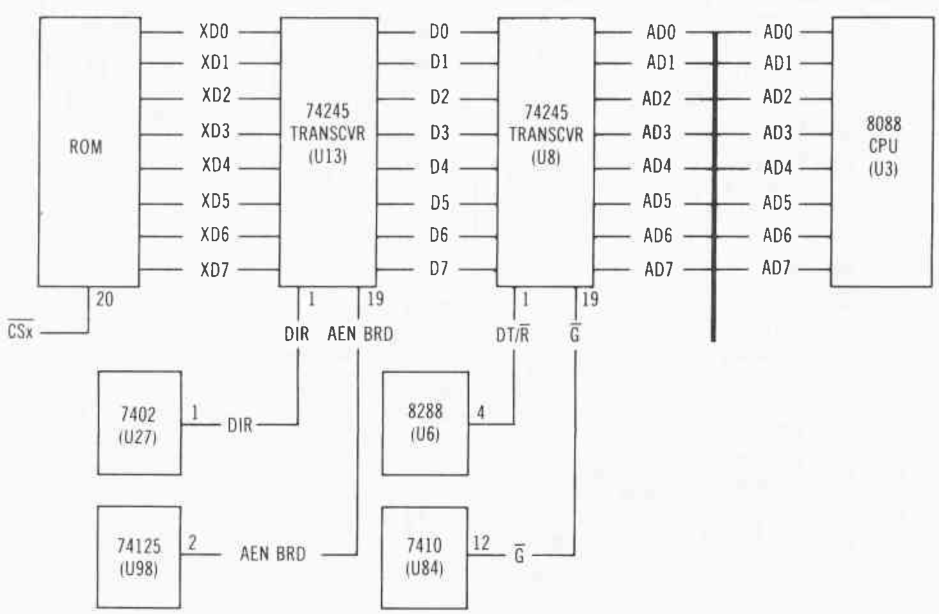


Fig. 2-33. Data transfer from ROM to CPU.

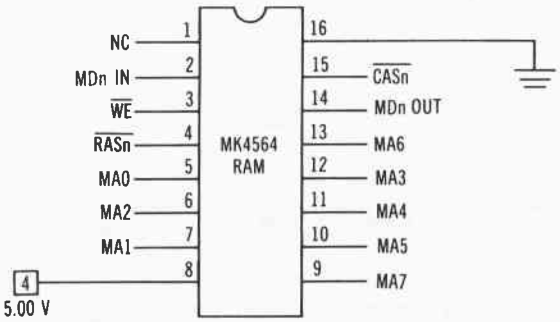


Fig. 2-34. IBM PC RAM chip pin assignments.

"n" suffix identifies a particular bit in a word. For example, RAS5* refers to bit 5 in an 8-bit byte. RASn* allows the row address bits to enter and be latched in the row address buffer and enables the activation of the memory row indicated by the address input. RAS* is also held low while strobing each of the row addresses in a row refresh operation.

The active low column address strobe (CASn*) on pin 15 is used to latch eight column address bits into the column address buffer. It also activates the column in the memory array decoded by the input memory address bits.

The active low write enable (WE*) on pin 3 is used to put the chip into a write or read mode. When WE* is high, the read mode is selected. An active low WE* input causes the chip to enter the write mode.

RAM MEMORY OPERATION

Approximately 500 microseconds after power is first applied to the system, and after RAS* has been held high for about 100 microseconds, the RAM circuitry is initialized by a software routine that does eight RAS* cycles. This initializes the dynamic RAM for the next memory activity.

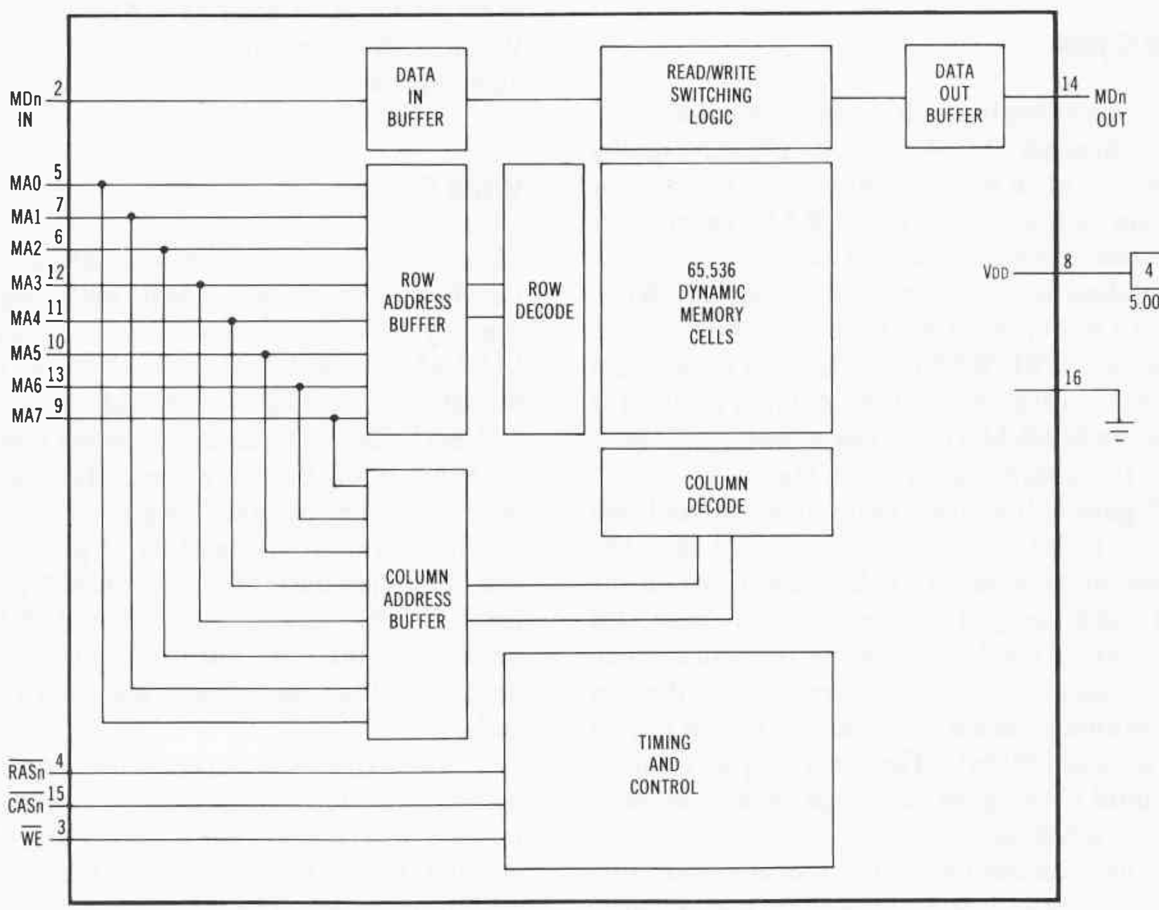


Fig. 2-35. Block diagram of 64K dynamic RAM.

Sixteen address bits are needed to decode one of 65,536 storage cell locations in a single RAM chip. Because each chip has only 8 address bit inputs, the 16 addresses needed to access each memory cell are multiplexed into the chip, row address first, followed by a column address. The signals that latch each part of the address into the chip are RAS* and CAS*. Eight row address bits are placed on the input address (MA0 through MA7) and latched into the chip with RAS*. Next eight column address bits are placed on the input address (MA0 through MA7) and latched into the column address buffer by CAS*. In each case, the addresses on the input must be stable on or before the falling edge of active low RAS* and CAS*. The RAS* command is much like a chip enable because it affects both the row decoder and the sense amplifiers. CAS* acts like a chip select because it activates the column decoder and both input and output buffers.

Read Cycle

A read cycle begins with a valid row address on MA0 through MA7 and a negative-going transition of RAS* as shown by the timing diagram in Fig. 2-36. When RAS* reaches its active low condition, the row address is captured and latched into the row address buffer. Write enable (WE*) must be high to define a read operation. With WE* high, the data input MDn on pin 2 is disabled and the column address is placed on MA0-MA7. A few nanoseconds later (after the column address is stable, or valid), CAS* goes active low. This causes the column address to be captured and latched into the column address buffer. CAS* also turns on the input and output buffers so a data bit representing the logic value in the storage cell location identified by the intersection of the row and column address is copied onto the pin 14 data output (MDn). The data output remains valid until CAS* goes back high causing MDn to return to a high impedance condition.

The data out buffer has tristate capability. It provides output data of the same logic polarity as what was stored via the input. The output of

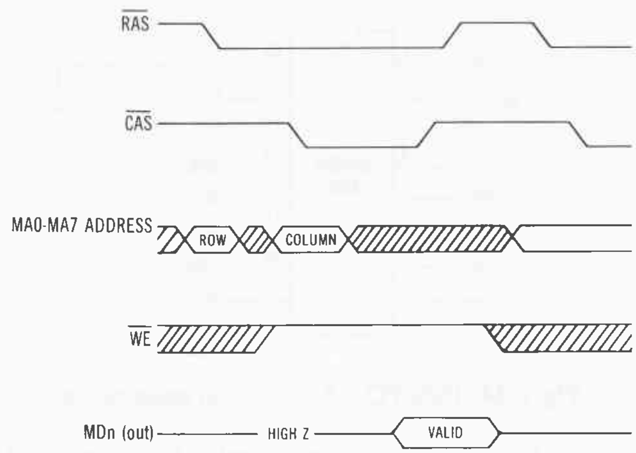


Fig. 2-36. Read cycle timing.

this buffer is a high impedance to the data bus until CAS* is pulled active low. During a read cycle, the output becomes active approximately 135 nanoseconds after the negative transition of CAS*. The output data then becomes valid. It remains valid as long as CAS* is active low. When CAS* goes high, MDn-pin 14 shifts to a high impedance state.

Write Cycle

Figure 2-37 shows the timing relationships for a RAM write operation. A write cycle begins like a read cycle in that a row address is placed on MA0-MA7, held stable, and then RAS* is brought low latching the row address into the row address buffer. The column address now appears on MA0-MA7, but here the difference occurs. WE* no longer remains (or goes) high signifying a read operation. Instead, WE* goes active low just before (or during) the time CAS* goes active low. If WE* goes low before CAS* becomes active low, the data out line (MDn on pin 14) holds in a high impedance state for the entire cycle.

The write cycle can occur in two ways: first, an "early write" occurs as described previously. In this operation, WE* must be valid long enough to be recognized by the read/write switching logic. The second write method is called a "delayed write" or "read-modify-write."

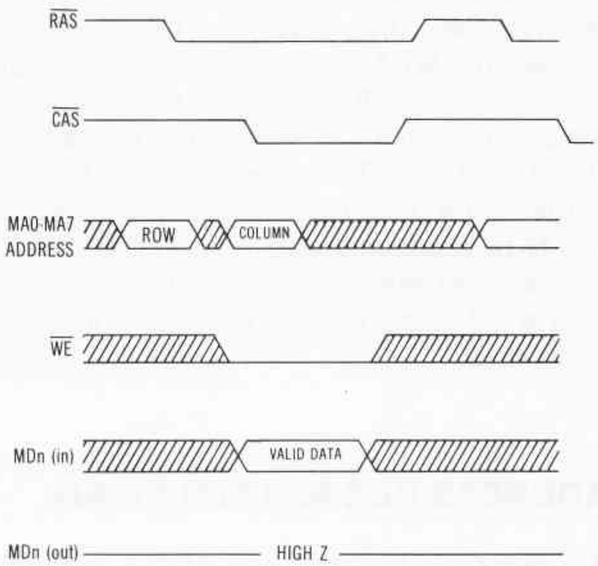


Fig. 2-37. Write cycle timing.

In this mode, WE* and MDn-in (pin 2) are delayed until after MDn-out (pin 14) becomes valid reading data out onto the data bus.

During an early write or delayed write operation, the falling edge of CAS* or WE* strobes the data in onto the data in buffer. During early write, WE* becomes active low before CAS* and the data is strobed into the chip by CAS*. During early write MDn-out (pin 14) is always tristate. In the delayed write or read-modify-write cycle, CAS* will already be low so the data is strobed into the chip by WE*. Here, the output follows the sequence for the read cycle.

Chip Select Circuitry

Figure 2-38 shows the circuitry associated with the row and column strobe signals that are used

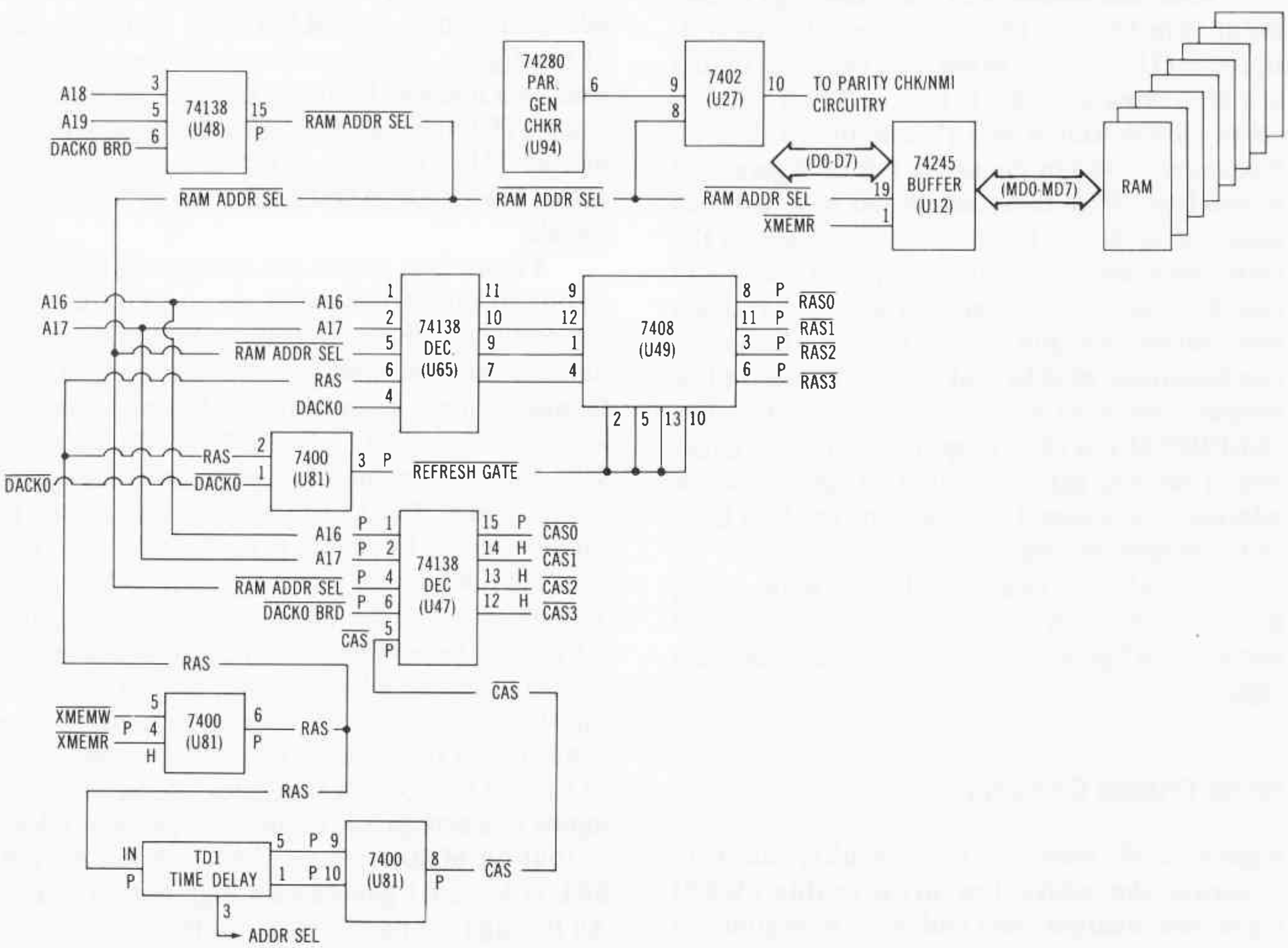


Fig. 2-38. RAM chip-select circuitry.

to select and operate the four banks of RAM memory. The occurrence of a buffered memory write (XMEMW*) or buffered memory read (XMEMR*) on pins 4 and 5 of 7400 quad 2-input NAND gate (U81) produces a high row address strobe signal (RAS) on output pin 6, as shown in the lower left of Figure 2-38. RAS is input to time delay TD1 where it becomes a delayed address select signal (ADDR SEL), and later, delayed inputs to pins 9 and 10 of U81 generating active low column address strobe (CAS*) on output pin 8. CAS* is used as an enable input to 74138 decoder (U47).

The RAS output from U81 is also connected to one input of U81 (pin 2) where it is NANDed with DACK0 on pin 1 to generate a (REFRESH GATE)* signal on pin 3. (REFRESH GATE)* becomes the qualifying input to each gate in 7408 quad 2-input AND gate (U49).

RAS also connects to the active high enable input (pin 6) of 74138 1-of-8 decoder/demultiplexer (U65). The other two enabling inputs are met when DACK0 is low, and ram address select (RAM ADDR SEL)* from the 74138 1-of-8 decoder (U48) in the upper left of Figure 2-38 is also low. With these conditions met, U65 will generate an active low output depending on the code comprised of inputs A16 (pin 1), and A17 (pin 2). Pin 3 (not shown) is tied high causing a low output on pin 7, 9, 10, or 11 for all combinations of A16 and A17. The active low output from U65 is ANDed with the active low (REFRESH GATE)* output from U81 to cause one of the AND gates to output an active low row address strobe signal (RASn*) for use by a bank of RAM memory chips.

Therefore, decoder U65 (with U49) produces the row address select signals, and decoder U47 produces the column address select signals.

Write Enable Circuitry

Figure 2-39 includes the circuitry used to generate the active low write enable (WE*) signal that enables read and write operations in the RAM memory. An active low buffered memory write signal (XMEMW*) is passed through 7404 hex inverter (U83) twice to produce the WE* signal that is applied to pin 3 of each dynamic RAM chip in the system and tristate enable pin 3 of 74125 quad 3-state buffer (U80). In U80, WE* is combined with the pin 5 output from 74280 parity generator checker (U94) to produce a parity bit (MDP) that is stored in the same row-column location as the data word being written into the other eight RAM chips.

ADDRESS BUS MULTIPLEXING

As shown in the lower left of Fig. 2-40, two 74LS158 quad 2-input data selector/multiplexers (U62 and U79) select row, and then column addresses for generating the MA0 through MA7 address inputs to each RAM chip. At the top left of the figure, 74245 octal transceiver (U12) is used as a one-way buffer to transfer the data bus signals (D0 through D7) onto the memory data bus as MD0 through MD7 under control of active low (RAM ADDR SEL)* and XMEMR* signals.

Figure 2-41 shows the internal architecture of one of the two multiplexers used to develop the row and column addresses. Multiplexer U62 handles the first nibble of these addresses. A0 through A3 are each connected to one input of internal AND gates 1, 3, 5, and 7. A8 through A11 are connected to one input of internal AND gates 2, 4, 6, and 8. Pin 15 is tied low enabling one of the two inputs to enable gates E1 and E2. The condition of address select (ADDR SEL) on pin 1 qualifies one of the other enable inputs to gates E1 or E2. Depending on which enable gate (E1 or E2) produces a high output, four of the eight input AND gates are selected passing the condition of the address bit at their other input to each of four output NOR gates. A zero on both inputs to a NOR gate is required to produce a high output on MA0 through MA3. When ADDR SEL is high, E1 generates a high output letting A0 through A3 pass through to the output (pins 4, 7, 9, and 12). The output signals MA0 through

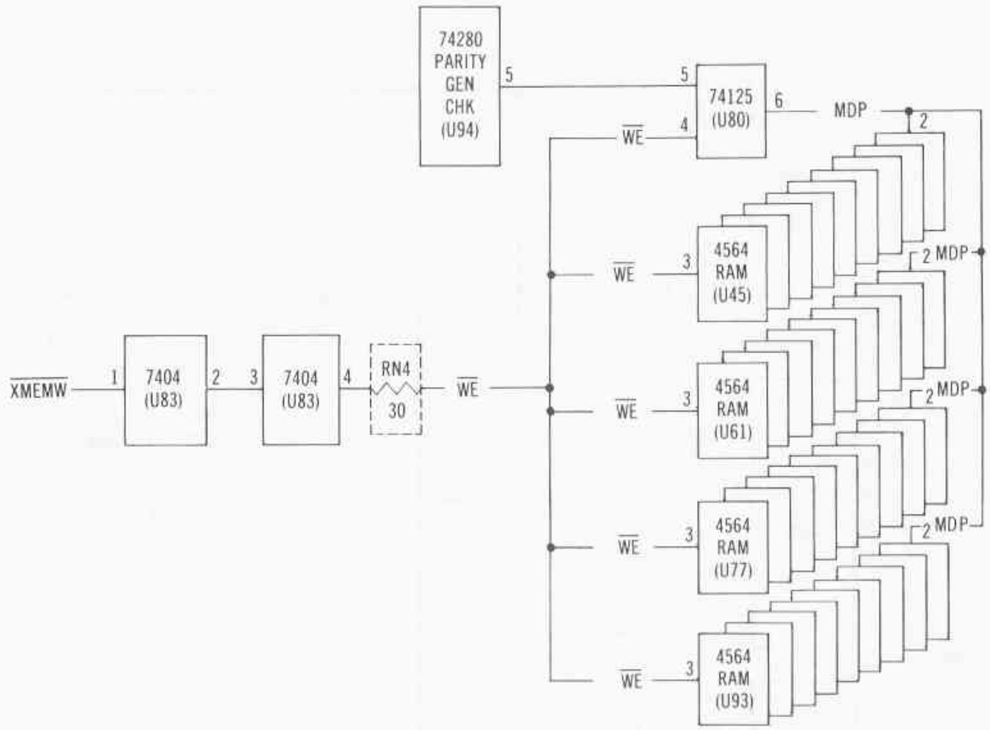


Fig. 2-39. Write enable (WE*) circuitry.

MA3 are actually the inverted condition of the qualified inputs.

The first address to pass through U62 and U79 is used to identify the row within each memory chip in a particular bank. Figure 2-42 shows that RAS is applied to time delay TD1 to produce an address select signal (ADDR SEL) that is passed to pins 1 of U62 and U79. The row addresses (A0 through A3) become valid (R valid) shortly after ADDR SEL goes high. When ADDR SEL returns low, the column address (A8 through A15) becomes valid (C valid) and is made available as MA0 through MA7 on the outputs of U62 and U79.

Table 2-9 shows the logic operation of U62. When (RAM ADDR SEL)* is high, no MEMW* signal will affect the output and no multiplexing occurs.

Figure 2-43 ties all the preceding control and enabling signals to describe the RAM addressing circuitry for bank 0. Row address select bank 0 (RAS0*) is generated by U49 and is held active low on the pin 4 input to each RAM chip in the array. The column address select bank 0 (CAS0*) signal is produced by U47. Multiplexers U62 and U79 produce the MA0 through MA7 address corresponding to the A0 through A7 row address input. When RAS0* occurs, the row address is latched inside each RAM chip. Then address select enable signal ADDR SEL goes low causing U62 and U79 to pass the A8 through A15 column address out as MA0 through MA7. CAS0* goes active low and the column address is latched into each RAM chip. Depending on the condition of write enable (WE*), data is written into each chip through pin 2 (MD0 through MD7), or read out of each chip via pin 14 (MD0 through MD7).

Table 2-9. Logic Table Relationship for 74LS158 Multiplexer U62

Enable Signal (RAM ADDR SEL)	Select Signal (MEMW)	Address Data (IN)	Address Data (OUT)
H	X	X X	H
L	L	A B	A
L	H	A B	B

A = input addresses A0-A3
B = input addresses A8-A11

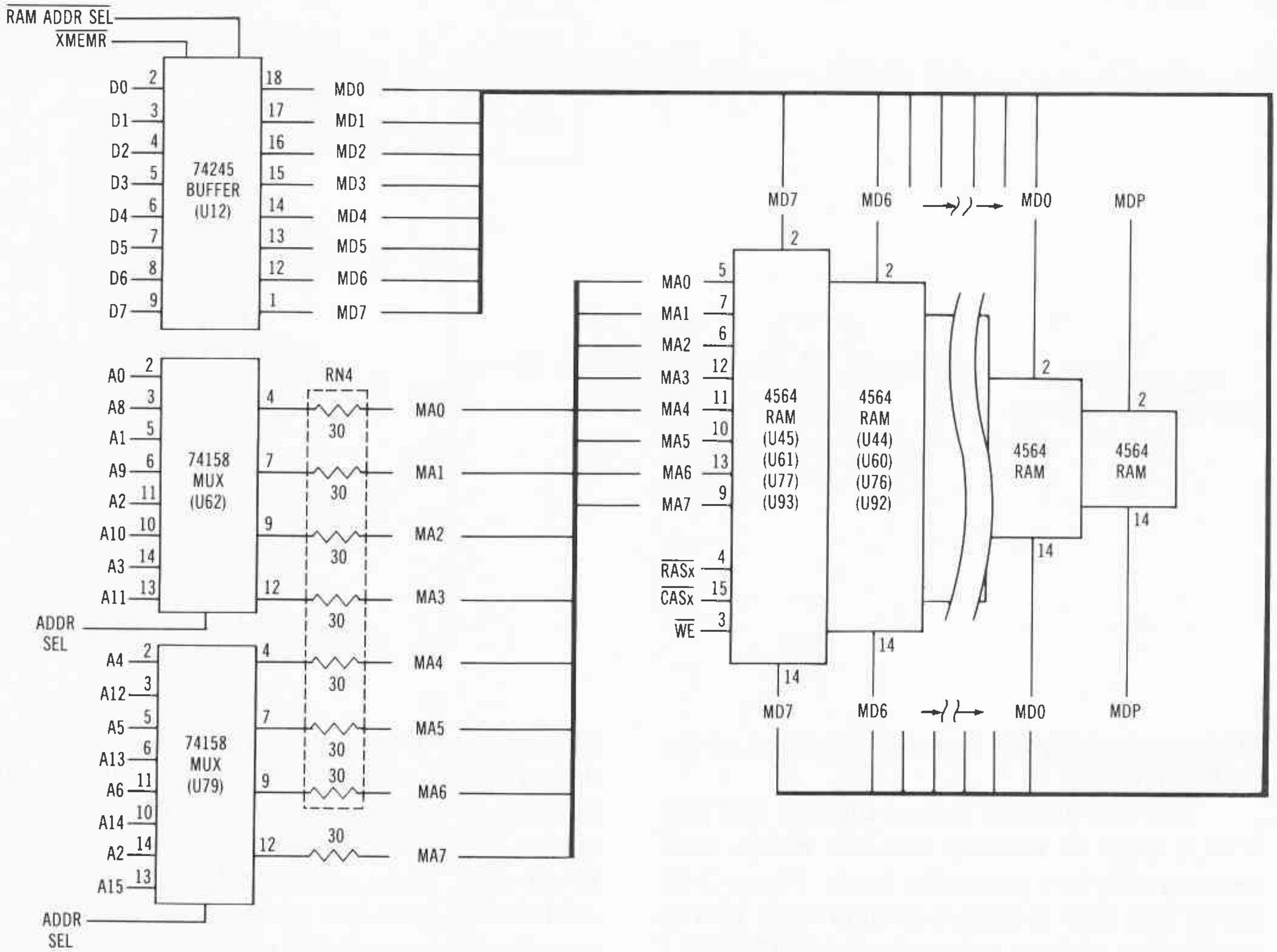


Fig. 2-40. RAM memory circuitry.

REFRESH

The RAM chips on your IBM PC system board are dynamic. Each memory cell is comprised of a single transistor that acts like a sample-and-hold circuit in which a capacitor is charged (logic 1) or discharged (logic 0). Since the charge in each cell can leak away, each memory location must be periodically accessed to restore the charge in cells that are in the logic high condition. The periodic accessing of memory to restore charge is called "refresh." The dynamic RAM (DRAM) chips in your system must be refreshed every 2-to-4 milliseconds.

Each time a DRAM location is read, all the memory cells in that row are refreshed. Capacitors that held a logic high are recharged to the full logic 1 charge. Depending on the manufacturer of the dynamic RAM in your system, refresh must occur each 2-to-4 milliseconds. Refresh is accomplished by doing a memory cycle at each of the 256 row addresses (8 bits = 256 address combinations) within each 2-to-4 millisecond interval. Any cycle in which RAS* becomes active will refresh the entire row. Because the chip output buffer is tristate to high impedance unless CAS* is applied, refresh can occur without ever activating CAS*. This RAS*-only refresh avoids any output during refresh and conserves power during the memory cycle. The RAS*-only refresh timing is shown in Fig. 2-44.

The counter OUT1 signal from the 8253 programmable interval timer (U34) shown in Fig. 2-45 clocks the 7474 dual-D latch (U67) to send a

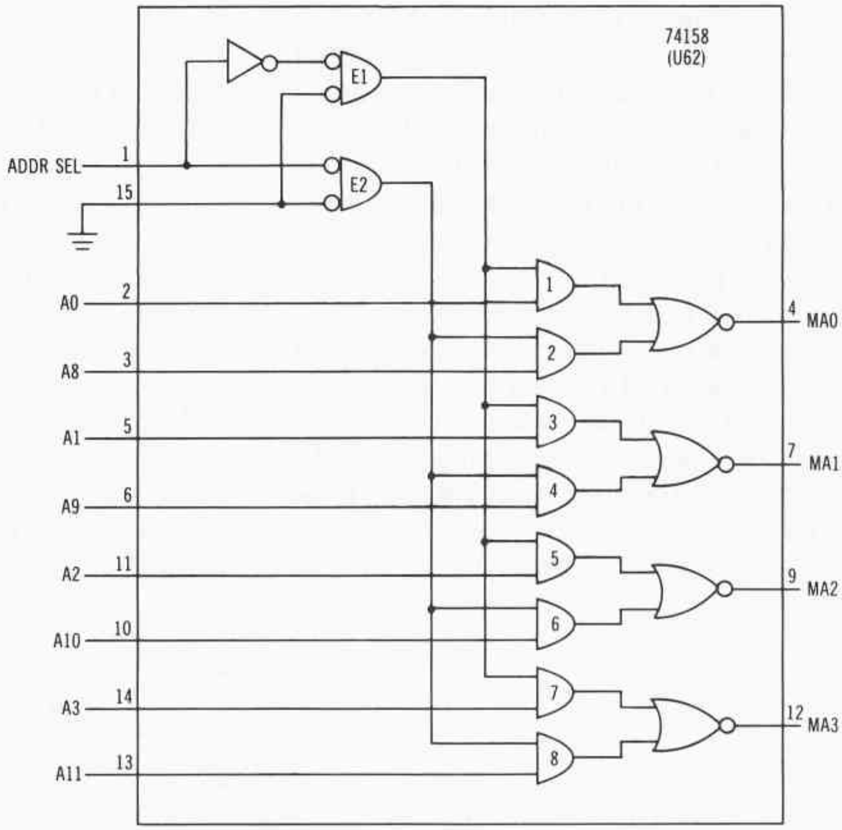


Fig. 2-41. The 74158 quad 2-input data selector/multiplexer.

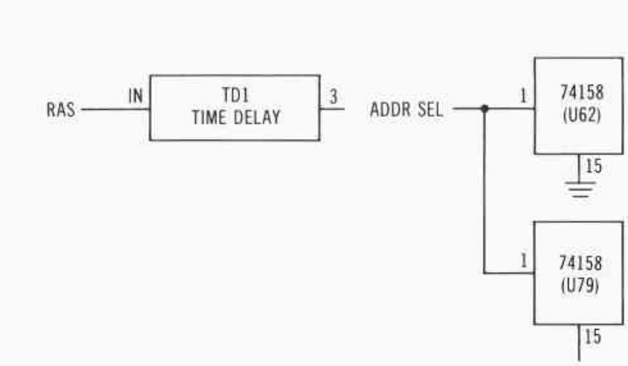


Fig. 2-42. Multiplex input selection timing and circuitry.

DMA request signal (DRQ0) into pin 19 of 8237 DMA controller (U35). The results in a (DACK0 BRD)* response out pin 25 that goes up to connect with pin 17 of 74244 buffer (U15) to become DACK0*. DACK0* combines with RAS in 7400 quad 2-input NAND gate (U81) to generate a (REFRESH GATE)* signal that enables the four gates in 7408 quad 2-input AND gate (U49) generating the row address strobe signals (RAS0*, RAS1*, RAS2*, and RAS3*) to the four dynamic RAM banks of memory. Each of these strobe signals represents the RASn* input to a particular RAM chip. Since OUT1 occurs every 15 microseconds, the memory accesses caused by OUT1 are well within the 2-to-4 millisecond refresh requirement. Refresh affects the memory on the system board and on any I/O expansion boards.

PARITY

Each bank of RAM chips includes one additional memory chip that is totally dedicated to storing a bit corresponding to the parity of the 8 bits stored for each byte or word of data. In the IBM PC, each word of data written into memory is evaluated to determine the number of binary 1s in the word. If the number of 1s is an odd number, a 0 parity bit is stored in a special memory chip (parity memory). If the number of 1s is even, a 1 parity bit is stored in the corresponding location in the parity memory chip.

When 8 bits of data are read out of memory, the parity of the word is checked by special circuitry on the system board and compared to the parity bit stored in the corresponding location in the parity RAM. If the two parity values (computed and stored) are equal, the data word is accepted by the CPU or co-processor and system operation continues. However, if the two values differ, a non-maskable interrupt (NMI) occurs, causing the machine to halt with a "PARITY CHECK" display on the screen.

The key to parity generation and checking is the 74LS280 9-Bit odd/even parity generator/checker (U94). Figure 2-46 is a logic diagram of U94. The 74LS280 is used to detect errors in data retrieval from the RAM memory. Both even and odd parity outputs are available. If the number of data inputs that are high is even, the even parity output on pin 5 goes high. If the number of high data bits is odd, the odd parity output (pin 6) goes high, and the even parity output (pin 5) goes low.

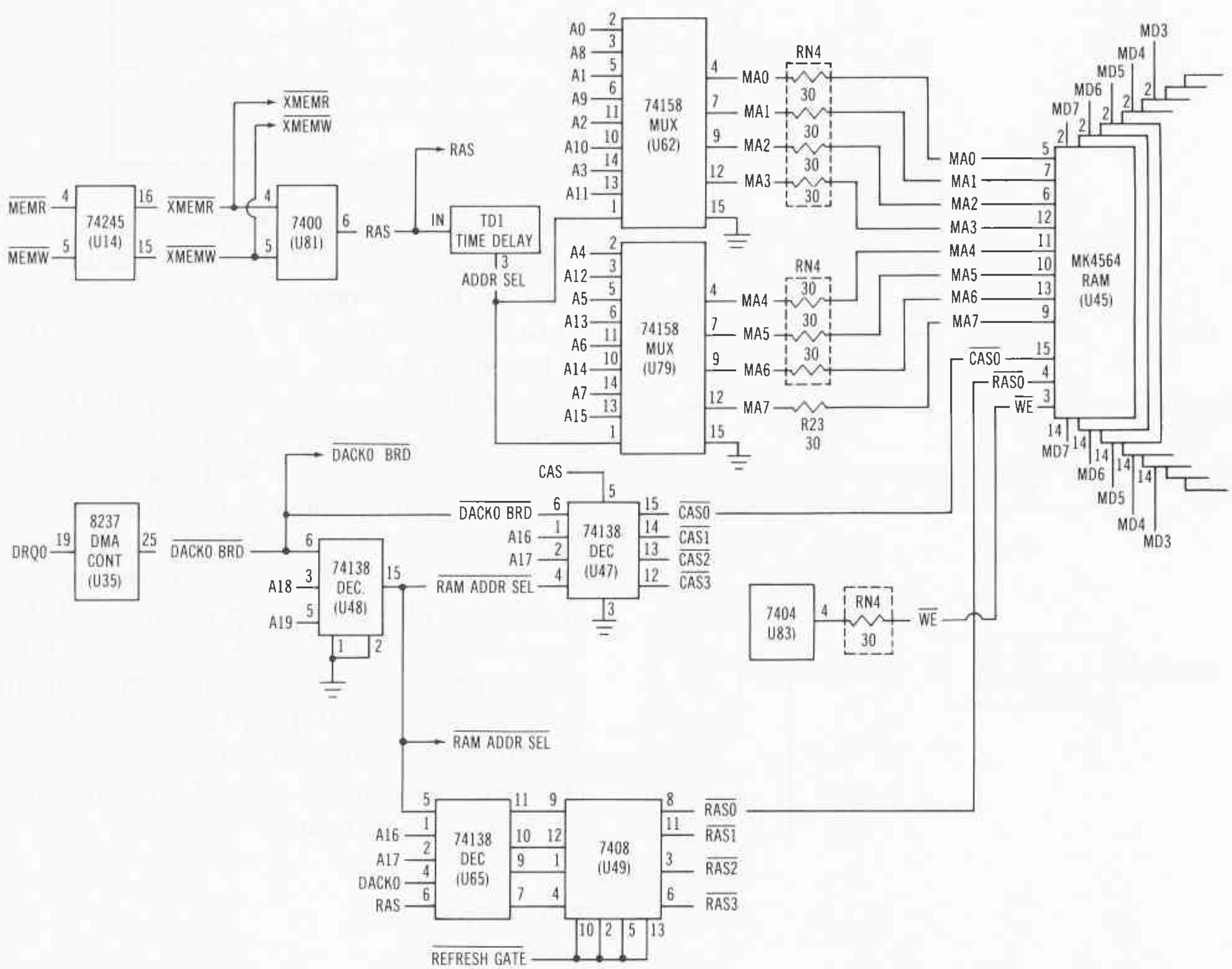


Fig. 2-43. RAM addressing circuitry–bank 0.

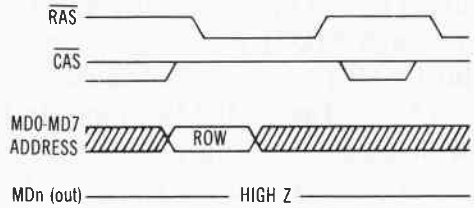


Fig. 2-44. RAS*-only refresh timing.

Both the even and odd parity outputs are used during memory writing and reading operations. The memory data bits (MD0 through MD7) that are being read into RAM are also applied to the inputs of U94 (pins 1, 2, and 8 through 13). The pin 4 input is generated by the ANDing of a parity bit read from memory and the status of the buffered memory read signal

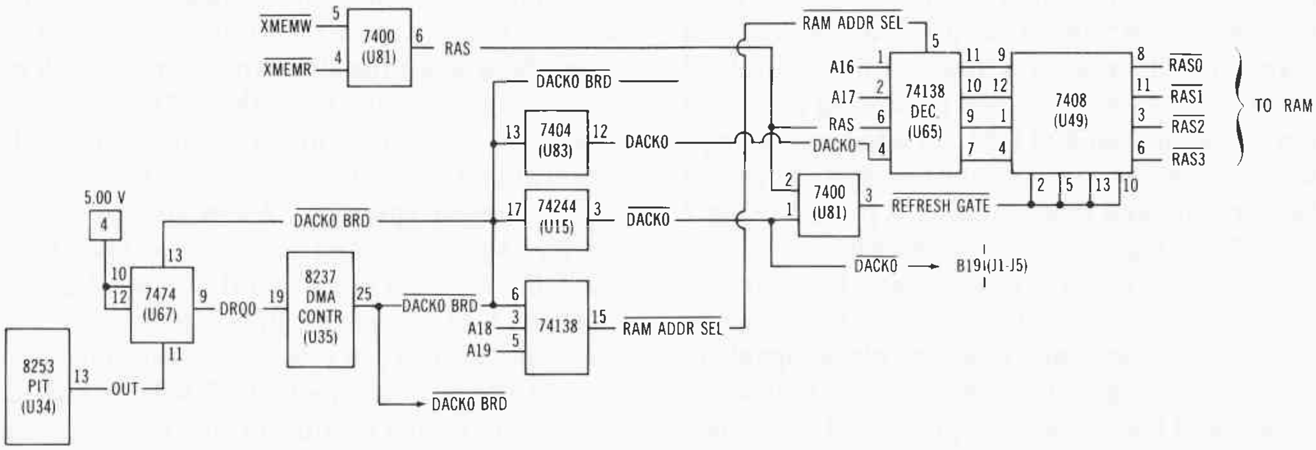


Fig. 2-45. Dynamic RAM refresh circuitry.

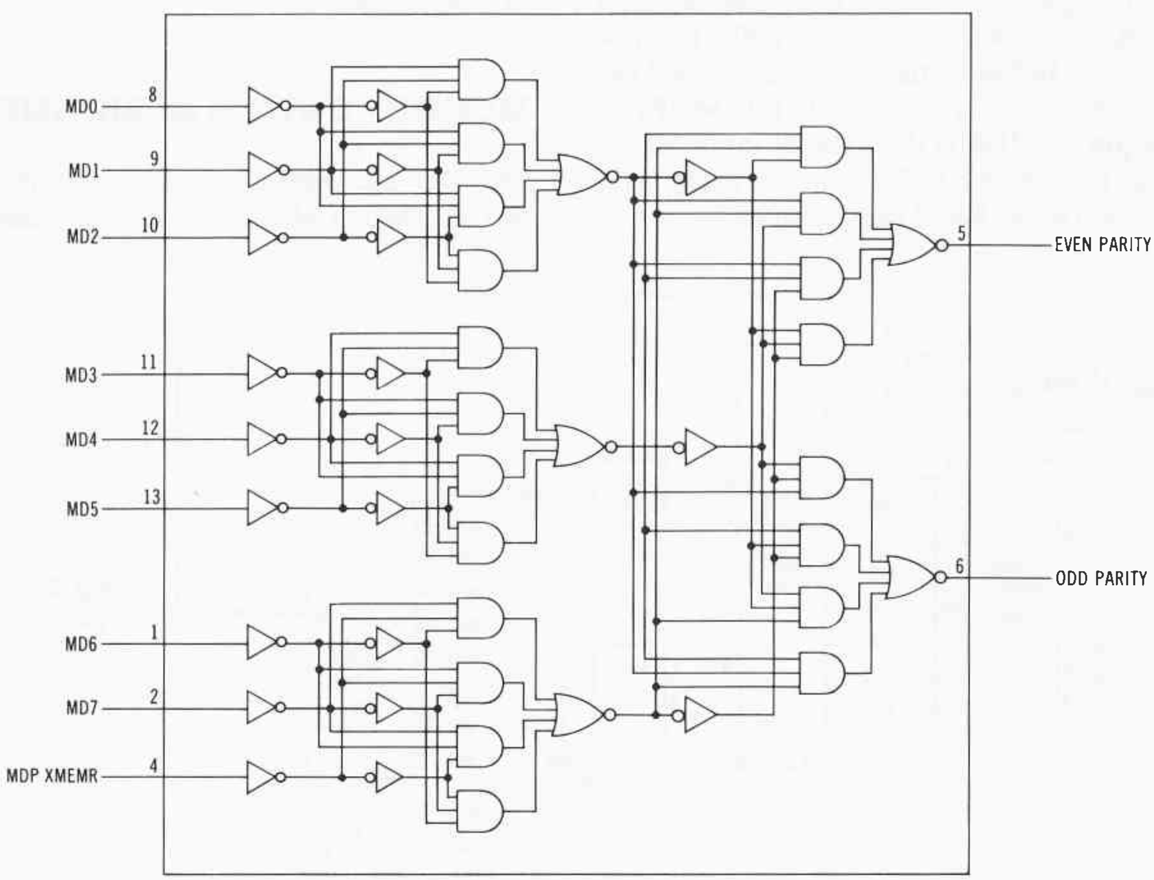


Fig. 2-46. Logic diagram of parity generator/checker U94.

XMEMR*. The nine inputs to U94 are passed through an inverter, buffer, AND, and NOR, circuit to yield outputs on pins 5 and 6 that correspond to the parity of the nine input data bits.

Figure 2-47 shows the parity circuitry in your PC. The buffered memory data bits MD6 and MD7 are combined with the pin 4 input from 74LS08 quad 2-input AND gate U97. This input is low during a write operation because the logic high XMEMR* input on pin 5 of 74LS04 hex inverter U83 places a low on pin 5 of U97 disabling the AND gate and producing a low out pin 6 and into pin 4 of U94. In addition, during a write operation, the output of each RAM chip is held tristate and this condition is passed to pin 4 of U97 as a high impedance open wire.

Parity generator/checker U94 is an asynchronous device that responds to signals on its inputs without any enabling clock signals to cause a timed operation. As such, the outputs on pins 5 and 6 are always represented. During a write operation, the pin 5 even parity output is passed into pin 5 of 74LS125 quad 3-state buffer U80. Active low write enable (WE*) is low enabling the buffer so the even parity signal can become the memory data parity bit (MDP) on output pin 6. MDP is the data bit input MD-in on input pin 2 of the MK4564 parity RAM (U37 in Fig. 2-47) in the RAM bank selected.

During a read operation, the 8 bits of data (MD0 through MD7) and the corresponding parity bit (MDP) are read out of memory and input into U94. The XMEMR* input to U83 is now low placing a high on pin 5 of U97. The combination of MDP and XMEMR produces an output signal from pin 6 of U97. This becomes one of the nine inputs to U94 during a parity checking operation. If the data word stored had an even number of 1s, the MDP value stored was high. Now when the data word is read back out of memory and into U94, the MDP high value causes the number of 1s to be odd. This generates a low out pin 5 and a high on odd parity output (pin 6). When this high (odd parity) signal is ORed with active low (RAM ADDR SEL)* on pin 8 of 74LS02 quad 2-input NOR gate U27, its pin 10 output is low.

However, if pin 6 is ever low during a read operation, both inputs to U27 will be enabled producing a high on output pin 10. This logic high will cause a non-maskable interrupt (NMI) to be generated.

MEMORY SWITCH ASSIGNMENT

Two DIP packages are mounted on the system board. Switch block 1 is used to identify the

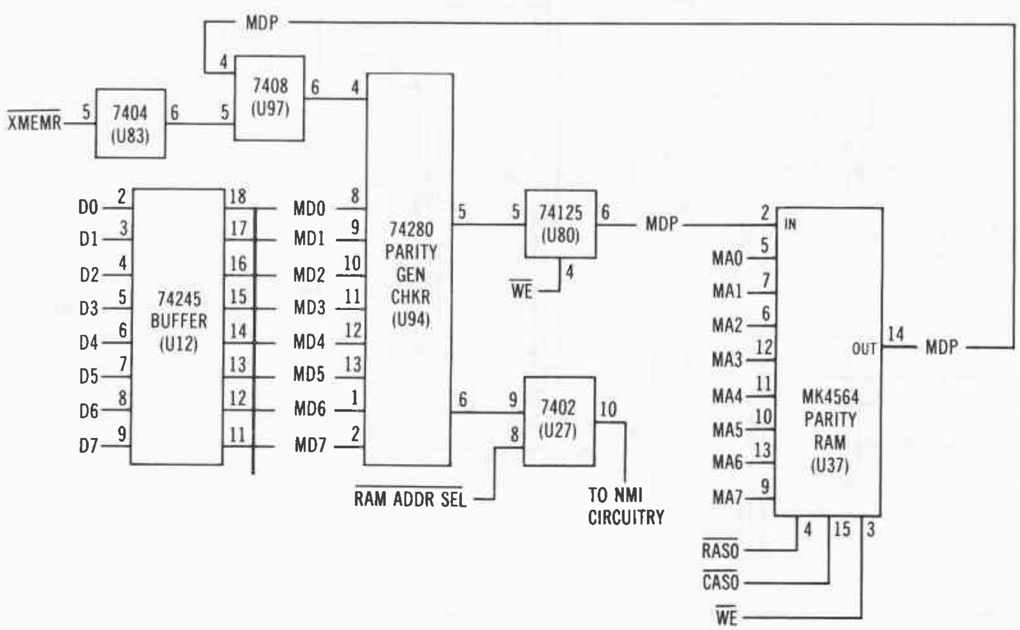


Fig. 2-47. RAM parity circuitry.

number of 5-1/4 inch diskette drives installed, the existence of an 8087 math coprocessor, the types of display connected, and the system board memory. Switch block 2 is used to define the amount of memory installed in the system.

Table 2-10 shows the function associated with each of the eight switches in blocks 1 and 2.

Table 2-10. System Board Switch Assignments

Switch	Function
	Switch Block 1:
1	Number of installed 5 1/4 inch diskette drives
2	Math coprocessor installed
3	System board memory
4	System board memory
5	Type of display connected
6	Type of display connected
7	Number of installed 5 1/4 inch diskette drives
8	Number of installed 5 1/4 inch diskette drives
	Switch Block 2:
1	Amount of installed memory
2	Amount of installed memory
3	Amount of installed memory
4	Amount of installed memory
5	Amount of installed memory
6	Always off
7	Always off
8	Always off

Figure 2-48 shows that both switches are connected to and read by the P8255A-5 programmable peripheral interface (U36). Each switch setting is manual. When each switch block is read by U36, a software program examines the input to U36 ports A and C and interprets the data to determine the type of system board configuration being accessed.

I/O MEMORY OPERATION

As described earlier, 64K of I/O memory space is available to the IBM PC system. Figure 2-49 shows the I/O device decoding circuitry. Two primary chips are involved in generating the chip select/decode signals. On the far left, 74LS245 octal transceiver (U14) has active low IOR* and IOW* on its input pins 2 and 3. Its chip enable pin 19 is tied to ground constantly qualifying U14 for operation. Send/receive control pin 1 has inactive high (DMA AEN)* connected. With pin 1 high and pin 19 low, U14 is configured to pass data from left to right. The output signals from U14 are labelled XIOR* (pin 18), and XIOW* (pin 17). Active low buffered I/O read (XIOR*) and active low buffered I/O write (XIOW*) act as qualifying signals for various chips in Fig. 2-49. In the center of Fig. 2-49, XIOR* is connected to input pin 12 of 74LS02 quad 2-input NOR gate (U27). This signal combined with XA9, and (ROM ADDR SEL) ANDed with XMEMW determine the logic value of direction (DIR) out pin 1 of U27. When address enable board (AEN BRD) is low, the value of DIR determines the direction of information flow through 74LS245 data bus octal transceiver (U13). When XA9 and the other three signals that generate DIR are low, DIR becomes low causing U13 to read data from left (XD0 through XD7) to right (D0 through D7) into the 8088 CPU (U3).

Besides U14, the other critical chip in the Fig. 2-49 select and decode circuitry is 74LS138 3-of-8 decoder U66. Three inputs are applied to U66: XA5 (pin 1), XA6 (pin 2), and XA7 (pin 3). The signals that enable U66 are XA8 (pin 5), XA9 (pin 4), and AEN* (pin 6). To enable U66, XA8 and XA9 must both be low–AEN* must be high. When these conditions are met, the combination of XA5, XA6, and XA7 will cause one of the eight (six of eight used) outputs to go active low.

The 8088 CPU (U3) can address up to 64K I/O ports using the lower 16 bits of its address bus (AD0 through AD7 and BA8 through BA15). Notice that the IBM PC only uses XA5 through XA9 for I/O port addressing. XA0 through XA4, and the buffered addresses above XA9 are ignored. This results in redundant addressing in that 32 different combinations of XA0 through XA9 can cause each of the U66 outputs to go active low. If XA5 through XA9 are all low, and AEN* is high, pin 15 is pulled low producing an active DMA chip select (DMA CS)* signal for the 8237 DMA controller (U35). However, with

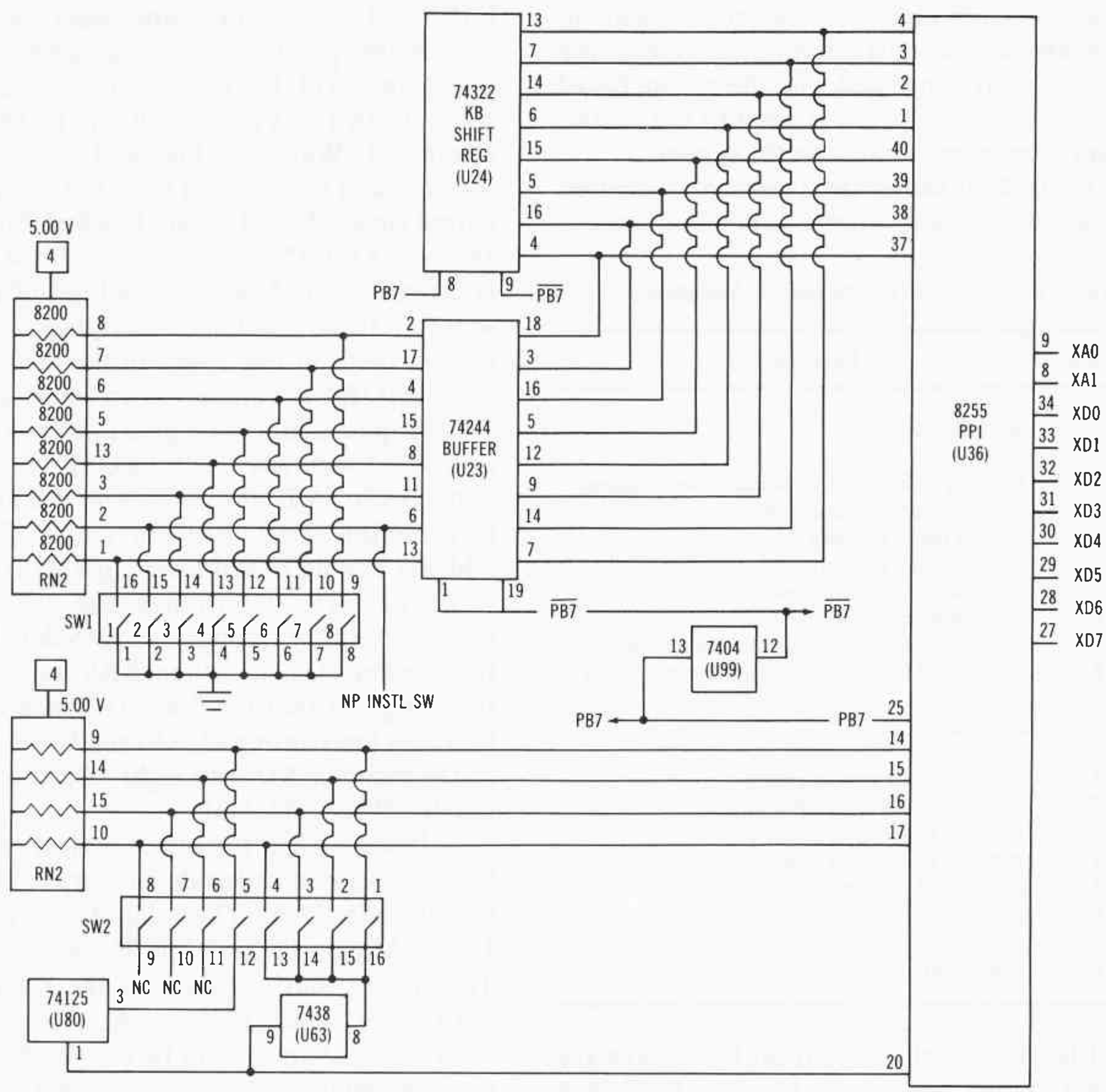


Fig. 2-48. Switch block read circuitry.

these same input conditions, XA0 through XA4 can cycle through 32 different combinations and still produce the same pin 15 (DMA CS)* output.

If U66 is enabled, and the XA5 through XA7 input is high-low-low, pin 14 goes active low producing interrupt chip select (INTR CS)* for the 8259 programmable interrupt controller (U2). Similarly, a low-high-low input combination will produce an active low terminal/count chip select (T/C CS)* for the 8253 programmable interval timer (U34). Another combination of XA5 through XA7 produces the active low pin 12 PPI chip select (PPI CS)* signal for the programmable peripheral interface (U36).

A low-low-high input produces an active low output on pin 11. This output is passed to pin 12 of 74LS02 quad 2-input NOR (U50). If XIOW* is also low (an output instruction is being executed), pin 13 of U50 goes high. This signal is inverted by 74LS04 (U51) to produce an active low (WRT DMA PG REG)* input to pin 12 of the 74LS670 DMA page register (U19).

A high-low-high input to U66 produces an active low output on pin 10. This signal is passed to pin 8 of another NOR gate in 74LS02 (U50). Its companion pin 9 input is XIOW*. If XIOW* is also active low, (WRT NMI REG)* goes active low on the clock input (pin 11) to 74LS74 dual

D-latch (U96). When (WRT NMI REG)* returns high, the positive transition of this signal transfers the value of XD7 to its Q output in the non-maskable interrupt (NMI) circuitry. This makes the NMI software maskable.

INTERRUPTS

The sequential execution of instructions by 8088 CPU U3 can also be altered by special input signals (NMI and INT) on pins 17 or 18. CPU interrupts can be generated by the hardware or initiated by software during program execution. Hardware interrupts are classified as maskable (can be ignored by design) or non-maskable.

The recognition of an interrupt by 8088 CPU U3 causes the machine to transfer control to a new program location. The 1024 memory locations (00H through 3FFH) are dedicated to storing up to 256 four-byte interrupt vectors which contain address pointers to the interrupt routines stored elsewhere in the memory space of the system. Each vector is comprised of a 16-bit base address in the higher-addressed word for the code segment register and a 16-bit offset in the lower-addressed word for the instruction pointer register inside the CPU, as shown in Fig. 2-50. Taken together these two registers point to a particular vector memory location where an interrupt service routine is stored. Each vector is 4 bytes long so the CPU can calculate the starting location of the correct interrupt code entry by multiplying the type code by four (for example, type 1 x 4 equals location 004H).

Four classes of interrupts are possible in the IBM PC system:

1. CPU internal interrupt
2. Non-maskable interrupt
3. External interrupt
4. Single-step interrupt

The four interrupt sources for U3 are shown in Fig. 2-51.

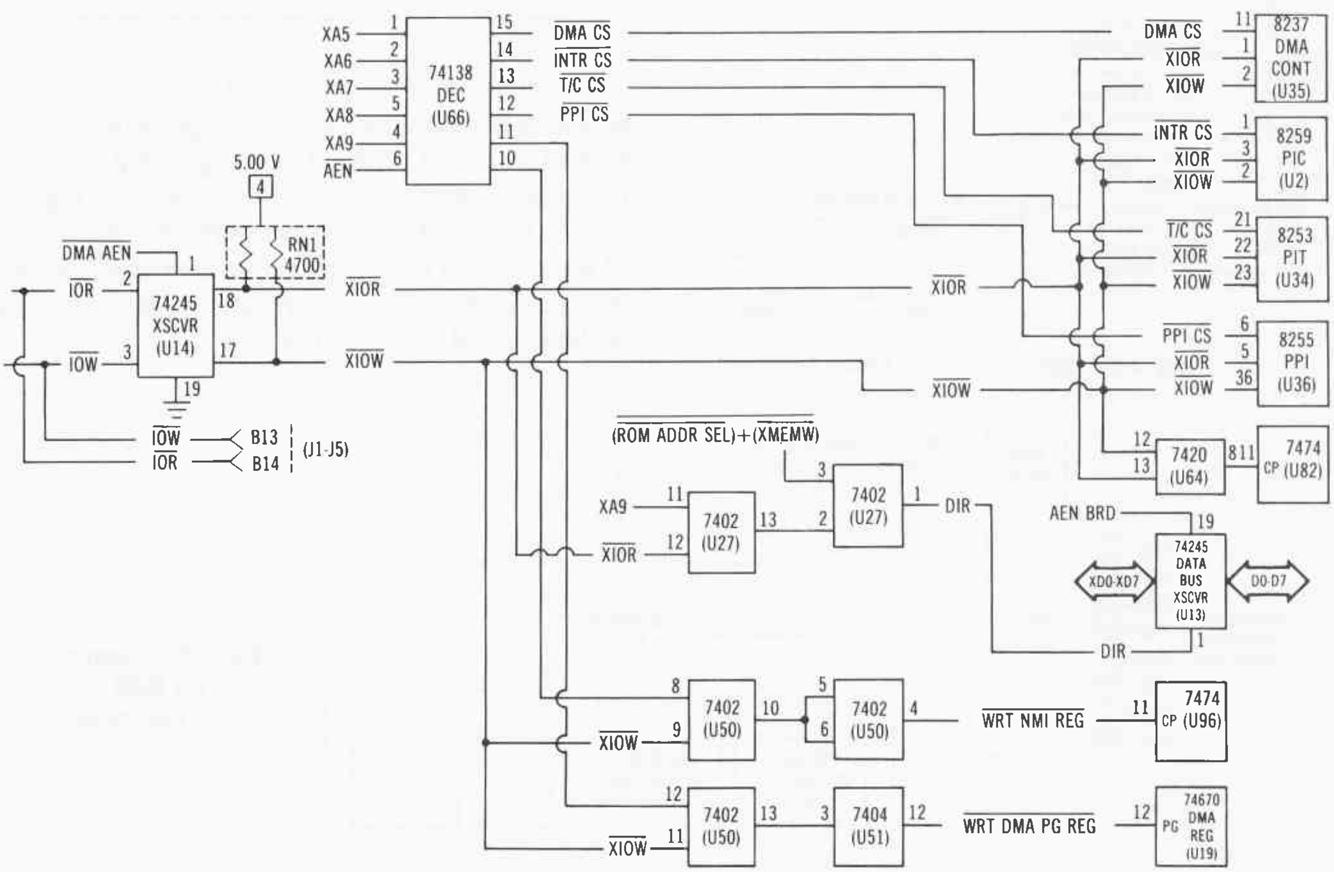


Fig. 2-49. I/O read/write chip select and decoding circuitry.

Interrupts have an internal priority for servicing by U3. Internal interrupts such as divide error, program interrupt, and overflow have the highest priority followed by the non-maskable, external device, and internally programmed single-step interrupts.

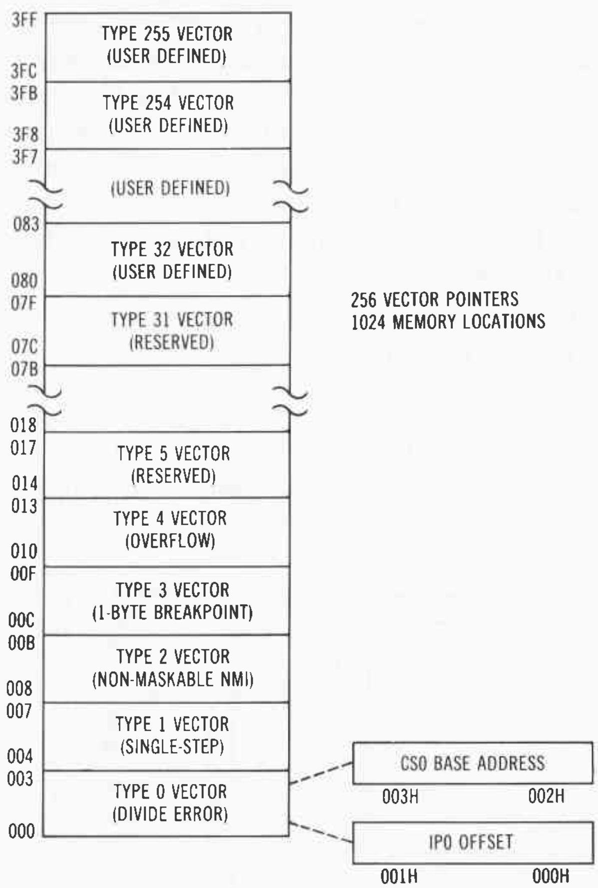


Fig. 2-50. Interrupt vector table.

When an interrupt occurs, U3 completes its current instruction and then begins to service the interrupt(s) on a priority basis. The interrupt latency (interval between CPU recognition of interrupt request and execution of initial interrupt routine) including time to save CPU status and register contents (interrupts only save CS, IP, and flag registers automatically) can vary between 50 and 61 clock cycles as shown in Table 2-11.

Table 2-11. Interrupt Priority and Processing Times

Interrupt	Priority	Description	Internal/ External	Minimum Servicing Time (clocks)
Type 0	1	Divide error	Internal	51
Type 1	4	Single step	Internal	50
Type 2	2	Non-maskable	External	50
Type 3	1	1-byte breakpt	Internal	52
Type 4	1	Overflow (into)	Internal	53
Software	1	Program (intn)	Internal	51
Hardware	3	Maskable (int)	External	61

Each time an interrupt occurs, certain action takes place within U3 depending on the type of interrupt. Except for single step, internal interrupts cannot be disabled. With a higher service priority for internal interrupts, the arrival of an external interrupt request at the time an internal interrupt occurs results in the servicing of the internal interrupt first.

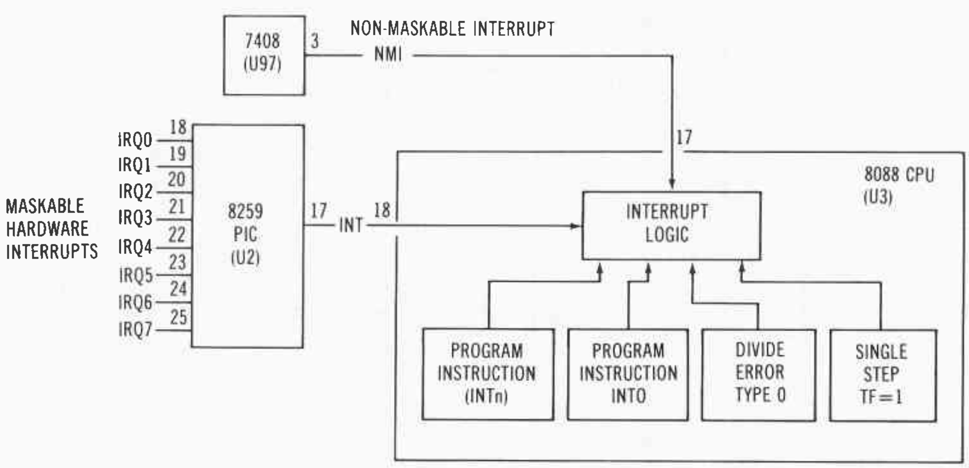


Fig. 2-51. Sources for 8088 CPU interrupts.

Internal Interrupts

Internal interrupts can be generated by program instructions INT and INTO, by error conditions resulting from DIV or IDIV instructions, and by single stepping each instruction when the trap flag (TF) has been set in the control flag portion of the 8088 execution unit. Setting TF to high causes the CPU to cause a type 1 interrupt after execution of each instruction. This single-step operation for most instructions is useful for program debugging.

A programmed interrupt (INTn instruction) and other internal interrupts cause the interrupt code contained in the instruction or a predefined interrupt code to be recognized by the CPU.

External Interrupts

Hardware interrupts from external devices are achieved in two ways. Parity errors result in the generation of a non-maskable interrupt signal (NMI) that is applied to pin 17 of the 8088 CPU U3. All other hardware interrupts are generated via interrupt request input signals to a 8259 interrupt controller (U2), as shown in Fig. 2-52. Chip pin descriptions appear within the 8259 block. IBM PC chip pin assignments are on each line connected to the block from outside. The output of U2 is a CPU interrupt INT applied to pin 18 of 8088 U3.

8259 Interrupt Circuitry

The 8259 programmable interrupt controller is a 28-pin DIP (dual in-line package) that handles up to eight vectored priority interrupt requests and generates a logic high interrupt signal to the CPU. The asynchronous logic requires no clock input. It responds to any interrupt request input given the control lines are properly configured. Its ability to handle multilevel priority interrupts minimizes software and real-time system overhead.

A description of the function of each active pin on U2 is provided in Table 2-13. Some pins (12, 13, and 15) are not used in this configuration.

Table 2-12 lists the IBM PC interrupt vector assignments.

Table 2-12. IBM PC Interrupt Vector Assignments

Interrupt Type	Function
0	Divide by zero error
1	Single-step
2	Non-maskable interrupt (NMI)
3	One-byte breakpoint
4	Overflow
5	Invokes logic to print screen
6	Reserved
7	Reserved
8	Time of day (18.2/second)
9	Keyboard hardware interrupt
A	Reserved
B	Serial communications
C	Serial communications
D	Fixed disk hardware interrupt
E	Diskette hardware interrupt
F	Printer hardware interrupt
10	Video input/output call
11	Equipment check call
12	Memory check call
13	Diskette input/output call
14	RS-232 input/output call
15	Cassette input/output call
16	Keyboard input/output call
17	Printer input/output call
18	ROM basic entry code
19	Boot strap loader
1A	Time of day call
1B	Get control on keyboard break
1C	Timer interrupt control
1D	Video initialization table pointer
1E	Diskette parameter table pointer
1F	Graphics character generator pointer
20	DOS program terminate
21	DOS function call
22	DOS terminate address
23	DOS CTRL-BRK exit address
24	DOS fatal error vector
25	DOS absolute disk read
26	DOS absolute disk write
27	DOS terminate, fix in storage
28-3F	DOS (reserved)
40-5F	Reserved
60-67	User software interrupts
68-7F	Not used
80-85	BASIC interrupts (reserved)
86-F0	Used by running BASIC interpreter
F1-FF	Not used

Table 2-13. 8259 Programmable Interrupt Controller (U2) Pin Assignments

Symbol	Pin No.	Type	Name and Function
(INTR CS)*	1	I	Interrupt chip select: Active low signal that enables XIOR* and XIOW* communication between the 8088 CPU and the 8259 PIT.
(XIOW)*	2	I	External I/O Write: Active low when (INTR CS)* is low enables PIT U2 to receive command words from CPU U3.
(XIOR)*	3	I	External I/O Read: Active low when (INTR CS)* is low enables PIT U2 to place CPU status data on address/data bus.
AD0-AD7	4-11	I/O	Bidirectional Data Bus: Transfer path for control, status, and interrupt vectors.
GND	14		Ground:
(SP/EN)*	16	O	Slave program/enable buffer: Used in buffered mode as output to 7410 three-input NAND U84 which combines this signal with DEN from the 8288 bus controller to generate G*, the enable signal for 74245 transceiver U8.
INT	17	O	Interrupt: Active high when valid interrupt request is asserted. Connected to CPU interrupt input pin 18.
IRQ0-IRQ7	18-25	I	Interrupt request: Active high asynchronous inputs used to generate interrupt output (INT) to CPU.
INTA*	26		Interrupt acknowledge: Response from CPU that causes 8259 to enable interrupt vector data onto address/data bus.
XA0	27	I	Buffered address bit 0: Acts with (INTR CS)*, (XIOR)* and (XIOW)* to decode CPU U3 command words and provide status back to U3.
VCC	28	I	Supply voltage: +5.00 volts

During power-up, the BIOS software does a test on U2. It writes all zeroes into an interrupt mask register inside the 8259 and compares the value read with what was written. Then it disables device interrupts and writes all ones to this register. Again, the program reads the register contents and compares it with what was written. All 1s in this register cause all interrupt request lines to be masked. The program reenables external interrupts and waits for 1 second to check for any hot interrupts that may have occurred during the test. If an error occurs during the comparisons, the speaker beeps and the program halts the system.

When several devices attempt to interrupt the system operation at the same time, a priority has been established at the input request lines to U2. The device with the highest priority is serviced first. Higher priority inputs can be masked without affecting the interrupt request lines of lower priority inputs. IRQ0 on pin 18 is the highest priority interrupt. It is used to cause a time of day clock tick. The second highest priority interrupt (IRQ1) is used during keyboard entry. Table 2-14 lists the assignments for all eight interrupt request inputs to U2. If two request lines become active at the same time, the request whose number is closest to IRQ0 is serviced first.

Table 2-14. 8259 Hardware Interrupt Request Listing

Interrupt Request	Type of Interrupt	Function
IRQ0	Type 8	Timer
IRQ1	Type 9	Keyboard
IRQ2	Type A	Reserved
IRQ3	Type B	- Asynchronous communications (secondary) - Synchronous data link control (SDLC) communication - Binary synchronous communications (BSC)
IRQ4	Type C	- Asynchronous communication (primary) - SDLC communication - BSC (primary)
IRQ5	Type D	Fixed disk
IRQ6	Type E	Diskette
IRQ7	Type F	Printer

Figure 2-53 shows the external interrupt circuitry associated with 8259 U2. During initiali-

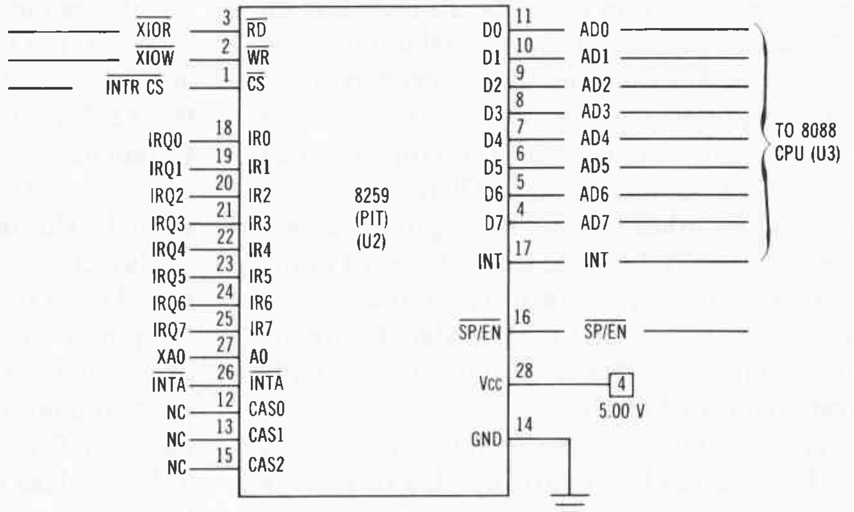


Fig. 2-52. 8259 programmable interrupt controller (U2).

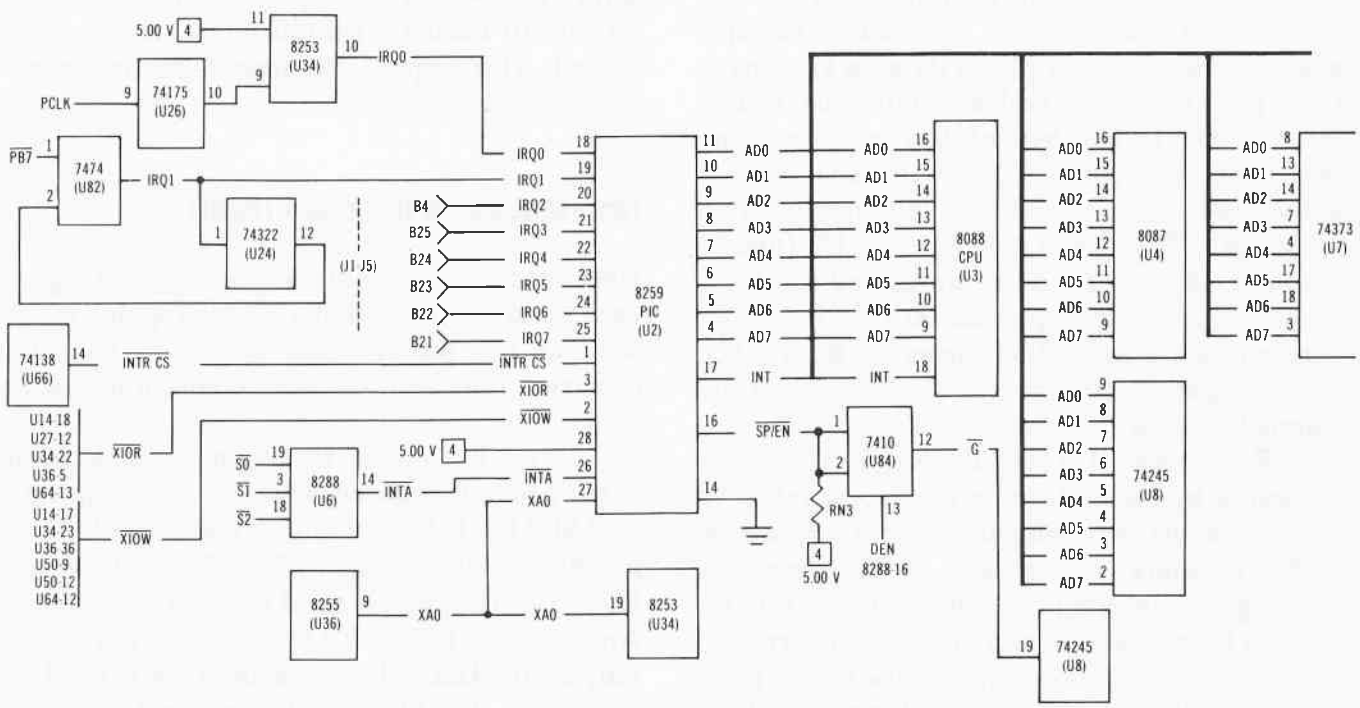


Fig. 2-53. 8259 programmable interrupt controller (U2) external hardware interrupt circuitry.

zation, U2 is configured so interrupt-request signals must make a low-to-high transition to generate INT out pin 17. The chip is also set to recognize that it is the only 8259 in the system. The chip is set to buffered mode causing (SP/EN)* to be an output from pin 16.

Interrupt Sequence

Upon sensing an active high interrupt-request signal on one of its eight inputs, U2 sets a corresponding bit in an interrupt-request register latching each interrupt request. U2 then passes an interrupt signal (INT) out pin 17 to pin 18 of CPU U3 causing the 8088 to pull status outputs S0*, S1*, and S2* active low (pins 19, 3, and 18 respectively). This code is passed to 8288 bus controller (U6) causing it to generate an active low interrupt acknowledge (INTA*) signal on pin 14.

This first INTA* signal on pin 26 of U2 communicates to the 8259 that the request has been honored by U3, and that an interrupt-acknowledge cycle is in progress. INTA* valid on pin 26 causes the 8259 programmable interrupt controller (U2) to set the highest priority bit in an interrupt-service register and to clear its corresponding bit in the interrupt-request register. CPU U3 also brings LOCK* low on pin 29 preventing other devices from gaining access to the bus. LOCK* is held active from T2 of the first INTA* bus cycle until T2 of the second INTA* bus cycle. CPU U3 also floats its address/data bus. INTA* is active during CPU bus cycle states T2 and T4.

A second 000 status signal is generated by CPU U3 causing bus controller U6 to place a second INTA* signal on U2 pin 26. When the 8259 (U2) senses this second interrupt acknowledge signal, it places data on U2 pins 4 through 11 of the address/data bus (AD0 through AD7). This byte of data represents the interrupt type (type 0 through 255) that is associated with the device requesting the interrupt. This byte is read by CPU U3 (pins 9 through 16) where it is multiplied by four producing an address pointer into the interrupt vector table. Figure 2-54 shows the 8259 (U2) edge-triggered timing relationships during external hardware interrupt activities.

Before 8088 U3 calls the interrupt routine indicated by the address in the vector table, it saves its status by pushing the current contents of its flag registers onto its stack. It then clears the flag register interrupt enable and trap bits to prevent later maskable and single step interrupts, and establishes an interrupt routine return path by pushing the current CS and IP register values onto the stack before loading these registers from the vector table.

Once the highest priority interrupt has been serviced, the next highest priority interrupt (as indicated by the next highest priority bit set in the 8259's interrupt-request register) receives system attention. One interrupt request (IRQ0) is produced approximately 18.2 times each second. This interrupt is used to produce a time-of-day clock tick. The 2.386363 MHz PCLK signal from the clock generator (U11) is sensed on pin 9 of 74LS175 quad-D flip-flop U26 producing a 1.19318 MHz clock input to 8253 programmable interval timer (U34) pin 9. Counter 0 inside U34 is preset so it accepts 65536 pulses of the 1.19318 MHz clock input before it produces an output. Counter 0 output on pin 10 occurs 1193180/65536 times each second. This output is the time-of-day interrupt-request signal (IRQ0).

Non-Maskable Interrupt (NMI)

NMI is an asynchronous edge-triggered signal used to tell the CPU that a "catastrophic" event such as bus parity error detection has just occurred. The NMI circuitry is shown in Fig. 2-55.

A parity output from pin 6 of 74LS280 parity generator checker U94 is matched up with (RAM ADDR SEL)* in a 74LS02 NOR U27 to produce a latch input to 74LS74 dual-d latch U96. (XMEMR)* is used to clock U96 pin 3. An inverted (ENB RAM PCK)* from pin 6 output of 74LS04 hex inverter U99 is used to clear U96. The Q* output from pin 6 of U96 is passed to input pin 10 of 74LS10 NAND U84. A second input to U84 comes from pin 1 of a

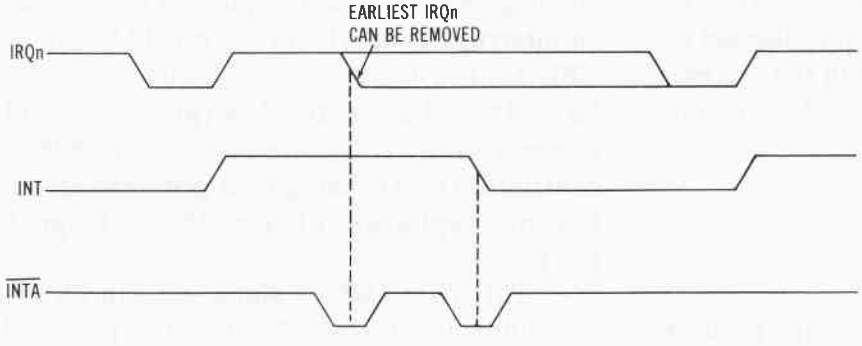


Fig. 2-54. 8259 interrupt timing relationships.

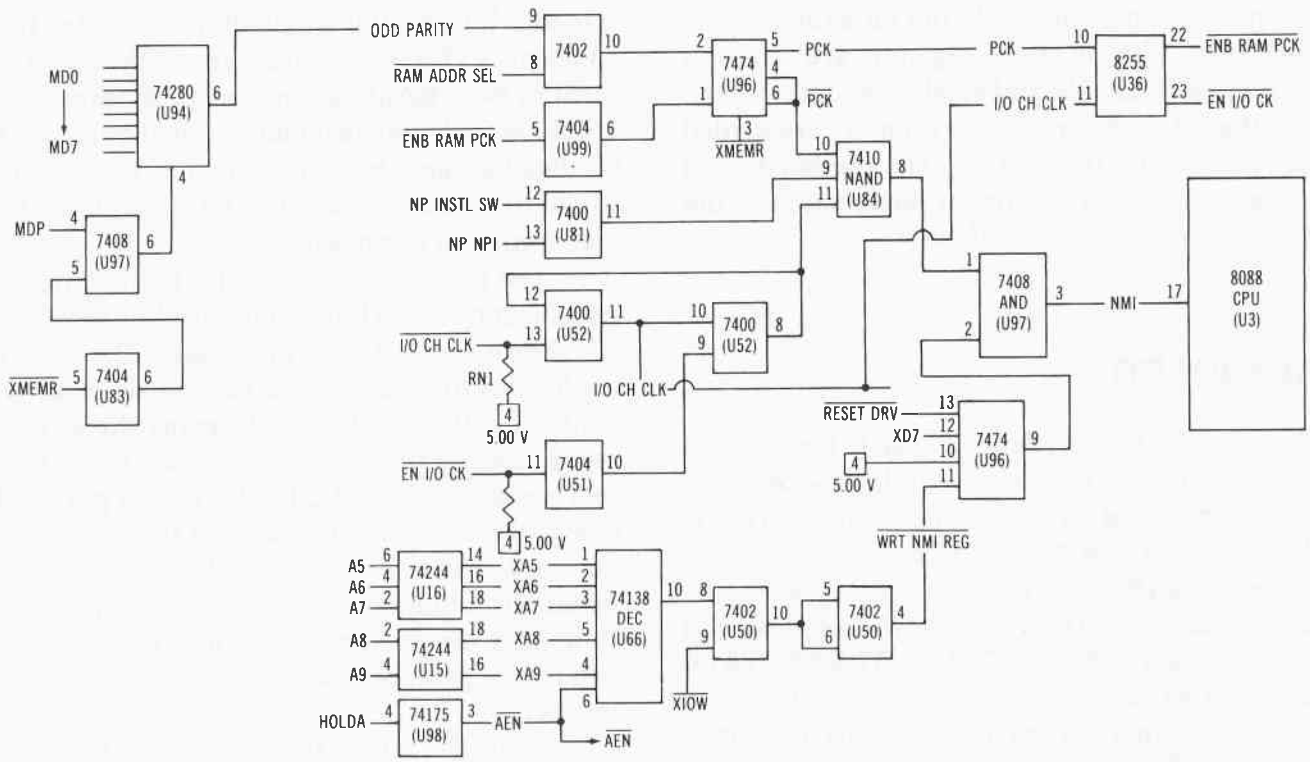


Fig. 2-55. Non-maskable interrupt (NMI) circuitry.

74LS00 2-input NAND U81 which combines NP INST SW and NP NPI on pins 12 and 13 to produce an enabling signal on pin 9 of U84. Pin 11 of U84 is enabled by output pin 8 from 74LS00 2-input NAND U52. U52 was enabled by I/O CH CLK and EN I/O CK.

The output from 74LS10 U84 pin 8 becomes one of two inputs to 74S08 AND U97. The other input (pin 2) to U97 comes from an address decoding circuitry comprised of 74LS244 tristate buffers U15 and U16, 74LS175 quad-D latch U98, 74138 Decoder U66, 7402 2-input NOR U50, and 74LS74 dual-D latch U96.

The presence of logic 10100 in address bits A5, A6, A7, A8, and A9 respectively on the inputs to the 74LS244 tristate buffers U15 and U16, with the AEN/(AEN BRD)* flip-flop in quad-D flip-flop 74LS175 reset holding (AEN)* high causes the "five-not" (5*) 74138 decoder output on pin 10 to go low enabling the other half of 74LS02 NOR (U50). This input on pin 8, and (XIOW)* active low on pin 9 causes output pin 4 to generate an active low (WRT NMI REG)* input to clock 74LS74 dual-D flip-flop U96. XD7 is latched into U96 producing an output on pin 9 that is passed to input pin 2 of 74S08 AND U97. Once enabled, 74S08 U97 output on pin 3 is a non-maskable type 2 interrupt (NMI) signal that is passed to input pin 17 of the 8088 CPU U3.

NMI is the highest priority hardware interrupt. NMI cannot be masked or disabled as can the hardware interrupts from 8259 PIT U2. CPU U3 input line 17 is edge-triggered. Therefore, to prevent spurious positive transitions on pin 17 from appearing like an NMI, this signal is held for two clock cycles to guarantee recognition by U3.

The asynchronous occurrence of NMI on pin 17 causes CPU control to transfer to an interrupt service routine defined by type 2 vector following the completion of the CPU's current instruction execution. NMI is predefined as a type 2 interrupt; therefore, the CPU is not supplied with a type code to call the NMI service procedure. U3 also does not produce INTA bus cycles in response to this signal.

During the CPU's internal acknowledgment of NMI, the current contents of the flag register are pushed onto the stack, the interrupt enable and trap bits in this register are cleared (disabling maskable and single-step interrupts), and the NMI vector address pointers are loaded into the CS and IP registers. The combination of these two registers points to the location of the NMI interrupt service routine.

KEYBOARD

Two types of keyboards are available for the IBM PC. The type 1 keyboard with its 23-row by 4-column momentary contact pushbutton array is described in the SAMS Micro Maintenance series book IBM PC Troubleshooting & Repair Guide (22358). The type 2 keyboard design is described in the SAMS COMPUTERFACTS on the IBM PC 5150. Both designs function in a similar manner. They differ in the keyboard matrix configuration and in the way an on-board microcomputer is connected to the I/O cable. Because most systems today use the type 2 keyboard, this design will be described here.

Of the 17 components inside the keyboard chassis, 4 are ICs, 1 is a capacitive key matrix, and the rest are capacitors, resistors, and an inductor. Each of the 83 keys on the board is connected to a switch matrix. Each time you depress a key, you close a switch at a crossover point on an X-row by Y-column capacitive matrix. This matrix is scanned by an on-board processor that senses the open or closed contact condition of each crossover in the matrix. The closing of a switch causes the processor to generate a bit code stream that is passed through the keyboard cable onto the system board and into the 8255 PPI (U36) which sends the data on into the 8088 CPU (U3) for interpretation.

Each key is typematic in that depressing a key causes a scan code to be generated indicating a closed (make) condition. Releasing the key produces an open (break) scan code.

The heart of the keyboard circuitry is the 40-pin Intel 8048 8-bit microcomputer on-board processor (M1) shown in the block diagram of Fig. 2-56. The 8048 is a completely self-contained 8-bit parallel single-chip computer that contains a 1K by 8-bit program ROM and a 64 word by 8-bit RAM data memory. Twenty-seven I/O lines including two bidirectional ports, an 8-bit data bus, an 8-bit timer/counter, an on-board oscillator and clock circuits complete the architecture of this machine.

The pin assignments and pin utilization of microcomputer M1 are illustrated in Fig. 2-57. As shown, not all pins are used. The chip is configured to function as a key matrix monitor/controller that continuously scans the keys to recognize key action and generate a serial code that passes out SERIAL DATA output pin 17. It contains a self-test at power-on that checks its memory, and checks for stuck keys. M1 also maintains a bidirectional serial communications flow with the system board and executes the handshake protocol required for each scan-code transfer.

Table 2-15 lists the functions associated with the pins on the 8048 keyboard single chip computer (M1). Only the principal pins that are connected in the circuit are described.

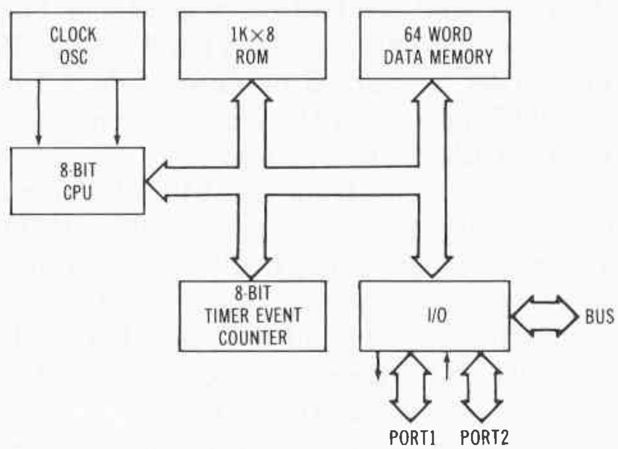


Fig. 2-56. 8048 8-bit microcomputer block diagram.

Single chip computer M1 contains an internal high gain parallel resonant circuit that uses pins 2 and 3 to connect a crystal or inductor-capacitor oscillator to generate the frequency reference for chip operation. Pin 1 is the input to the circuit amplifier stage. Pin 2 is the output of the stage. On the type 2 keyboard, a capacitor-

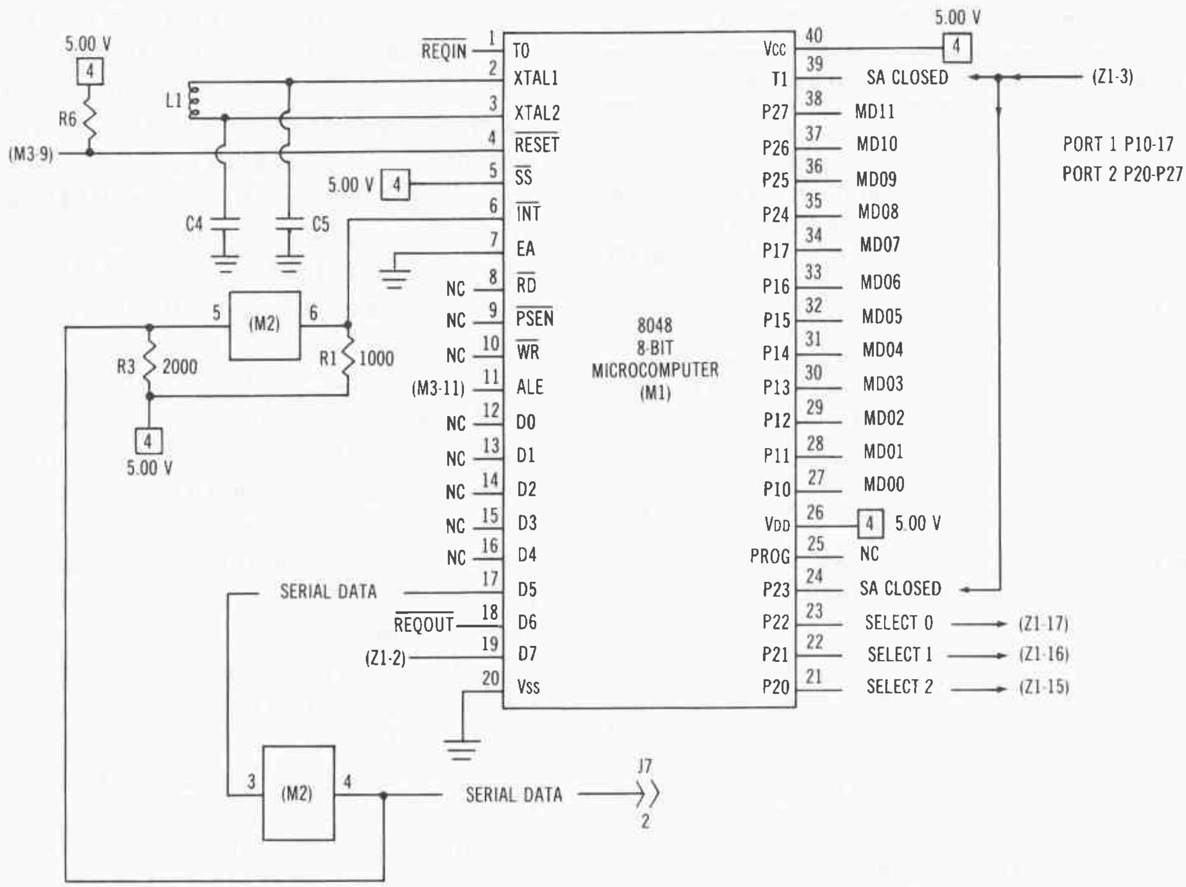


Fig. 2-57. 8048 8-bit microcomputer pin assignments.

inductor-capacitor circuit provides the feedback and phase shift required for oscillation because an accurate frequency reference and maximum (8 MHz) processor speed are not required to handle typing actions. The oscillator runs at approximately 4.77 MHz.

The output of the oscillator is divided internally by three to create a clock signal defining the state of the machine. This clock signal is made available on output pin 1 under program control. As illustrated in Fig. 2-58, the pin 1 output request in signal (REQIN*) is passed through keyboard buffer M2 onto the system board as a keyboard clock pulse used to clock the serial scan data coming out pin 17 of 8048 M1 off the keyboard circuit board onto the system board. The REQIN* clock pulse output is disabled by an address latch enable (ALE) pulse coming out pin 11 of M1. ALE is used to clock flip-flop M3, periodically resetting M1 so it can rescan the keyboard matrix.

The 12-row by 8-column keyboard capacitive matrix in Fig. 2-58 is scanned by M1 every 3 to 5 milliseconds. Twelve pins of 8048 M1 I/O ports 1 and 2 are connected to the keyboard matrix. Port 2 output pins 21, 22, and 23 form three binary weighted inputs to keyboard decoder/sense amplifier Z1. The three inputs (SELECT 0, SELECT 1, and SELECT 2) enter Z1 pins 15, 16, and 17 where they are decoded to activate a particular sense output (SENSE A through SENSE H) that connects to the keyboard capacitive matrix. The condition of the decoded sense line is returned to 8048 M1 via Z1 output pin 3 as signal SA CLOSED.

Therefore, when a key is depressed, this condition can be recognized by reading the input lines MD00 through MD11 and scanning the sense lines (SENSE A through SENSE H) to determine which intersection point is active. When a key closure is detected, the event timer program in M1 waits a few milliseconds to let the

Table 2-15. Pin Function Summary

Label	Pin(s)	Function
REQIN*	1	Request in: Active low input from buffer M2. Functions as external interrupt input. Low level on pin 1 causes subroutine jump at location 3 in program memory.
XTAL1	2	Crystal 1: One side of crystal input for internal oscillator. L1, C4, and C5 replace crystal in type 2 keyboard. Inductor L1 functions as the timing control element.
XTAL2	3	Crystal 2: Complementary side of external timing control element.
RESET*	4	Reset: Processor initialization input. The Q output from D-latch M3.
SS*	5	Single step: Tied high to keep the 8048 in the "run" mode.
INT*	6	Interrupt: Active low input from buffer M2. Initiates internal interrupt sequence.
EA	7	External access: Tied low to cause 8048 to make all memory fetches from internal memory.
ALE	11	Address latch enable: Occurs once during each cycle. Used as clock signal for D-latch (M3).
SERIAL DATA	17	Serial data: Part of bidirectional data bus. Used as output to buffer M2 to pass keyboard scan codes serially to system board.
REQOUT*	18	Request out: Active low output to buffer (M2).
SELECT 0-2	21-23	Select 0-2: Quasi-bidirectional port outputs that combine to generate a 3-bit input to 3-of-8 decoder/sense amplifier (Z1).
SA CLOSED	24	Sense amplifier closed: Active high input from sense amplifier (Z1) to indicate the closing of one of eight sense lines in the keyboard capacitive matrix. Also connected to input pin 39 (T1) to start internal event counter under program control.
MD00-MD11	27-38	Matrix data bus: 12-bit input bus connected to the keyboard capacitive matrix.
SA CLOSED	39	Sense amplifier closed: An input pin testable using 8048 instructions. Is used as the internal event counter input causing a delay before reading the matrix data bus input. This eliminates keybounce problems.

key bounce settle out and the key condition become stable before reading the MD00 through MD11 inputs. Then 8048 M1 stores the fact that a key closure has occurred in its internal RAM memory as an 8-bit scan code. If a key is held down longer than one-half second, M1 causes the same scan code to be generated ten times each second. Internal RAM enables M1 to buffer up to 16 key scan codes permitting type-ahead for the operator.

The release of a key closure is also detected by M1 causing the eighth bit (bit 7) of the scan code to be set high. This effectively produces a break code that is decimal 128 higher.

M1 also searches the array for phantom switch closures (several interconnections made and falsely encoded). If two keys are depressed causing closed switches in the same column, and one of the two rows containing a closed switch has another switch closed, a phantom switch condition has occurred. The 8048 single chip computer M1 usually ignores this condition. Only legitimate double and triple key closure operations are accepted. The scan is done in 3 to 5 milliseconds and at least 20 to 30 milliseconds pass between key entries, the matrix can be scanned at least once each keystroke and incorrect data encoding eliminated.

Each key action caused M1 to generate a unique scan code as shown in Table 2-16. A specific scan code is generated when a key is depressed and a scan code 128 higher is generated when the key is released. Depressing the Enter key causes M1 to generate the hex code 1DH (00011101 in binary). When your finger is removed from this key, 8048 M1 generates the code 9DH (10011101 in binary). Only the high bit has changed. This is the same as adding 128 to the original scan code. Once this code has been generated and passed out pin 17, the scan code signal drops to 0 (00H). Uppercase characters and special functions can be generated by depressing the Alt/Ctrl/Shift keys and one or more character keys.

When a key (or set of keys) has been depressed, M1 generates a logic high 0.2 millisecond signal that is passed out M1 pin 17 into pin 3 of the keyboard buffer (M2). The pin

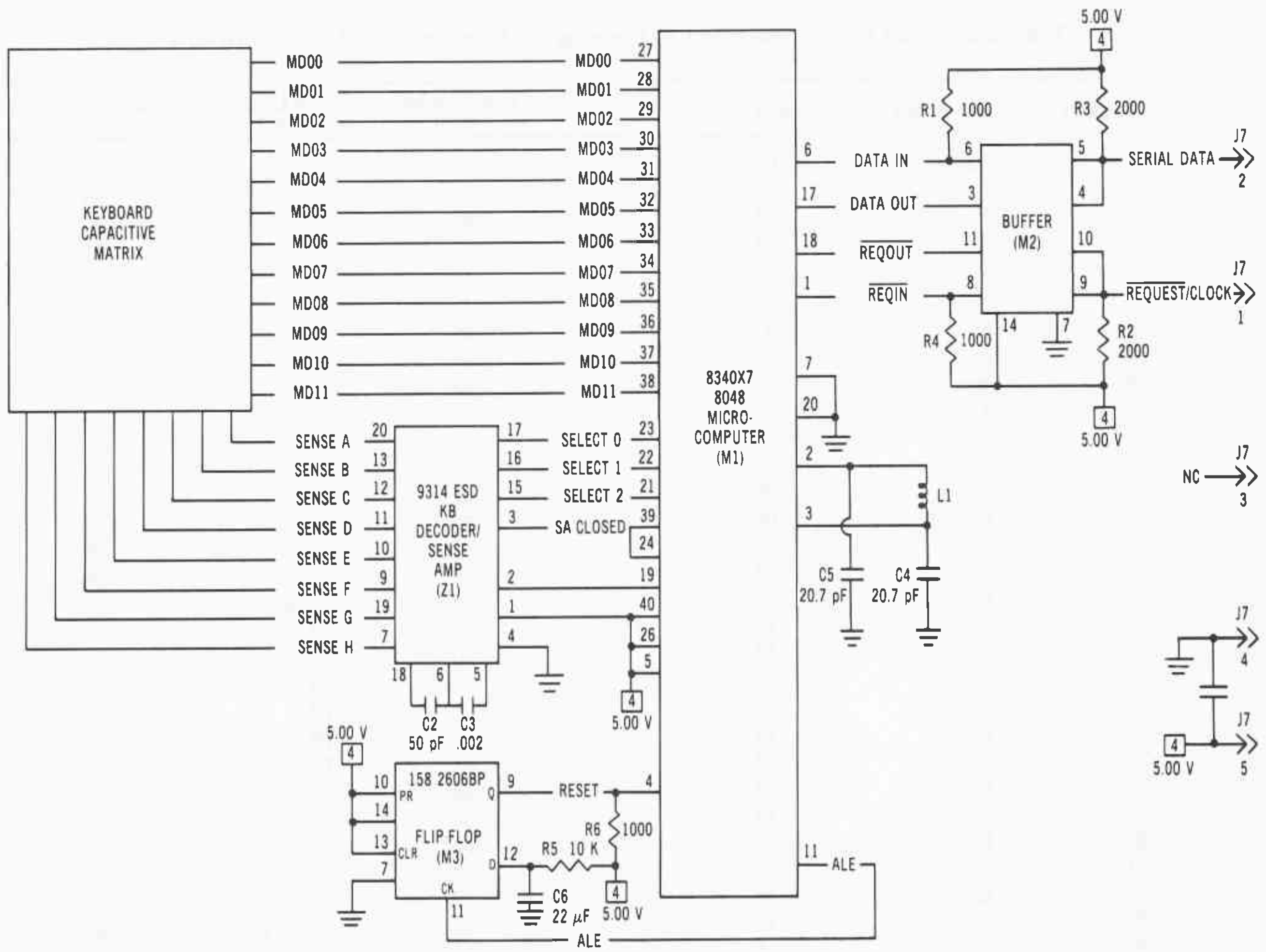


Fig. 2-58. Type 2 keyboard circuitry.

4 output of M2 notifies the system board circuitry that SERIAL DATA is coming. Then M1 clocks an 8-bit serial scan code through M2 out the keyboard and onto the system board (Fig. 2-59). This code is sent least significant bit first. Each bit is 0.1 millisecond wide.

The scan code data (SERIAL DATA) passes through the keyboard cable up to input pin 17 of 74LS322 serial/parallel buffer U24. In the meantime, 8048 M1 in the keyboard generates a request signal (REQUEST*) out pin 18 (REQOUT*) through buffer M2, out the cable and into pin 4 of 74LS175 quad-D flip-flop (U26). Flip-flop U26 is clocked by the 2.386363 MHz PCLK signal from the 8484 clock generator on the system board. The pin 6 output of U26 is a clock input on pin 11 of U24. This signal clocks the scan code data into pin 17 of U24. Pin 2 of U24 is tied high causing the chip to function in a serial-in/parallel-out configuration. Thus the scan code data is serially entered into U24 and then prepared for transmittal out as a parallel signal on the 8255 PPI (U36) port A bus (PA0 through PA7).

When the last of the 8-bit scan code has been shifted serially into U24, a signal is generated at pin 12. This signal is passed to the D input (pin 2) OF 74LS74 dual-D flip-flop (U82). On the next occurrence of a clocked output from 74LS175 quad-D flip-flop (U26) into pin 3 of U82, passing the state of U82 out its Q (pin 5), and Q* (pin 6) outputs. The Q* output becomes an enable signal to 74LS125 quad 3-state buffer (U80) pulling the keyboard SERIAL DATA in line low. The Q output becomes an interrupt request 1 (IRQ1) signal that enables the parallel output register of 74LS322 buffer (U24) so the 8255 PPI (U36) port A can receive

Table 2-16. Scan Codes Generated by Pressing the Keys on the IBM PC Keyboard

Key Number	Key Label	Scan Code	Key Number "cont."	Key Label "cont."	Scan Code "cont."
1	Escape	01			
2	1	02	43	\	2B
3	2	03	44	z	2C
4	3	04	45	x	2D
5	4	05	46	c	2E
6	5	06	47	v	2F
7	6	07	48	b	30
8	7	08	49	n	31
9	8	09	50	m	32
10	9	0A	51	<	33
11	0	0B	52	>	34
12	-	0C	53	/	35
13	=	0D	54	Shift	36
14	Backspace	0E	55	Pt Sc	37
15	Tab	0F	56	Alt	38
16	q	10	57	Space	39
17	w	11	58	Caps Lock	3A
18	e	12	59	F1	3B
19	r	13	60	F2	3C
20	t	14	61	F3	3D
21	y	15	62	F4	3E
22	u	16	63	F5	3F
23	i	17	64	F6	40
24	o	18	65	F7	41
25	p	19	66	F8	42
26	[	1A	67	F9	43
27	]	1B	68	F10	44
28	Enter	1C	69	Num Lock	45
29	Ctrl	1D	70	Scroll Lock	46
30	a	1E	71	7	47
31	s	1F	72	8	48
32	d	20	73	9	49
33	f	21	74	-	4A
34	g	22	75	4	4B
35	h	23	76	5	4C
36	j	24	77	6	4D
37	k	25	78	+	4E
38	l	26	79	1	4F
39	;	27	80	2	50
40	'	28	81	3	51
41	`	29	82	0	52
42	Shift	2A	83	Del	53

PA0 through PA7. IRQ1 is also passed to pin 19 of the 8259 programmable interrupt controller (U2).

Upon receipt of the IRQ1 interrupt request, U2 generates an interrupt signal (INT) that alerts the 8088 CPU (U3) that an external device wishes to communicate with it. (This process was covered in the section on interrupts.) CPU U3 halts what it is doing and responds by passing a code out its S0 through S2 lines into the 8288 bus controller (U6). U6 reacts by generating an interrupt acknowledge (INTA) that is passed back to U2. As described in the section on interrupts, a second INTA is generated causing the 8259 (U2) to place an interrupt code (INT 9) on the system data bus.

The 8088 CPU (U3) reads the data bus and calls the INT 9 subroutine in the ROM-based operating system. INT 9 causes the scan code to be read into port A (PA0 through PA7) of U36

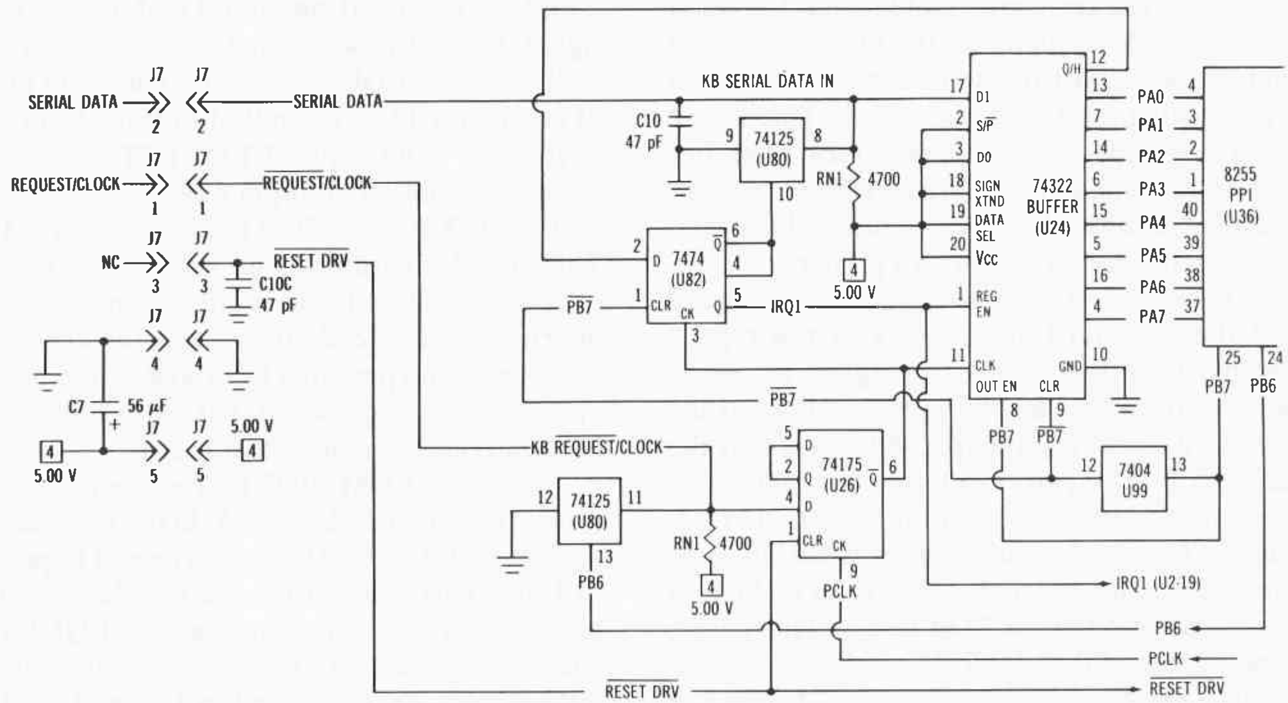


Fig. 2-59. System board keyboard interface.

and on into the 8088 CPU (U3). The scan code is converted by U3 into an ASCII code for the character selected. An ASCII conversion chart can be found in Appendix G. The 8-bit scan code and the 8-bit ASCII character code are stored in 32 consecutive locations of a 16-character circular RAM buffer. INT 9 also clears the interrupt request by causing the PPI (U36) to generate an active high PB7 signal out pin 25 of U36 where it gets inverted by 74LS04 hex inverter (U99) to produce PB7*. This active low signal clears the 74LS74 dual-D flip-flop (U82) removing the IRQ1 active high signal so another interrupt can occur.

The ASCII character and the scan code are combined as two bytes per character with the low byte representing the encoded character and the high byte the keyboard scan code. For example, the ASCII code for lowercase "a" is 097 decimal (61H). The scan code generated when "a" is depressed is 1EH. Therefore, the keyboard buffer in RAM contains 611EH (0110 0001 0001 1110 in binary). Special keys such as a function key or numeric keypad key usually have the scan code in the high byte and all zeroes in the low byte. The buffer content for depressing function key F1 (key position 59) would, therefore, be 3BH yielding a buffer code 3B00H.

Keystrokes are captured and translated by the basic input/output system code (BIOS) stored in the ROM chips on the system board. The system's ROM BIOS produces an INT 16 interrupt causing the ASCII and scan codes to be read out of the RAM buffer. INT 16 causes the operating system software to execute a keyboard I/O routine. This routine reads through the keyboard buffer until it finds a character code. The value of this 16-bit word is read into the 8088 (U1) accumulator register (AX). The scan code stays in the upper byte (AH). If this byte is all zeroes, a noncharacter key has been pressed. The program then reads the status of the data to determine if any special keys such as Ctrl, Alt, or Shift were depressed. The ASCII character code is passed to the calling program which uses the character in a software code character string or data input while the BIOS continues its program execution, passing the character to an active output device (screen or printer) to complete the operator-machine-operator interaction or uses it internally as a special password.

Some keys, or key combinations, are directly affected by the ROM BIOS. The Alt key can be used to directly enter ASCII character codes from the keyboard. Holding this key down and typing three digits on the numeric keypad enables the ROM BIOS to recognize the input as representing an ASCII character. This is one way to generate graphic characters. Another built-in function key is */Prtsc. Depressing shift and */Prtsc causes the BIOS to print all the characters on the display screen on a printer.

Communication between the system board and the keyboard also occurs in the type 2 keyboard configuration. Two signals are generated by the ROM BIOS to reset or to clear the keyboard circuitry. Figure 2-60 shows that the 8255 PPI (U36) is used to send software-generated commands from the 8088 CPU (U3) into the keyboard circuitry. Port B of U36 is the gateway for these signals. Port B bit 6 (PB6) is connected between pin 24 of U36 and the enable input pin (pin 13) of 74LS125 quad 3-state buffer (U80). Pin 25 of U36 connects PB7 to pin 8 of 74LS322 serial-to-parallel shift register (U24), and to pin 13 of 74LS04 hex inverter (U99).

One section of code in the ROM BIOS causes the binary code 0 0 0 0 1 1 0 0 (hex 0CH) to be placed in the lower 8 bits of the 8088 CPU accumulator register (AL). The contents of AL are then passed to port B of U36. Then, PB6 and PB7 are both zero. The low PB6 output from pin 24 of U36 enables U80 generating an active low REQUEST* signal out pin 11 of U80. This signal holds the keyboard clock low for 20 milliseconds. REQUEST* is also passed to pin 1 of connector J7 into pin 9 of buffer M2 in the keyboard. The input REQUEST* signal is relabelled REQIN* out pin 8 of M2 and passed into pin 1 (T0) of the 8048 microcomputer (M1). This signal functions as an external interrupt causing the 8048 to do a subroutine jump to internal program code that resets the keyboard electronics and prepares it for key action by the operator. Scan code AAH is returned to the 8088 CPU (U3) on the system board.

Another ROM BIOS subroutine places the code 1 1 0 0 1 1 0 0 (hex CCH) in the internal AL register of U3. The AL is again passed to port B of U36. This brings PB6 and PB7 both active high. Buffer U80 is not enabled so REQUEST* CLOCK is held high. However, the high signal out PB7 (pin 25) is inverted by U99 and used to clear 74LS74 dual D latch (U82). This brings the Q* output (pin 6) of U82 low enabling a section of 74LS125 quad 3-state buffer (U80) passing a low signal out pin 8 through pin 2 of connector J7 and into pin 5 of buffer M2 in the keyboard. This low becomes the CLEAR DATA signal that enters pin 6 (INT*) of 8048 microcomputer (M1). Active low on pin 6 causes M1 to generate an internal interrupt clearing the keyboard.

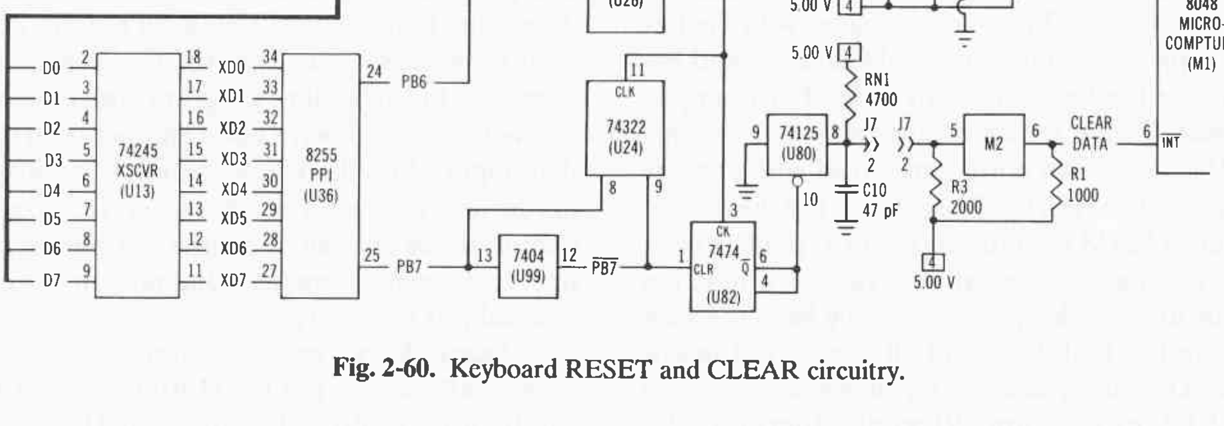


Fig. 2-60. Keyboard RESET and CLEAR circuitry.

8087 NUMERIC PROCESSOR EXTENSION (NPX)

The 8088 CPU in the IBM PC is designed for general data processing applications requiring fast, efficient data movement and control instructions. The arithmetic performed in this microprocessor is simple. However, the PC is being used in many engineering, scientific, and business batch processing applications. These environments require more powerful arithmetic instructions and data types and deal with fractional values, sine, cosine, logarithms, and square roots. The results of complex operations require extreme accuracies and rapid calculations. The Intel 8087 numeric processor extension (NPX) was designed to support these operations while residing in the same circuitry as the 8088 CPU. Both the hardware and the software interfaces for the 8087 are compatible with the 8088.

The 8087 NPX is ideal for number crunching applications. It can handle numeric data over a wide range of values including integer and noninteger values. The 8087 can produce very precise results with a large number of significant digits. It can also handle calculations involving real and imaginary numbers. Integers up to 18 digits long and floating point numbers from 16 to 80 bits wide can be used in this machine. The 8087 can respond to built-in math instructions for add, subtract, multiply, divide, absolute value, arctangent, tangent, square root, log base two and log base e.

A prewired 40-pin socket is mounted on the system board to hold an optional 8087 NPX. With the 8088 CPU configured in maximum mode, the 8087 NPX shares the multiplexed address/data bus, S0 through S2 status signals, queue status signals, ready status signals, clock, and reset. The pin assignments for the 8087 NPX are shown in Fig. 2-61. Two output signals, test (TEST*) and numeric processor numeric processor interrupt (NP NPI) on pins 23 and 32 respectively are used to inform the CPU of NPX internal status. The corresponding Intel labels are BUSY and INT. To ensure that the 8088 CPU always sees a "not busy" status if no 8087 NPX is installed, the input to CPU U3 is connected to the 5 volt supply through a 4700 ohm resistor in resistor network RN1.

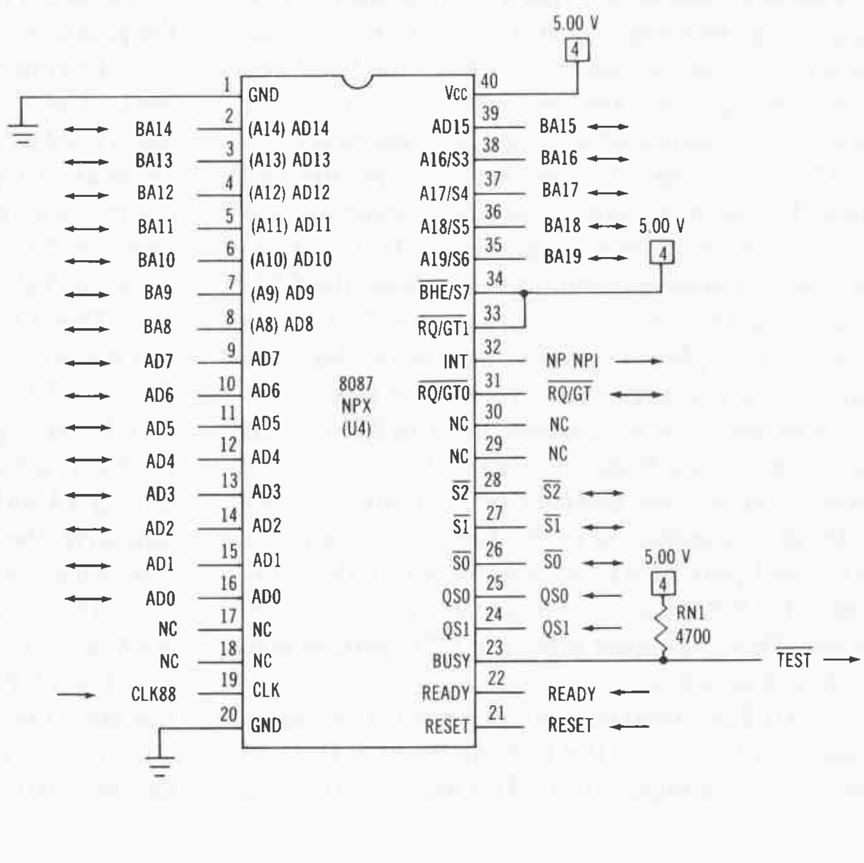


Fig. 2-61. 8087 Numeric processor extension (NPX) pin assignments.

The TEST* (BUSY) signal is designed as an active high signal to tell the CPU that the NPX is executing a numeric instruction. The TEST* input to pin 23 of the CPU is designed as a test input that is sampled by a wait instruction. If the input is low, CPU execution continues, otherwise the 8088 goes into an idle state. The Intel hardware reference manual on the 8087/8088 suggests installing a 10K pull-down resistor on the BUSY/TEST signal line between the NPX and the CPU sockets to ensure that the CPU always sees a "not busy" status if no 8087 is installed on the system board. With the 4.7K pull-up resistor on the IBM PC system board, and no 8087 NPX installed, a CPU wait instruction will interpret the active high input on pin 23 as an indication that a numeric instruction is in process within a (phantom) coprocessor. This will cause the CPU to enter an idle state forever. Therefore, a wait instruction should not be used unless an 8087 NPX is actually installed in the system.

The 8087 NPX is designed to sit idle and monitor the 8088 CPU instructions. Both the CPU and the NPX decode the same instructions. Only the CPU can respond to CPU instructions. A numeric instruction that requires 8087 action appears as an escape (ESC) instruction. As soon as an ESC instruction occurs, both the 8087 and the 8088 decode and execute it. A numeric operation begins when the CPU executes the ESC instruction. The NPX monitors this and looks for the next byte of the ESC instruction and acts on this coded command. If the ESC instruction involves memory references, the CPU calculates the effective address specified in the instruction, places the address on the bus and initiates a memory read cycle. The 8088 CPU ignores the data it receives, but the 8087 reads the data coming from memory and completes the execution of the instruction. If no memory reference is indicated in the ESC instruction, the NPX will pull TEST* active low idling the CPU until the NPX numeric instruction is complete. When TEST* returns high, the CPU proceeds to its next instruction.

All ESC instructions begin with the most significant 5 bits of the high order byte (bits 11 through 15) a logic 11011. The most significant 2 bits of the low order byte (bits 6 and 7) define the addressing mode and the number of bytes remaining in the instruction. The nonmemory form of ESC causes specific coprocessor activity based on the nine remaining bits. The 8088 CPU ESC instructions provide 64 memory reference opcodes and 512 nonmemory reference opcodes. The 8087 NPX can respond to 57 of the memory reference opcodes and 406 of the nonmemory reference opcodes.

Coprocessor instructions are labelled beginning with F for "Floating point." Therefore, FMUL represents a floating point multiplication instruction.

To ensure that the 8087 is finished with its operation before the CPU should fetch and execute the next instruction in the program, a wait instruction precedes the ESC. If the 8088 must wait for the 8087 to complete storing data in memory before CPU operations can continue, the programmer places another wait instruction in the code just after the ESC instruction. In this way, the wait and ESC instructions work together to enable CPU and NPX operations on the same system board hardware.

Table 2-17 describes the signals connected to the pins of 8087 NPX (U4).

During operations when the CPU (U3) has control of the bus, the eight status line signals described in the section on the 8088 CPU are generated by U3. During NPX bus control operations, only five combinations of the status lines (S0* through S2*) signals are encoded, as shown in Table 2-18.

These status signals are driven active during bus machine cycle T4. They remain valid during T1 and T2, and they shift to a passive state (1,1,1) during clock tick T3 or during TW when READY is high. Any change in S2*, S1*, or S0* during T4 indicates the beginning of a bus cycle. Similarly, the return to the passive state in T3 or TW marks the end of a bus cycle.

The primary interfaces between the 8087 NPX and the 8088 CPU are shown in Fig. 2-62. The 8088 CPU (U3) and 8087 NPX (U4) fetch the same instructions and bytes of the instruction stream. This allows the 8087 to monitor and decode instructions synchronously with the 8088

Table 2-17. Pin Signal Descriptions

Label	Pin(s)	Type	Name and Function
BA15-BA7	2-8, 39	I/O	Buffer address: The time multiplexed high order memory address byte.
AD7-AD0	9-16	I/O	Address bus: The time multiplexed low order memory address byte.
BA19-BA16	35-38	I/O	Buffered address: Address lines during T1 of memory operations. Input lines to monitor the 8088 when it has control of the bus.
CLK88	19	I	Clock 88: A 4.772727 MHz asymmetric 33% duty cycle clock to provide optimized internal timing for the processor and bus controller.
RESET	21	I	Reset: An internally synchronized signal that causes NPX to end present activity. Must be high for at least four clock cycles.
READY	22	I	Ready: Active high acknowledgment from addressed memory device that it will complete data transfer. READY is synchronized by 8284 clock generator (U11).
TEST*	23	O	Test: When active high, indicates to 8088 (U3) that 8087 NPX is executing numeric instruction. When TEST* is low, U4 is idle.
QS0, QS1	24, 25	I	Queue status 0, 1: Status inputs from 8088 CPU to allow 8087 NPX to track CPU instruction queue.
S2*-S0*	26-28	I/O	Monitor inputs when 8088 has control of bus. Status outputs when 8087 is in control.
RQ*/GT*	31	I/O	Request/grant: Used by 8087 to request the local bus. 8088 CPU generates grant and release pulses.
NP NPI	32	I	Numeric processor interrupt: An active high output signal used to indicate that an unmasked exception has occurred during numeric instruction execution when 8087 interrupts are enabled. This signal is routed to the NMI circuitry.

CPU without introducing any CPU overhead. Thus, U4 knows at all times what instruction was just fetched into U3. The NPX and CPU instructions can be mixed in the program instruction stream. And the 8087 NPX can process instructions in parallel with and independent of the 8088 CPU.

Table 2-18. 8087 NPX Bus Cycle Status Line Encoding

S2*	S1*	S0*	Function
0	X	X	Unused
1	0	0	Unused
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive

When the 8087 is executing a numeric instruction, the TEST* line (pin 23) is used to resynchronize the system. The 8088 WAIT instruction tests the TEST* input to determine when the NPX can execute later instructions.

The NPX (U4) maintains an instruction queue that is identical to the CPU. Its queue length is automatically set to match that of the CPU by the continuously active high input on pin 34 (BHE*/S7 in Fig. 2-61). Therefore, immediately after reset, the queue length in U3 and U4 are identical.

To help coprocessor U4 in monitoring the CPU operations, nine status lines are connected between the 8087 and 8088 machines (QS0, QS1, and S0* through S6* as shown in Fig. 2-61). The QS0 and QS1 inputs on U4 pins 25 and 24 respectively are used to monitor the CPU and enable the NPX to obtain and decode instructions synchronously. Table 2-19 describes the decoded meaning for the combination QS0 and QS1 inputs from CPU (U3).

Table 2-19. QS0-QS1 Code Definitions

QS1	QS0	Description of CPU Status
0	0	No operation
0	1	First byte of op code from queue
1	0	Empty the queue
1	1	Next byte from queue

Notice that the status signals S0* through S2* are also passed to the 8288 bus controller (U6) in the lower right of Fig. 2-62 to generate the memory and I/O access commands, and to the 74530 8-Input NAND (U5) where they combine with the LOCK* signal from U3 and generate an output for the HOLDA circuitry. HOLDA is used by the 8237 DMA controller (pin 7 on U35) and by 74LS175 quad D-latch (U98) which generates the AEN* and AEN BRD signals described earlier in the chapter.

The 8087 NPX (U4) can interrupt CPU (U3) whenever it detects an error or exception. If an incorrect instruction is sent to U4, such as a command to load a full register, or to divide a number by zero, U4 can signal the CPU (U3) via an interrupt. The 8087 interrupt circuitry is shown in Fig. 2-63.

Without an 8087 NPX installed in socket U4, switch SW1 position 2 is opened (OFF position) pulling the pin 12 input to 74LS00 quad 2-input NAND gate (U81) high. When an 8087 NPX is installed in the system, SW1-2 is closed (ON position) grounding the pin 12 input to U81. The other input to U81 is the NP NPI line from the empty 8087 NPX (U4) socket. NAND gate U81 output (pin 11) connects to one of the three inputs to 74LS10 triple 3-input NAND gate (U84). The pin 10 input to U84 comes from the Q* (pin 6) output from 74LS74 dual D-latch (U96). On the positive edge transition of the pin 3 clock input XMEMR*, U96 latches the D input (pin 2) into the flip-flop. Pin 2 connects to the output (pin 10) of 74LS02 quad 2-input NOR gate (U27). The pin 8 and 9 inputs to U27 are (RAM ADDR SEL)* and the EVEN parity output from pin 6 of the 74LS280 parity generator/checker (U94).

The third input to the 74LS10 triple 3-input NAND gate (U84) comes from pin 8 of 74LS00 quad 2-input NAND gate (U52). U52 is enabled

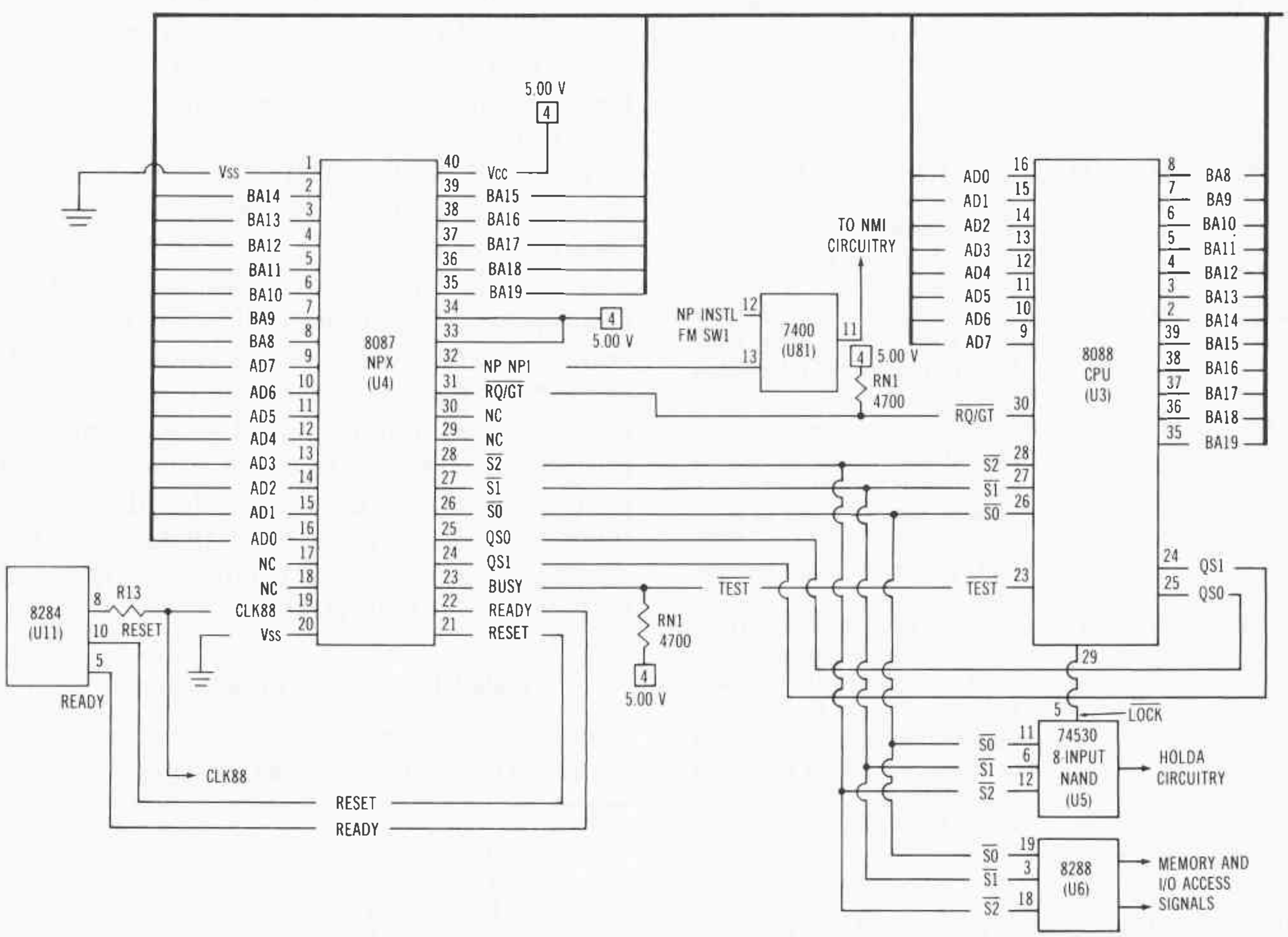


Fig. 2-62. 8087 NPX (U4) and 8088 CPU (U3) interface circuitry.

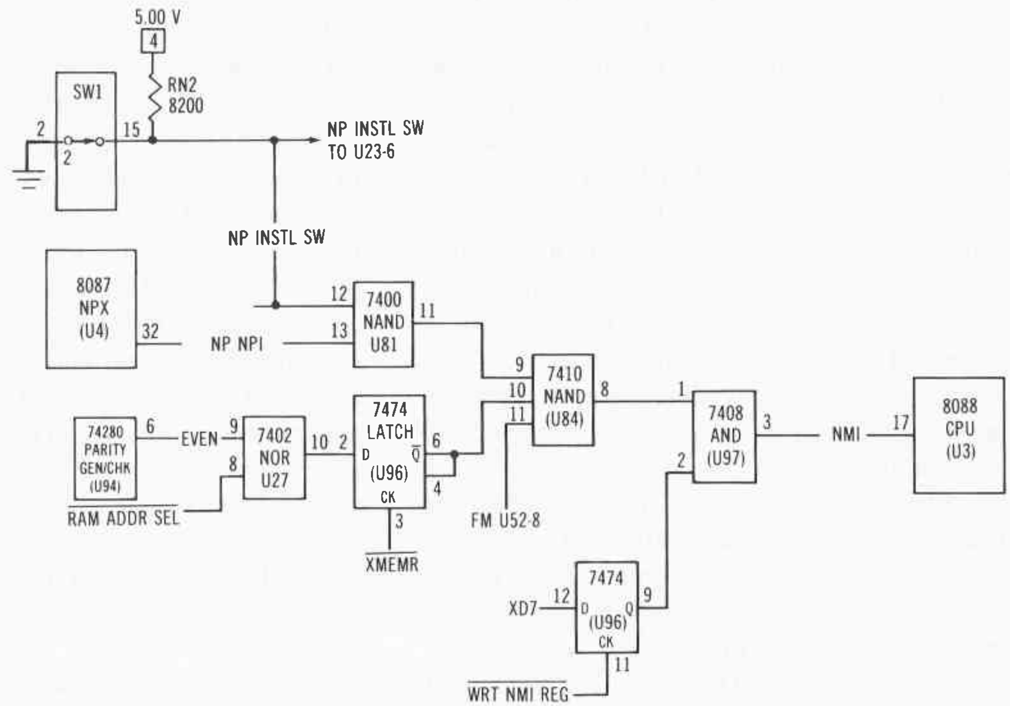


Fig. 2-63. 8087 NPX (U4) interrupt circuitry.

by I/O CH CLK and EN I/O CK. The pin 8 output from U84 becomes an input (pin 1) to 74LS08 quad 2-input AND gate (U97). The other input to U97 (pin 2) is the Q output from the other half of 74LS74 quad D-latch (U96). This flip-flop follows the XD7 input (pin 12) whenever (WRT NMI REG)* transitions from active low to high. The ANDed output from U97 (pin 3) is the non-maskable interrupt (NMI) described earlier in the chapter. NMI is passed directly into pin 17 of the 8088 CPU (U3).

With an 8087 NPX installed in socket U4, only three conditions will prevent an interrupt from occurring once interrupt conditions exist inside U4.

1. Certain bits in the 8087 control word (exception and interrupt enable) are set high.
2. System board switch SW1-2 is closed (ON position).
3. The 74LS74 NMI mask register (U96) is set to ONE.

U96 is cleared at power-up to disable NMI. Once quiescent conditions are met in the system circuitry, U96 is free to be set by clocking (WRT NMI REG)* on pin 11 to place the logic condition of XD7 in the U96 flip-flop.

Intermittent 8087 System Performance Problems

The 8087 NPX draws 0.457 milliamp of current and dissipates up to 3 watts. This can create two related problems: increased heating inside the chassis, and excessive circuit power consumption. If the system has several power-hungry expansion boards, the standard 67.5 watt power supply can be stressed worsening the heat problem. These thermal management issues can cause intermittent CPU lockup, power-on self test failures, suspicious RAM memory malfunctions, unreliable disk drive write operations, and even power supply failure. Additional cooling and/or increased power supply capability may be required to prevent 8087-caused system failures.

VIDEO

Three types of video signals are produced on interface boards plugged into expansion slots in the PC system board. One signal is NTSC composite video comprised of horizontal and vertical syncronization signals combined with the video information. For a color display, the composite signal has color information phase and amplitude modulated as a 3.579 MHz subcarrier superimposed on the standard composite video. A second type of video is an RF amplitude modulated signal that can drive a standard television receiver. The third type signal is comprised of discrete video and synchronization signals that can directly drive a special IBM display monitor. All three of these signals will be described in this section.

A video screen image is generated as thousands of tiny picture elements (pixels) arranged in neat rows and columns. Each row is called a "raster," and each column position in a raster is called a "pixel" or "dot."

Each display unit (monitor or television) has a cathode ray tube (CRT) inside. The face of the CRT is what you observe when you look at a display screen. A beam of electrons from the inside rear of the cathode ray tube (CRT) inside the display unit scans across the screen under control of a horizontal sawtooth wave signal. As the beam moves across the screen, its intensity may increase momentarily as it passes over specific pixel positions on the screen. Upon reaching one side of the screen, the electron beam is essentially stopped and the focus point is retraced back to its original column. However, a second control signal is applied to vertical deflection plates inside the CRT to move the beam down one row. Therefore, the beam is moved horizontally by a horizontal sweep signal, blanked out during retrace, and shifted vertically down a raster by the vertical sweep signal. When the last raster row has been traced, the beam is blanked and the CRT focus returned to the upper left corner of the display area.

The inside of the CRT screen is coated with a material that glows when hit by high intensity electron beams. The increased intensity dots form patterns on the screen that we recognize as characters or graphic shapes. The pattern of intensity is determined by a sequence of binary values generated within the adapter board connected to the PC system board. These binary values are synchronized to the horizontal and vertical sweep frequencies of the display and are transmitted to the display unit via one of several video connectors on the board. Each logic high in the dot pattern causes a particular pixel position on the inside of the CRT screen to receive a high intensity beam of electrons from the CRT gun. Raster displays of picture or text are produced when this beam of electrons is repeatedly scanned across the inside surface of the CRT screen to form a pattern of closely spaced horizontal lines (the raster) which covers the entire screen. The inside surface of the screen is covered with a phosphor that glows when the electron beam hits it, so pictures are formed as the beam turns on and off while scanning along each raster line on the screen surface.

The number of raster lines and dot pixels on each raster defines the resolution of the display. The more raster rows and the more pixels per raster, the higher the resolution.

All the video signals required by the display monitor are produced on external interface boards. Address, data, and control signals are passed from the system board onto the expansion bus backplane and into one of many types of video display boards designed for the IBM PC. Only one video adapter board is required, although one can use a color and a black-and-white display board in the same system to provide flexibility. The two display boards produced by IBM are the monochrome monitor/printer adapter and the color/graphics monitor adapter. Because non-IBM display boards are also available, this text only provides an overview of the IBM monochrome and color/adapter cards. The ideas described for these two boards apply to the adapters provided by other companies.

The IBM monochrome display/printer adapter can produce 350 raster lines of vertical resolution. Each raster line has 720 dots of horizontal resolution. The IBM color/graphics monitor adapter can produce 200 raster lines of vertical resolution and 640 dots of horizontal resolution. These pixel specifications define a screen matrix area 350 x 720 or 200 x 640 dots in size. Each of these matrices can easily fit within the 525 lines of horizontal resolution in a standard television receiver.

Synchronization signals sent to the display unit control horizontal and vertical sweep oscillators that electrically make the CRT electron beam scan across the screen. Horizontal sync pulses lock the picture horizontally to the incoming signal. Vertical sync pulses perform a similar role in the vertical circuitry of the display unit and prevent the display picture from rolling in a vertical direction.

Coarse and fine adjustments control the relationship of the video dot pattern information to the horizontal and vertical sweep of the CRT gun. Coarse adjustment is made using the horizontal and vertical hold controls on the outside of the monitor. These controls affect the oscillation frequencies of the CRT electron beam circuits. Fine adjustment is accomplished using horizontal and vertical sync signals passed with the video dot pattern information to the display unit from the adapter board.

Video monitors have wider signal bandwidths (10 to 20 MHz) than a standard television (4.5 MHz) so they can display small details clearly. In a standard television, the horizontal sweep frequency is 15,750 Hz, so each scan line requires about 53.5 microseconds plus 10 microseconds for the horizontal retrace. The vertical sweep frequency is 60 Hz, which allows 262.5 horizontal scan lines during one vertical sweep period. It takes 16.7 milliseconds (one-sixtieth of a second) to scan the entire screen area once (this is called one field), and 60 fields are displayed per second. Only about 245 of the horizontal lines are visible on the screen, however, since 1.25 milliseconds is required for the vertical retrace that brings the beam back to the top of the screen after a field has been completed.

The IBM monochrome display monitor uses a higher than normal 18.432 kHz horizontal sweep frequency and a lower than normal 50 Hz vertical sweep frequency so 350 raster lines can be traced within one complete scan of the screen. The monochrome adapter produces 720 dots for each horizontal raster line to obtain the 80 characters per row. These dots must be transmitted from the adapter board to the display unit during the time required to scan a single raster line. This places severe performance requirements on the circuitry in the display and the adapter. The dot transmission rate requires a video bandwidth of more than 16 MHz for the video amplifiers in the display. Because of the high bandwidth and nonstandard sweep rates, only IBM monitors and a few non-IBM monitors can be used with the monochrome adapter card. The monochrome adapter card provides a single direct drive video interface to the display unit.

The color monitor used with the PC (color/graphics card installed) has a horizontal sweep rate of 15.74 kHz and a vertical drive frequency of 60 Hz. This enables up to 640 pixels and 200 rows of display dots with a video band-width of 14 MHz. The color/graphics adapter card provides direct drive RGB video for high resolution monitors and composite video for low resolution (monochrome or color) monitors and a television receiver via an RF modulator connection.

The characters (numbers and letters) or shapes that are drawn on a computer display are generated by turning on or off an electron beam in the display unit as the beam sweeps (scans) across each raster line producing a pattern of bright dots on the screen. The characters or graphic shapes are represented by closely spaced dot patterns that are drawn one raster line at a time.

The generation of color video works the same way as monochrome except that, with color, three electron beams are used and the phosphor screen is coated with a pattern of circular or rectangular dots arranged in a three-pixel configuration. One of the three dots glows red when hit by an electron beam, another dot glows green, and the third dot glows blue.

Characters are produced in a fixed matrix within the dot array of the complete screen. The monochrome display adapter produces letters within a 7 by 9 dot matrix contained within a 9 by 14 character box. The extra lines (rows) and columns of dots allow room for descenders and for intercharacter and interline spacings.

Monochrome and color video are produced in different ways, but each type of IBM display adapter uses a Motorola 6845 CRT controller (CRTC). The 6845 CRTC will be described in the section on the monochrome monitor/printer adapter. Its operation is similar on the color/graphics adapter card. Refer to COMPUTERFACTS CSCS2-A for this discussion.

Monochrome Monitor/Printer Adapter

The monochrome monitor/printer adapter generates black-and-white video and printer signals on a common circuit card. This text will cover the video portion of the board only. The direct drive video output from a 9-pin D-connector at the rear of the card produces 720 dots of horizontal raster lines on a connected monochrome display monitor. The vertical sweep frequency generates 350 raster lines on the display. This enables a 25-row display with 80 characters per row.

The adapter generates video characters only. No graphics are produced on this board. Each character is produced as a 7 by 9 dot matrix within a 9 by 14 dot array. The extra dots around the character provide spacing between characters and lines and provide room for letters with descenders (such as the letter g).

As described earlier, the horizontal and vertical sweep frequencies generated on this adapter card are not standard. A higher-than-normal video bandwidth requirement and nonstandard sweep rates limit the display options to few monitors except the IBM product. In addition, the video output is not a composite signal with the horizontal and vertical sync signals combined with the video dot pattern. Instead, the signals present on the pins of the output connector provide direct drive video as shown in Fig. 2-64. The video is comprised of separate sync signals, a video dot pattern signal, and an intensity signal that can produce bright, boldface letters. The "custom" video output configuration reduces the video display unit selection.

6845 CRT Controller (CRTC)

The 6845 CRT Controller (U35 in folder CSCS2-A) is an LSI component designed to provide an interface for the 8088 CPU to a raster scan CRT display. The primary function of the 6845 is to generate timing signals necessary for raster scan displays under the control of the 8088. The design of U35 places keyboard functions such as cursor movements, editing, and read/write under control of the system board CPU (U3) while providing the video timing and refresh memory addressing signals. U35 is fully programmable via the 8088 data bus. Under software control it generates a variety of character widths, display modes, and graphic shapes.

The chip can be programmed to generate a fixed height cursor, blinking characters, and interlace or noninterlace scan. The noninterlace scan is used in the IBM PC display system. As shown in Fig. 2-65, U35 is a 40-pin compact IC. Eleven of the 14 refresh memory address lines are used in the IBM PC design. Four pins are used to generate an address into the character generator (U33). The 8-bit data bus is buffered off the expansion board backplane into U35 as buffered data bits BD0 through BD7. A reset pulse is applied on pin 2. On the lower right of Fig. 2-65, five control inputs are used to select, enable, and clock the chip. Besides the refresh memory address and character generator row address outputs, U35 generates a horizontal and vertical sync, cursor, and display enable signals.

Table 2-20 describes the functions of each data, address, or control pin of CRTC U35.

The monochrome display/printer adapter and the color/graphics monitor adapter boards are both designed around the 6845 CRT controller (CRTC). A block diagram of this chip is shown in Fig. 2-66. The 6845 CRTC control chip is used to generate refresh addresses over MA0 through MA10, character generator raster addresses over RA0 through RA3, a display enable, and video monitor timing signals HSYNC and VSYNC. The 6845 CRTC also has an internal register that generates an output CURSOR signal whenever its contents match that of the current refresh address. A light pen

Table 2-20. 6845 Pin Description

Signal	Pin	I/O	Function
VSS	1	I	Ground
RESET*	2	I	RESET* Active low input that clears all internal counters and stops display operation. Forces all outputs except the data bus to a low condition. Does not affect internal control registers.
LPSTB	3	I	Light pen strobe: High impedance input that is synchronized by the clock input on pin 21 to latch current refresh memory address (MA0-MA13) in 14-bit light pen register on the low to high transition of a strobe pulse detected by the light pen and control circuit.
MA0-MA10	4-14	O	Memory address (refresh): Active high outputs that enable 2K words of refresh memory (one 2000 character screen). (NOTE: MA11-MA13–pins 15 through 17 are not used.)
DISPEN	18	O	Display enable: Active high signal indicating the CRTC is providing addressing in the active display area. This signal defines the display period in horizontal and vertical raster scanning. The video signal is enabled only when DISPEN is high.
CURSOR	19	O	Cursor: Active high signal that is mixed with the video signal to produce a cursor display on the CRT screen.
CCLK*	21	I	Character clock: Input signal that defines character timing for CRTC display operation. Used to synchronize all CRT control signals on high to low transition.
XIOW*	22	I	Buffered I/O Write: High impedance input that controls the direction of data transfer between the CRTC internal register file and the 8088 CPU. Active high enables 8088 CPU read from CRTC. Active low enables CPU write into CRTC.
6845E	23	I	6845 (CRTC) enable: High impedance active high input that enables the data bus I/O buffers and clocks data into/from the CRTC internal registers. Signal is derived from high to low transition of 8088 clock signal CLK coming in from expansion backplane bus.
BA0	24	I	Buffered address 0: Active high input that selects either address register or one of 18 data registers inside CRTC. Active low selects address register. Active high selects control data registers. Derived from lowest bit of 8088 CPU buffered address bus.
6845CS*	25	I	6845 (CRTC) chip select: Active low signal that enables read/ write operation to CRTC internal register file. Active when address from CPU is valid and stable.
BD0-BD7	26-33	I/O	Buffered data: Bidirectional bus used to transfer data between 6845 CRTC internal register file and 8088 CPU. Output drivers are tristate (high impedance) except during CPU read of CRTC.
RA0-RA3	35-38	O	Raster address: Four of five outputs from internal raster counter. Used to select the row (raster) of the character generator ROM.
HSYNC	39	O	Horizontal sync: Active high output that determines the horizontal position of displayed text. This signal directly drives a monitor, or it can be processed to generate composite video.
VSYNC	40	O	Vertical sync: Active high output that determines the vertical position of displayed text. With a pulse width fixed at 16H (horizontal raster lines), this signal can directly drive the monitor, or it can be processed to generate composite video.

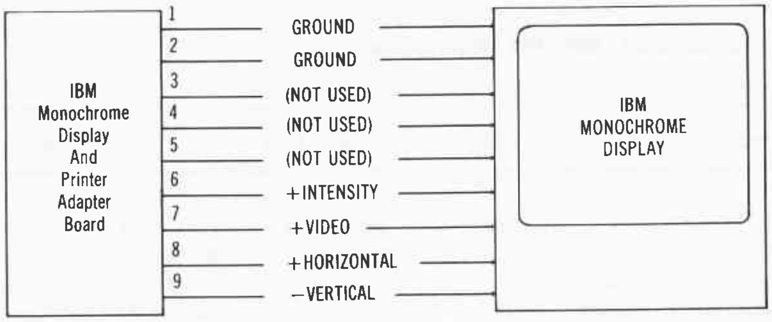


Fig. 2-64. The signals present on the pins of the connector of the monochrome adapter card.

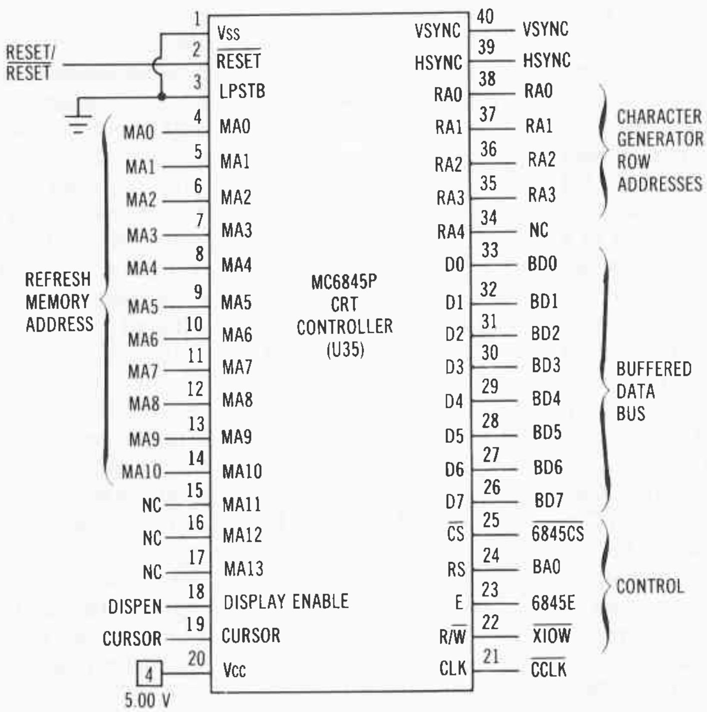


Fig. 2-65. 6845 CRT controller pin assignments (monochrome adapter board).

strobe input enables the chip to capture the refresh address in an internal light-pen register.

A programmable linear address register and 18 data registers are used in the CRTC to produce the necessary control signals for raster scan display generation. Table 2-21 describes the size and function of these registers.

Operation of the CRTC begins at system initialization when the system reset pulse clears all the counters and pulls the outputs low. As shown in Fig. 2-67 (CF page 2), the RESET signals are derived from the RESET DRV coming in on P3-B2 of the expansion bus backplane. The signal becomes RESET at the pin 3 output of 74LS125 quad 3-state buffer (U59) and is applied to the inputs of 74LS04 hex inverter (U56), 74LS393 dual binary ripple counter (U28), and 74LS86 quad 2-input exclusive OR gate (U54). Hex inverter U56 produces the active low RESET* signal that is applied to the rest of the circuitry shown in Fig. 2-67. Either U56 pin 12 or an optional RESET* signal from 74LS86 quad 2-input exclusive OR gate (U54) is connected to input pin 2 of 6845 CRTC (U35).

The active low RESET only functions when the LPSTB (pin 3) line is pulled low. Therefore, unused pin 3 is tied to ground on the monochrome monitor/printer adapter. One clock cycle after RESET occurs, the refresh memory address and row address bus outputs are pulled low. Immediately after the RESET signal is removed, the CRTC starts the display operation.

Table 2-21. Description of Internal Registers of 6845 CRTC

Reg.	Bits Used	R/W	Function
AR	5	W	Address register: A write-only pointer to one of 18 data registers (RA0-RA17). When 6845E and BA0 are both low, this register is addressed. When BA0 is high, the 18-register file is addressed.
R0	8	W	Horizontal total register: Write-only register that determines horizontal sync frequency. Used to program the total number of horizontal characters per line including the retrace period.
R1	8	W	Horizontal displayed register: Determines number of characters that will be displayed per line.
R2	8	W	Horizontal sync position register: Determines horizontal sync positions on horizontal line as multiple of character clock period.
R3	4	W	Horizontal sync width register: Determines width of horizontal sync pulse. Programmed as multiples of character clock period to allow compensation for different horizontal sync widths on certain monitors.
R4	7	W	Vertical total register: Determines the total number of lines per frame including vertical retrace period.
R5	5	W	Vertical total adjust register: To adjust total number of rasters per field and thus vertical deflection frequency.
R6	7	W	Vertical displayed register: Determines number of displayed character rows on CRT screen. Programmed in character row times.
R7	7	W	Vertical sync position register: Determines vertical sync screen position as multiple of horizontal character line periods. Increasing value shifts display position up. Decreasing value shifts display position down.
R8	2	W	Interlace mode register: Controls raster scan mode. 0 0 = noninterlace mode 0 1 = interlace sync mode 1 0 = noninterlace mode 1 1 = interlace sync & video mode In noninterlace mode used on IBM PC, the rasters of even and odd number fields are duplicated.
R9	5	W	Maximum scan line address register: Determines number of raster scan lines per character row including spacing.
R10	7	W	Cursor start register: Lower 5 bits determine cursor start raster address. Upper 2 bits define cursor display mode with top bit for blink and next bit for the period. B P Cursor Display Mode -- -- ---------------------------- 0 0 Nonblink 0 1 Cursor nondisplay 1 0 Blink period 16X field period (blink frequency 1/16 of vertical field rate) 1 1 Blink period 32X field period
R11	5	W	Cursor end register: Sets end raster address (see Fig. 2-66).
R12	6	W	Start address register (high): Combines with R13 to define first address generated as refresh address after vertical blanking.
R13	8	W	Start address register (low): Lower 8 bits of the 14 bit refresh address.
R14	6	R/W	Cursor register (high): Combines with R15 to define cursor location. Top 2 bits always zero.
R15	8	R/W	Cursor register (low): Lower 8 bits of 14 bit screen location of cursor.
R16	6	R	Light pen register (high): Combines with R17 to capture and store the detection address of the light pen. Because of slow light pen response, the value must be corrected (calibrated) by the BIOS program. Contents of internal address counter strobed into R16 and R17 on following high to low transition of CCLK after LPSTB goes high. LPSTB tied low on monochrome display/printer adapter so cannot use light pen with this board.
R17	8	R	Light pen register (low): Lower 8 bits of 14-bit detection address defined in description for R16.

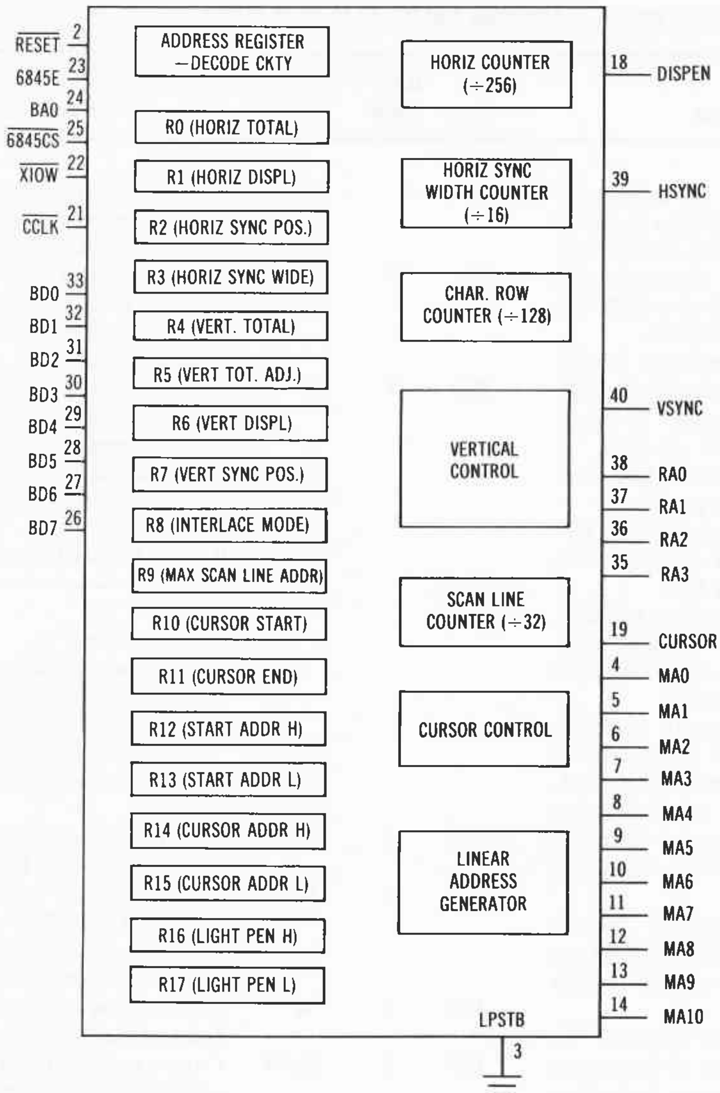


Fig. 2-66. Block diagram of 6845 CRT controller.

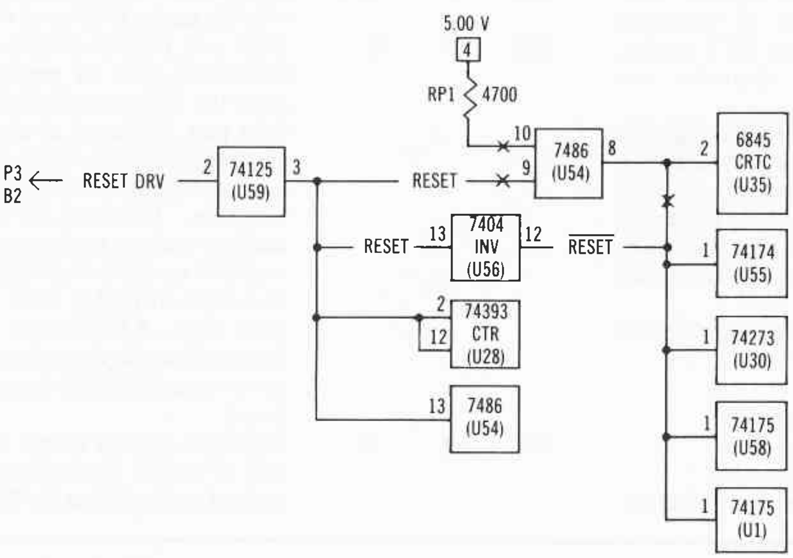


Fig. 2-67. Monochrome adapter board reset circuitry.

The same system reset that generated the RESET DRV signal passed out on the expansion bus also started the various clock signals to begin. The internal operation of the CRTC is synchronized by the control character clock input (CCLK) on pin 21 (Fig. 2-65). This signal enables the 8088 CPU to communicate with the 6845 CRTC over a buffered 8-bit data bus.

Control clock signal CCLK and its alternate CCLK* are generated by the circuitry shown in Fig. 2-68. Either the 16.257 MHz oscillator in the lower left of the figure or a TEST OSC signal are multiplexed through 74LS153 (U24) to produce DOTCLK. This signal is used to clock the 74LS112 Dual J-K negative edge-triggered flip-flop (U5). The delayed output from 74LS174 hex D flip-flop U1 is applied directly to the pin 3 J clock signal CACS CCLK on output pin 6 of U26.

With the adapter board clock signals pulsing and the 4.772727 MHz CLK signal coming onto the adapter board from the expansion bus, the monochrome card begins to stir. As shown in Fig. 2-69, the active low buffered I/O read and write inputs to 74LS00 quad 2-input NAND gate (U53) produce an active high enable signal E that is passed out onto the board and into the D (pin 12) and clear (pin 13) inputs to 74LS74 dual D flip-flop U45. Pin 13 needs an active low signal to clear the flip-flop, therefore, on the rising edge of the next CLK input on pin 11, the Q output (pin 9) toggles producing the 6845 CRTC enable signal 6845E that is applied to pin 23 of the CRTC U35.

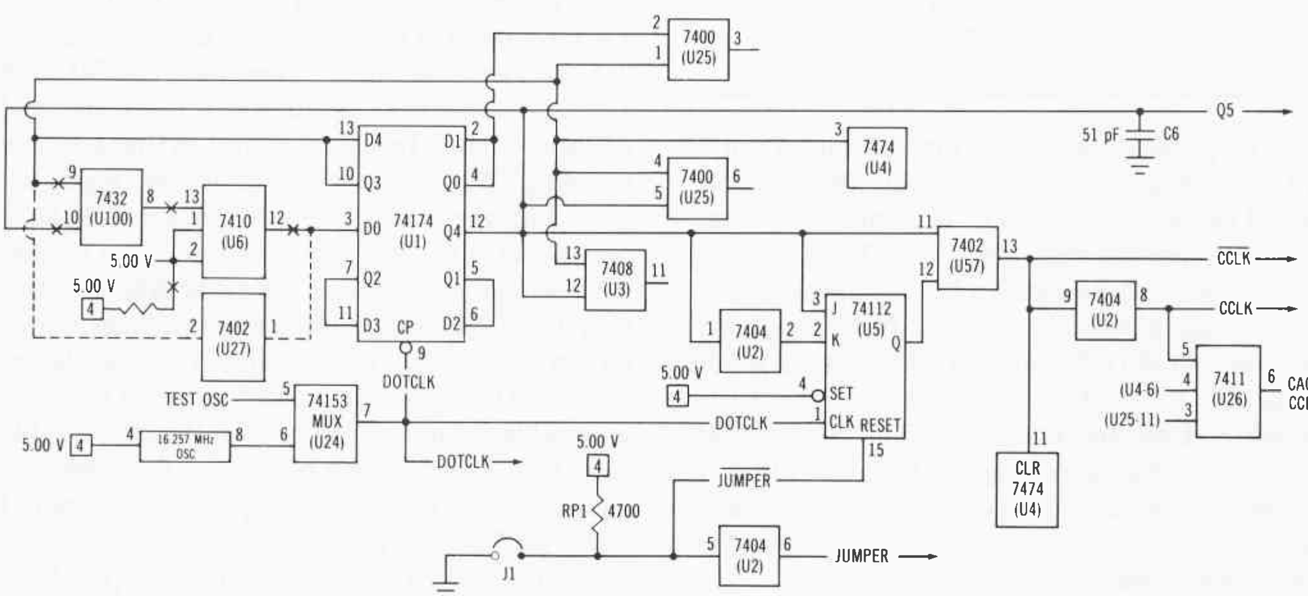


Fig. 2-68. 6845 clock (CCLK*) circuitry.

input to U5 and via the 74LS04 inverter (U2) to the pin 2 K input. The Q output from U5 is NORed with the delayed (Q5) signal from U1 to produce an active low CCLK* output on pin 13 of U57. CCLK* is applied to the pin 21 clock input to 6845 CRTC U35.

CCLK* is used to clear the 74LS74 dual D flip-flop U4 and is inverted by 74LS04 hex inverter U2 to produce CCLK. CCLK is ANDed with the outputs from U4 pin 6 and U25 pin 11 to generate a control address chip select control

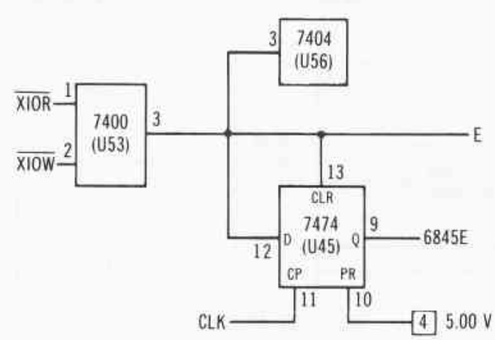


Fig. 2-69. 6845 chip enable signal (6845E).

With the CRTC enabled, the address bus and the system board address enable signal AEN are passed onto the adapter board and decoded by 74LS138 1-of-8 decoder/demultiplexer U52 as shown in Fig. 2-70.

The adapter board is addressed as an I/O device using hex addresses 3B4H, 3B5H, 3B8H, 3BAH, 3BCH, 3BDH, 3BE, and 3D8 through 3D1, as shown in Table 2-22.

Table 2-22. I/O Monochrome Adapter Board Addressing

I/O Address	Accesses
3B4	6845 index (address) register
3B5	6845 data registers
3B8	CRT control port 1
3BA	CRT status port
3BC	Parallel data port
3BD	Printer status port
3BE	Printer control port

To generate an active low output on pin 7 of U52 in Fig. 2-70, an address of 3Bx must be placed on the address bus. The suffix "x" must be a hex value less than eight. The 3B part of the address produces an active low output from pin 7. The signal becomes a qualifying input for another 74138 (U50) and 74LS32 quad 2-input OR gate U43. Buffered address signal BA3 is generated from address bit A3. The ORed output is the 6845 chip select signal (6845CS*) that is applied to pin 25 of CRTC U35. Thus anytime 3B4 or 3B5 are placed on the address bus, the CRTC is accessed.

The active low signal 6845CS* is inverted by U44 to produce the active high 6845CS signal that is used elsewhere on the adapter board.

The board has been reset, the clocks started, and the CRTC enabled and selected. The video system wakes up and the waveforms described in Fig. 2-71 are produced.

Mode Control Port 1 (3B8H)

The first command sent to the board by the 8088 CPU is an address to I/O location 3B8H (CRT control port 1). The value placed on the system address bus is 01H. This value sets the monochrome board to the high-resolution mode. This is a necessary prerequisite to accessing the monochrome adapter. The CRT mode control port 1 is formed by the circuitry shown in Fig. 2-72 (See CF (CSCS2-A) pages 2, 15, and 16).

The port has the I/O address 3B8H (0 0 1 1 1 0 1 1 1 0 0 0 in binary). With this code, bits 3, 4, 5, 7, 8, and 9 are high. Therefore, the 74LS138 1-of-8 decoder U52 inputs A4, A5, A7, A8, and A9 are high. Inputs A6 and AEN are low enabling U52 to generate an active low signal out pin 7 into the enable input of another 74LS138 decoder (U50). BA0, BA1, and BA2 are all low. BA3 is high. With either XIOR or XIOW active low, 74LS00 quad 2-input NAND produces a high on pin 3 that is felt on input pin 3 to 74LS04 hex inverter U56. The low on output pin 4 becomes an enable input to U50 completing the enable code (pin 5 low and pin 6 high are the other two enable inputs) and generating a low select port 1 signal (SEL1*) out pin 15.

SEL1* is the clock input on pin 9 of 74LS175 quad D flip-flop U58. A hex 01 is on the data bus input so BD0 is 1, BD2, BD3, and BD5 are all low (binary 0). When SEL1* goes

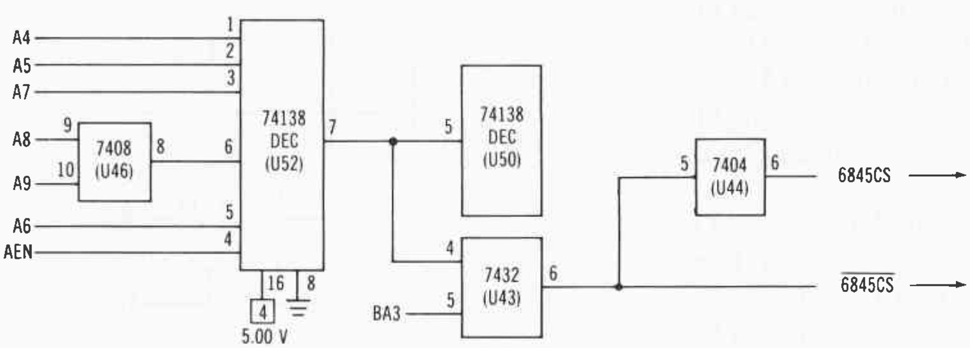


Fig. 2-70. 6845 chip select circuitry.

low to high, the high on BD0 is loaded in pin 4 generating a low out the Q* output pin 3. This low signal is felt on pin 4 of 74LS00 2-input NAND U53 producing a high on output pin 6. The high out pin 6 is felt on input pin 11 to 74LS10 3-input NAND U6. The other two inputs to U6 are held high so the pin 8 output becomes the active low high resolution signal HRES*.

By changing the input data word (BD0, BD2, BD3, and BD5) on the inputs to U58, other modes of operation can be selected. Table 2-23 describes the various modes that can be produced.

Status Port (3BAH)

The 8088 CPU (U3 on system board) can monitor the status of the video circuitry by addressing hex 3BA (0 0 1 1 1 0 1 1 1 0 1 0 in binary). The lower four bits of the address (BA0, BA1, BA2, and BA3) on the input to U50 in Fig. 2-72 produces an active low output on pin 13 (STATUS SEL*). This signal is passed to the enable input (pin 1) of 74LS244 octal buffer (U60) shown in the upper right of Fig. 2-73.

When enabled, U60 passes the status of the horizontal drive and line video signals onto

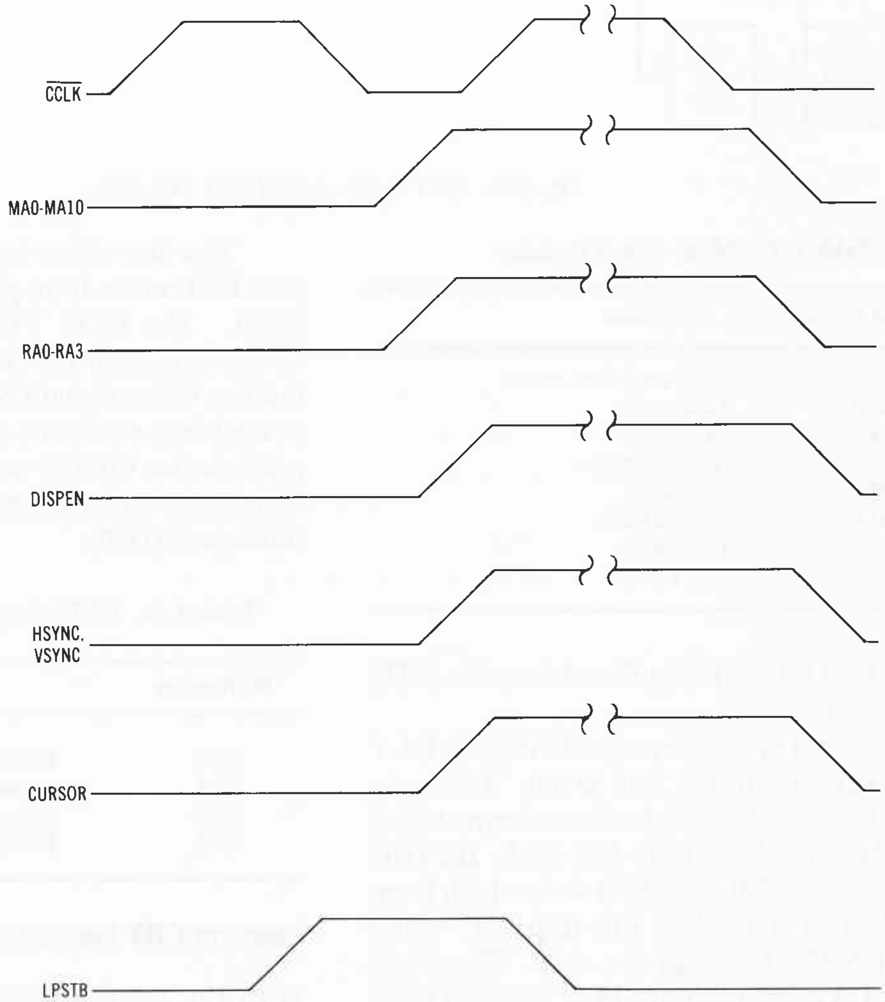


Fig. 2-71. 6845 CRT controller timing diagram.

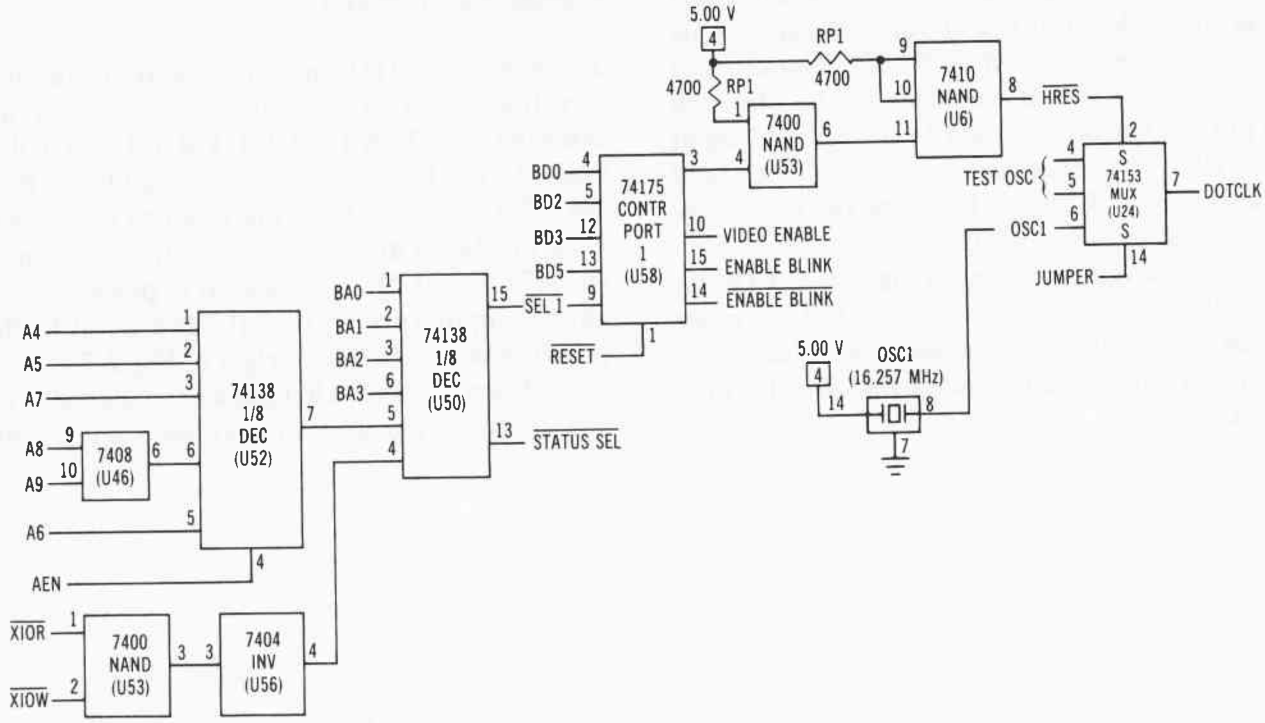


Fig. 2-72. CRT mode control port 1 circuitry.

Table 2-23. Mode Select Register

Data Bit Number	Function
BD0	High resolution mode
BD1	(not used)
BD2	(not used)
BD3	Video enable
BD4	(not used)
BD5	Enable blink
BD6	(not used)
BD7	(not used)

the lower four bits of the buffered data bus (BD0 through BD3).

Horizontal sync delay signal HSYNC DLY is derived from 74LS32 NOR U100. This gate monitors the status of the horizontal sync signal input to 74LS174 hex D flip-flop U55. HSYNC DLY is ANDed in 74LS08 (U3) with a high from pin 5 of 74LS74 dual D flip-flop U45 when VIDEO ENABLE clocks the chip. The pin 6 output of U3 is input on pin 13 of 74LS244 octal output buffer U64 to generate the horizontal drive signal (HORIZ DRIVE) out pin 7.

The line video input to pin 8 of the status port U60 comes from pin 5 of 74LS74 D flip-flop U101. The B/W VIDEO signal on pin 2 is clocked through U101 by DOTCLK to become the line video signal LVIDEO. LVIDEO is also passed into pin 15 of the output buffer U64 to produce the VIDEO output on pin 5. Table 2-24 defines the buffered data bus outputs of the CRT status port (U60).

Table 2-24. CRTC Status Port Bit Assignments

Bit Number	Function
BD0	Horizontal drive status
BD1	(reserved)
BD2	(reserved)
BD3	Black/white video status

Loading CRT Registers

With the CRT controller (U35) selected and enabled, the 8088 CPU performs an OUT instruction to I/O location 3B4. This addresses

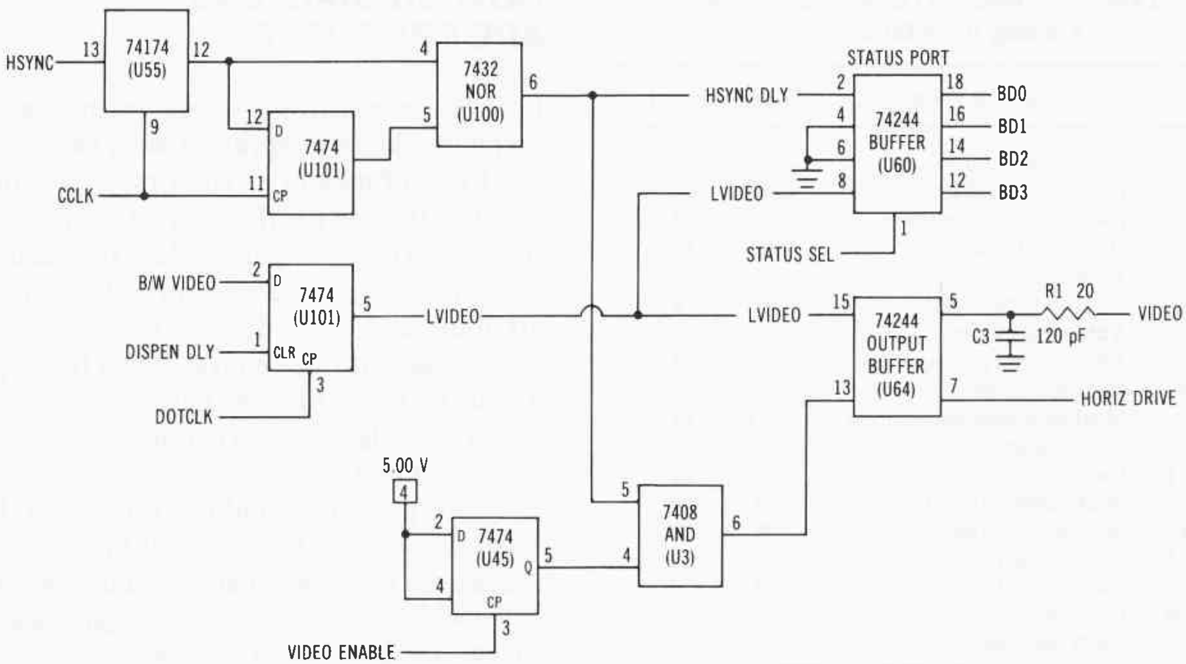


Fig. 2-73. CRTC status port circuitry.

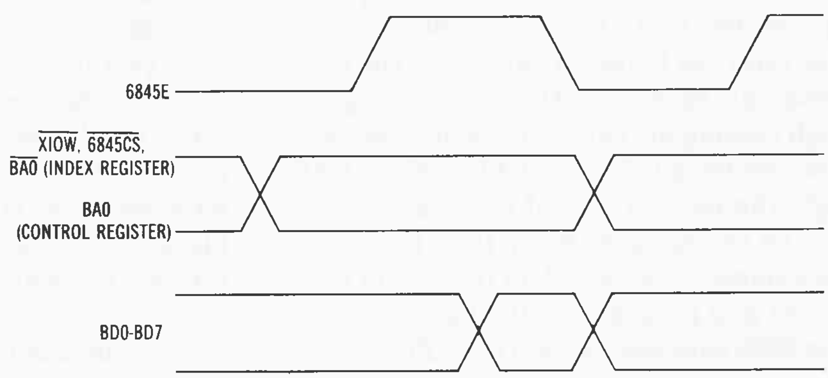


Fig. 2-74. Writing information into the 6845 CRT controller via the buffered data bus.

the 6845 index register. The lower 5 bits on the CPU data bus is a code representing 1 of the 18 control data registers. The code locks the CRTC into accessing a particular data register when the 8088 performs its next instruction, an OUT to location 3B5. The inversion of the least significant bit (BA0) selects the 18 control register stack. Because only 1 of the 18 registers is enabled, the information on the buffered data bus is copied directly into the selected and enabled control register. Figure 2-74 shows the timing relationships for writing information into the 6845 CRT controller via the buffered address bus.

Signal 6845E, chip enable goes high, XIOW* goes low, 6845CS* goes low, and BA0 goes low selecting the index address register. Data on the buffered data bus (BD0 through BD7) represents one of the 18 control registers. Then, with 6845E still high, XIOW* still low, and 6845CS* low, new data is placed on the buffered data bus and BA0 shifts high latching the new data into the selected control register.

Table 2-25 summarizes the 6845 CRTC internal register utilization and access addressing for use on the IBM monochrome display/printer adapter.

Table 2-25. 6845 CRTC Internal Register Loading upon Initialization

Register	Function Value	Hex	Decimal
R0	Horizontal total	61	97
R1	Horizontal displayed	50	80
R2	Horizontal sync position	52	82
R3	Horizontal sync width	0F	15
R4	Vertical total	19	25
R5	Vertical total adjust	06	6
R6	Vertical displayed	19	25
R7	Vertical sync position	19	25
R8	Interlace mode	02	2
R9	Maximum scan line address	0D	13
R10	Cursor start	0B	11
R11	Cursor end	0C	12
R12	Start address (high)	00	0
R13	Start address (low)	00	0
R14	Cursor (high)	00	0
R15	Cursor (low)	00	0
R16	Light pen (high)	-	-
R17	Light pen (low)	-	-

Reading Information Out of CRTC

Figure 2-75 describes the timing relationships for reading information from the 6845 CRT controller onto the buffered data bus. The chip is enabled and selected. Here, XIOW* goes active high causing the chip to recognize the data flow direction from CRTC to CPU. When BA0 goes high, the data in one of the four control registers (R14 through R17) that has been previously selected, is placed on the output data pins of U35 and passed over the buffered data bus to the 8088 data bus and into the CPU.

HOW CHARACTERS ARE PRODUCED

Both the monochrome display/printer and color graphics adapters represent each character with two bytes of memory. The first byte represents the ASCII code for the character. (A listing of the ASCII character codes is included in Appendix G.) The second byte contains an attribute code that defines the video features associated with the character to be displayed. These features include background darkness, foreground darkness, brightness (intensity), and blink condition.

Six possible combinations exist for the attribute byte. One, normal video with light characters on a dark background; two, reverse video with dark characters on a light background; three, flashing light characters on a dark background; four, flashing dark characters on a light background; five, invisible light characters on a light background; and six, invisible dark characters on a dark background. The last two combinations are of little use.

Two interlaced memories are installed on the monochrome adapter board. The character codes for the characters which are produced on the monitor screen are stored in 2K bytes of static memory (U12, U13, and U14), as shown in Fig. 2-76. U13 and U14 contain character codes for the top half of the display screen. The character codes for the bottom half of the screen are contained in U12 and U14.

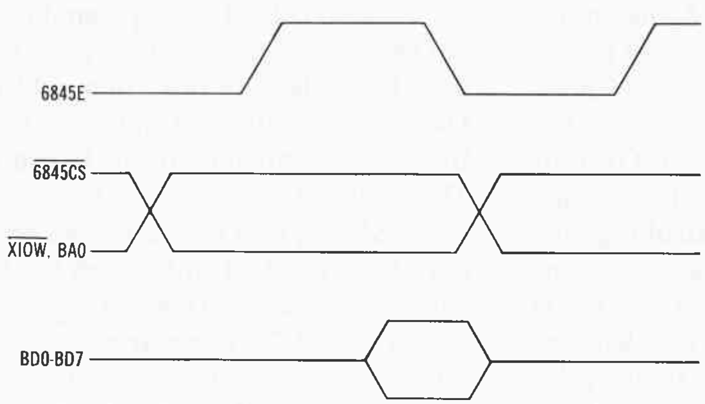


Fig. 2-75. Reading information from the 6845 CRT controller onto the buffered data bus.

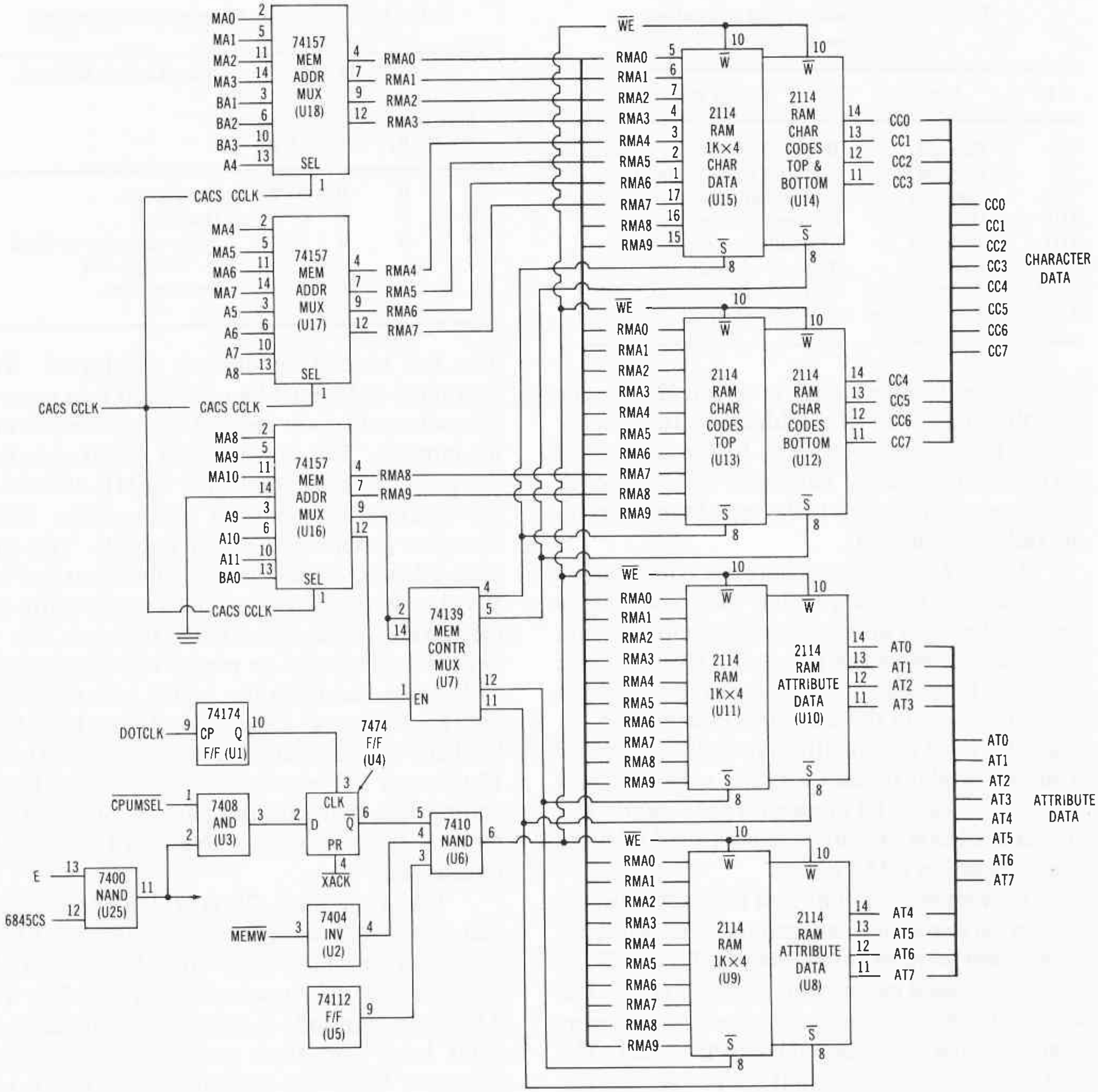


Fig. 2-76. Display buffer memory.

The blink, highlight, reverse video, and underline attribute features are stored in another 2K bytes of static RAM (U8, U9, U10, and U11). Table 2-26 describes the memory allocation for monochrome display video attribute information. The blink feature for the top half of the screen (first 1024 characters) is stored in U8. The highlight and underline features for the top half of the screen are stored in U11. These features for the bottom half of the screen are stored in U10. Reverse video information for the top half of the display screen is stored in U9 and U11. Reverse video for the bottom half of the screen is stored in U8 and U10.

Video information from the system board is stored in a fast static 4K RAM. Containing combined character codes and attribute codes, the 4K static RAM display buffer holds the video

Table 2-26. Memory Chip Allocation for Video Attributes

IC	Attribute	Screen Pixel Area
U8	Blinking	Bottom 976 character positions
U9	Blinking	Top 1024 character positions
U10	Highlight	Bottom half of screen
U10	Underline	Bottom half of screen
U11	Highlight	Top half of screen
U11	Underline	Top half of screen
U8, U10	Reverse video	Bottom half of screen
U9, 11	Reverse video	Top half of screen

Table 2-27. Attribute Feature Enhancements

Attribute Bits						Video Feature Achieved
Background			*Foreground*			
B6	*B5*	*B4*	*B2*	*B1*	*B0*	
0	0	0	0	0	0	Nondisplay
0	0	0	0	0	1	Underline
0	0	0	1	1	1	White character on black background
1	1	1	0	0	0	Reverse video

information for one complete screen (25 rows by 80 columns). The first address in the display buffer (B0000) corresponds to the upper-left corner of the screen. The lower-right corner of the screen corresponds to the top of the 4K memory (address B0F9FH).

Up to 256 different character codes can be stored in the 4K display buffer. Each character is represented by a unique character and attribute code pair, as shown in Fig. 2-77. Even address locations hold the character codes; odd address locations contain the attribute information. A character code and an attribute code are fetched from the display buffer every 552 ns producing a video data rate of 1.8 megabytes per second. The contents of this 4K buffer can be read into the system board by DMA action.

Combining the blink and intensity bits with the foreground and background bits produces other video features as described in Table 2-27.

The second memory on the adapter board is an 8K ROM that contains the dot patterns (fonts) for the 256 different character codes. The ASCII character code that enters the monochrome adapter board from the system board data bus cannot be directly displayed. The character code must be converted into rows of dot patterns that are sent out the video cable into the monitor. The conversion of ASCII code into dot patterns is accomplished by MK-36906N-4, an MK36000-compatible 8K-by-6-bit ROM character generator U33 (CF page 2). This chip is an edge-activated NMOS ROM that has on-board address latches controlled by the active low chip enable input signal CEROM* (pin 20). A negative-going edge on pin 20 will activate U33 and strobe and latch the inputs into the chip's address registers. Once the address hold time has been met, the outputs (pins 9 through 11, and 13 through 17) become active and contain the appropriate character dot pattern. The outputs remain latched and active until CEROM* returns high.

When the 6845 CRTC (U35) determines that display data is required, it causes the ASCII code and attribute data stored in the RAM display buffer to be read out (see Fig. 2-78). The 8-bit character code is temporarily stored in an octal latch and then passed into character generator U33. The other input into U33 is a 4-bit address defining which row of dots for the

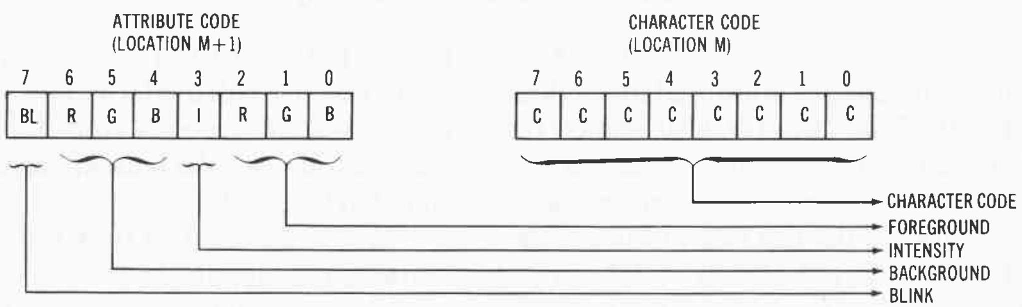


Fig. 2-77. Character and attribute codes.

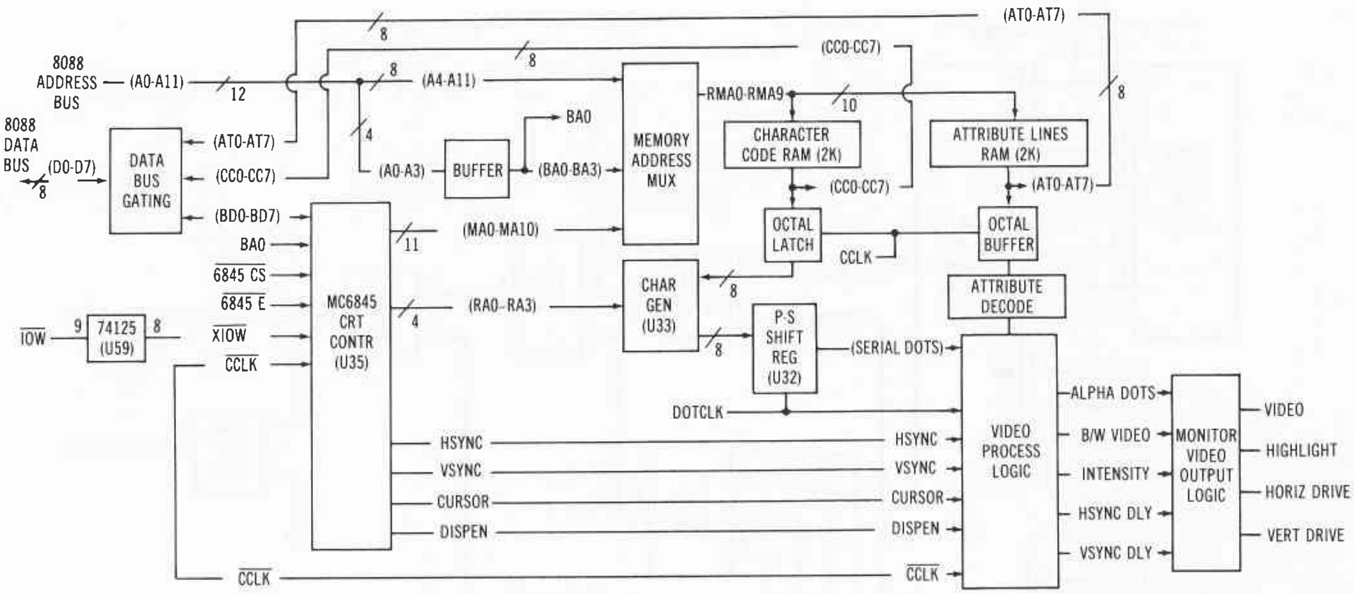


Fig. 2-78. Monochrome display adapter block diagram.

character to be displayed will be passed out U33 into a 74LS166 parallel-to-serial shift register (U32) to be converted into a serial dot stream at its output.

The attribute information is applied to video process logic with the serial dot patterns to produce a modified dot pattern with the desired attribute features. This combined signal is clocked by CCLK* through the logic to become ALPHA DOTS, a select signal to enable a blink/no-blink intensity attribute signal, and a black and white video serial dot stream (B/W VIDEO). B/W VIDEO passes through a monitor direct drive output buffer to become the VIDEO signal at the unit video connector J3. Figure 2-79 shows the circuitry that produces the ALPHA DOTS and B/W VIDEO signals that are applied to the monitor direct drive output logic (see also CF page 2). An 8-bit code is output by character generator U33 onto its character generator bus (CGB0 through CGB7). This code enters the data input buffer of 74LS166 parallel-to-serial shift register U32 on pins 2 through 5, 10 through 12, and 14.

An active low clear video (CLRVIDEO*) signal is used as a master reset input on pin 9 of U32. The chip is clocked by the DOTCLK input on pin 7. Pin 15 is for the parallel enable serial load signal S/L*. When S/L* is low one setup time before the low-high clock transition, parallel data from U33 enters U32. This same signal prevents a serial input from entering the chip via SERIN on pin 1. Once the character generator bus has been entered into the eight internal R-S flip-flop latches inside U32, SERIN is held low and S/L* is pulled high letting DOTCLK shift the 8-bit dot pattern code from least significant bit to most significant bit out the Q7 register output (pin 13) as a sequence of serial dots (S DOTS). The character generator produces a row of 8 dots. The character box is 9 dots wide so a blank dot is inserted between each character. SERIN is used to duplicate the eighth dot into the ninth dot position for ASCII characters whose codes are between B0H and DFH.

The S DOTS bit stream is ORed with the UNDERLINE signal on pin 13 of 74LS32 quad 2-input OR U43 to produce a modified bit stream input to pin 11 of 74LS11 3-input AND gate U26. The other two inputs to U26 are NODSPLY* from 74LS175 quad D flip-flop U29 and attribute control from the pin 6 output from 74LS20 dual 4-input NAND U62. The pin 8 output from U26 is ANDed with the combined CURSOR DLY and CURSOR BLINK signals from 74LS08 quad 2-input AND U3 in another part of 74LS32 (U43) to produce the signal ALPHA DOTS. These ALPHA DOTS becomes one input to 74LS86

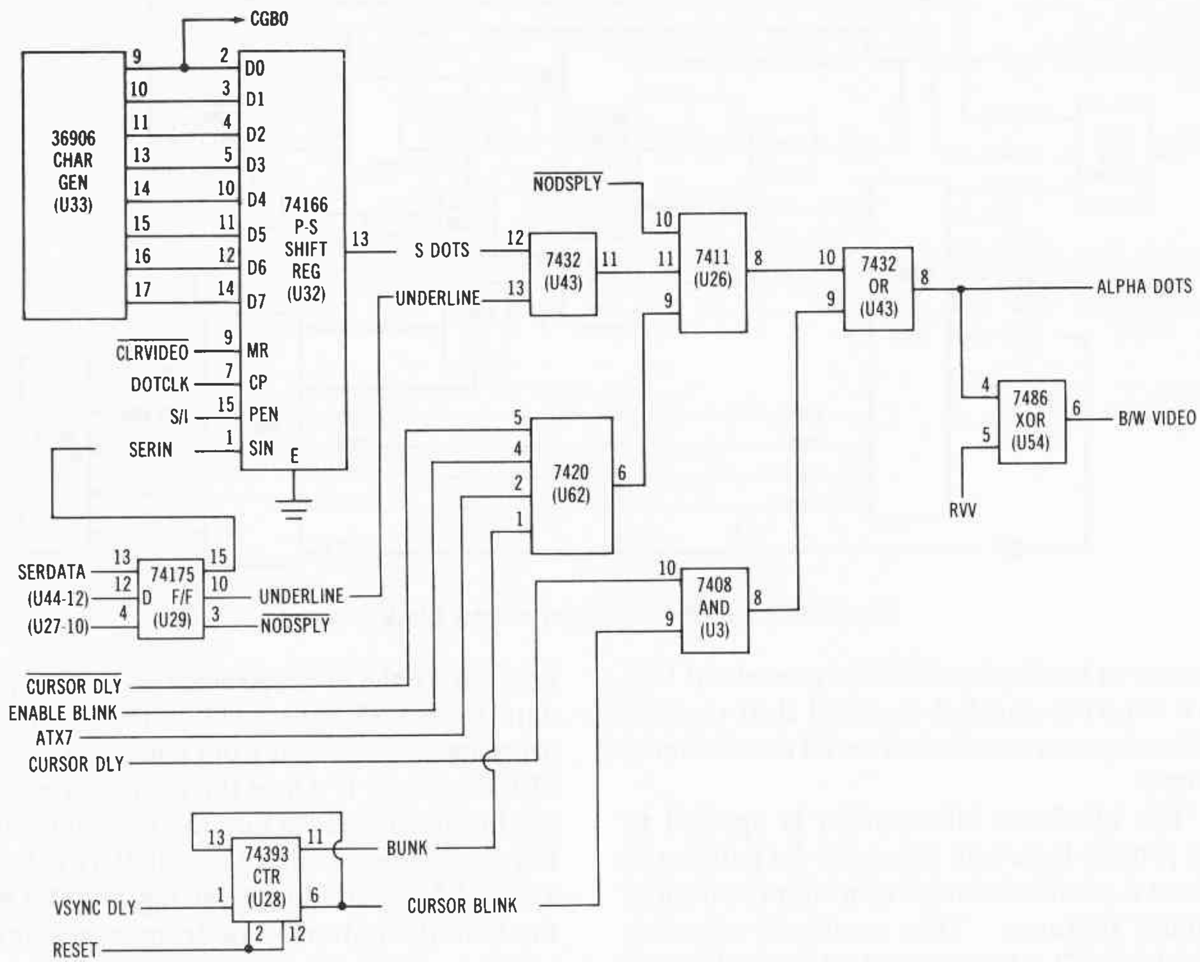


Fig. 2-79. Video display circuitry.

quad 2-input exclusive OR gate U54. A reverse video signal RVV on pin 5 is the other input. The EXOR output on pin 6 becomes the black and white video signal B/W VIDEO that reaches the J3 connector as the signal VIDEO.

The horizontal and vertical sync signals (HSYNC, VSYNC), CURSOR, and DISPEN signals are also applied to the video process logic. HSYNC and VSYNC become HSYNC DLY and VSYNC DLY inside the logic and end up as horizontal and vertical drive signals (HORIZ DRIVE, VERT DRIVE) at the video output connector J3, as shown in Fig. 2-80.

The pins 39 and 40 output from 6845 CRT controller U35 become inputs to 74LS174 hex D flip-flop U55. HSYNC on D input pin 13 is passed out the Q side of the latch on pin 12. This signal is delay-latched through 74LS74 U101 and then ANDed in 74LS32 U100 to produce HSYNC DLY on output pin 6. A logic high is clocked through 74LS74 U45 to appear at pin 4 of 74LS08 AND gate U3 when VIDEO ENABLE is active high on the pin 3 clock input of U45. The ANDed output from U3 is buffered through 74LS244 tristate octal output buffer U64 to become a 15,750 Hz stream of active low 5 microsecond horizontal drive (HORIZ DRIVE) pulses at video connector J3 pin 8.

The VSYNC output from pin 40 of 6845 CRTC U35 is latched through U55 to become VSYNC DLY on pin 1 of 74LS86 exclusive OR gate U54. Its other input (JUMPER*) comes from the J1, resistor, 74LS04 inverter U2 network. The output from U54 is buffered through U64 to become a 60 Hz stream of 190 microsecond pulses (VERT DRIVE) on pin 9 of connector J3.

The video monitor direct drive output logic

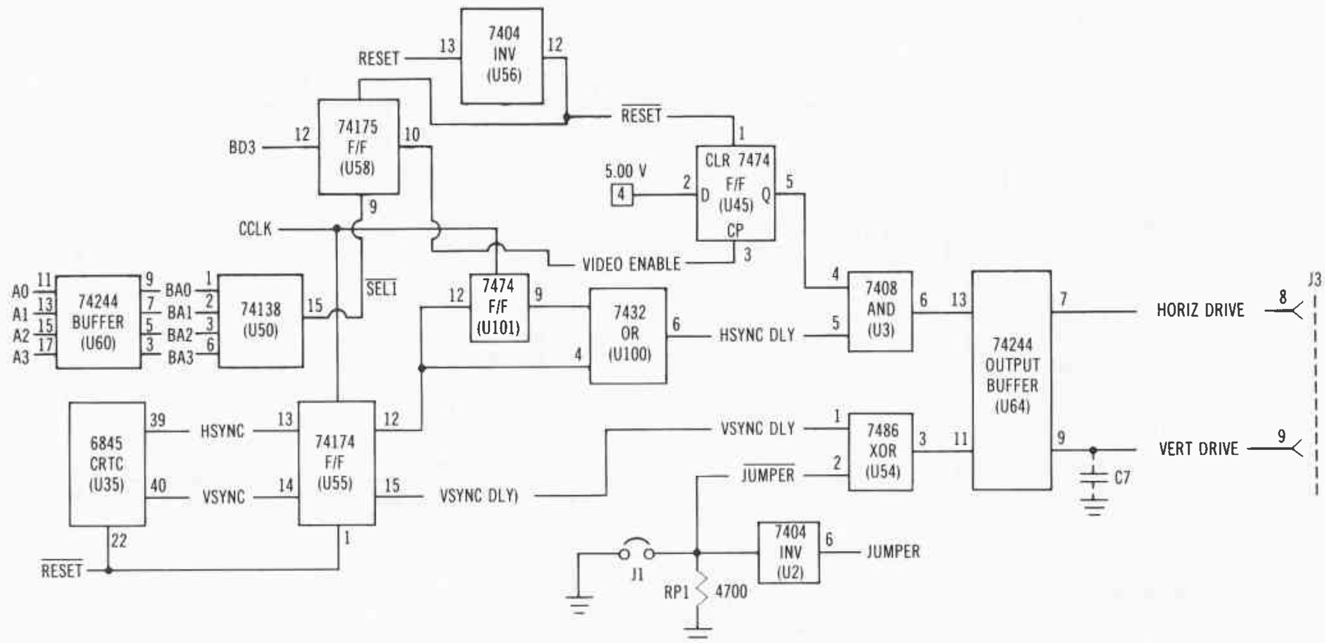


Fig. 2-80. Monochrome adapter horizontal and vertical sync circuitry.

is shown in Fig. 2-81. B/W VIDEO is clocked through U101 and U64 to become the VIDEO dot pattern information passed out J3 pin 7. HSYNC DLY is ANDed in 74LS08 U3 and passed through U64 to become HORIZ DRIVE pulses on J3 pin 8, and VSYNC DLY is exclusive ORed in 74LS86 U54 and buffered through U64 to become VERT DRIVE pulses on J3 pin 9.

The fourth important output from this logic circuitry is the intensity signal (HIGH LIGHT) on J3 pin 6. Figure 2-81 shows that this signal originates from the high bit (AT7X) of the attribute byte coming out of the 2K attribute RAM. As described with Fig. 2-77, the high bit can be toggled to turn on and off the blink function. Bit 3 (AT3X) of the attribute word is used to control the intensity of the character being displayed. Buffered attribute bits AT3X and AT7X are latched into two flip-flops in 74LS273 octal D flip-flop U30. The Q7 output (pin 19) is ANDed with (ENABLE BLINK)* to produce a bright blinking character control intensity blink signal I(B) on pin 3 of U46. The Q3 output (pin 9) is the full intensity control signal I(F).

Both intensity signals–I(B) and I(F) are applied to 74LS157 multiplexer U63. The pin 1 (ALPHA DOTS) and pin 15 (DISPEN DLY)* signals are used to select I(B) or I(F) as the pin 12 output. An active low DISPEN DLY signal on pin 15 enables ALPHA DOTS on pin 1 to select one of the two intensity input signals. When pin 1 is high, I(F) is selected and its condition is passed through to output pin 12. A low on pin 1 selects I(B) pin 14 as the signal to pass through to output pin 12.

The multiplexed output from U63 is buffered by U64 and becomes the signal HIGH LIGHT that is passed out through connector J3 pin 6. Figure 2-64 described the monochrome video adapter outputs at connector (J3).

So we have a serial stream of video dot information, clocking out over the video connector into the monochrome display. Figure 2-82 shows that the internal registers of the 6845 CRTC determine how many characters are displayed on the screen (R1=80), the total character dot arrays provided (R0=97), the number of raster lines for each character (R9=14), the number of vertical characters displayed (R6=25), and the vertical total offset (R5=6).

If we zoom in on a single character position (for example, C1 in Fig. 2-82), a 9 by 14 dot array can be noticed, as shown in Fig. 2-83A. The serial VIDEO stream of dot pulses coming out

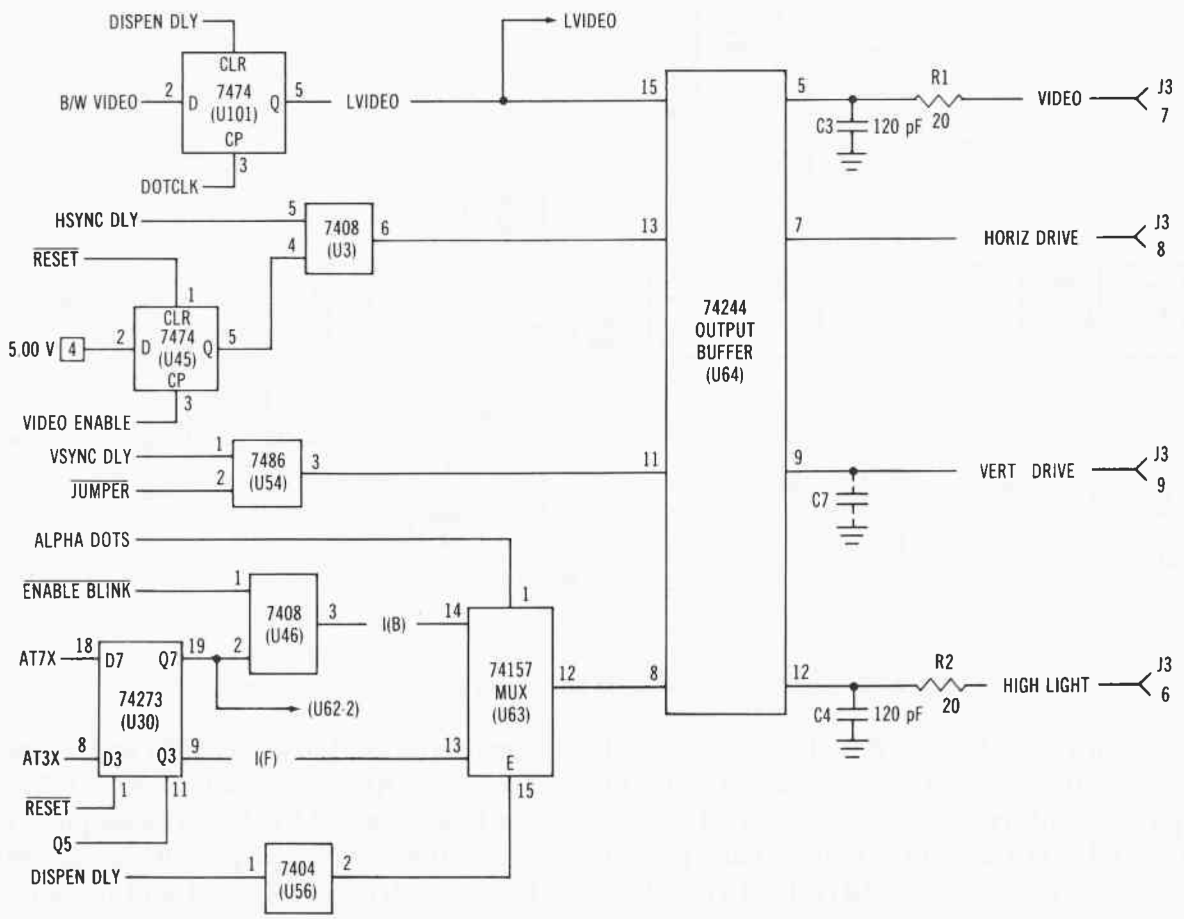


Fig. 2-81. Monitor adapter video output circuitry.

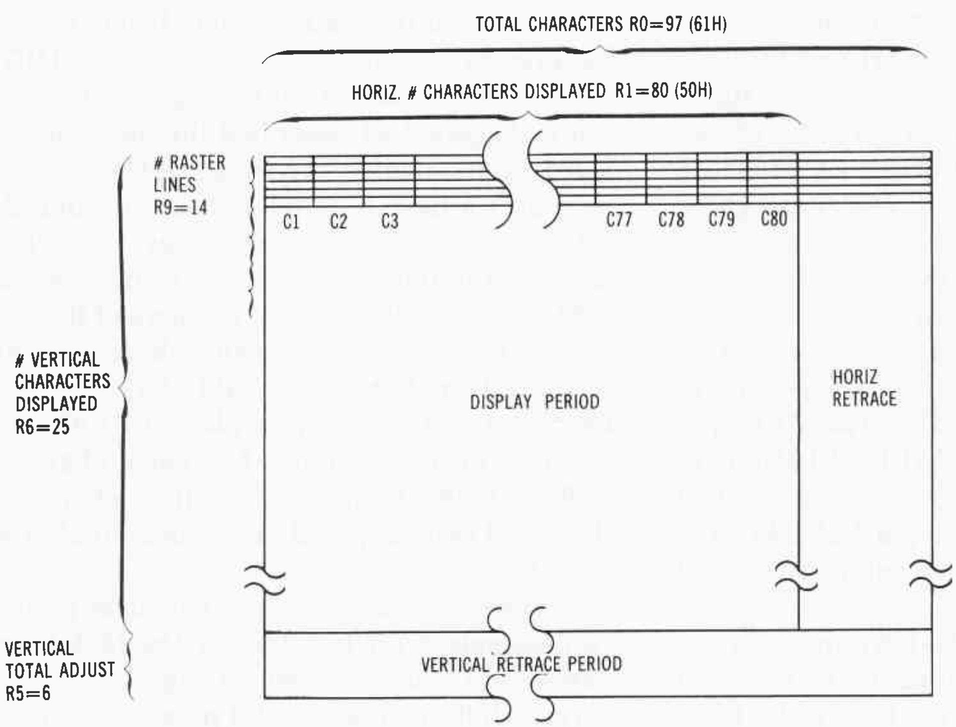


Fig. 2-82. 6845 CRTC register control of display screen.

over connector J3 are arranged such that each raster line is comprised of 97 nine-dot sequences. Each 9-dot packet represents one raster of the 14 needed to define a character box. As shown in the figure, two raster lines of no dots appear above the character, and three raster lines of no dots appear below the character. The additional raster lines below the A character provide room for an underline symbol (and for other characters, a descender).

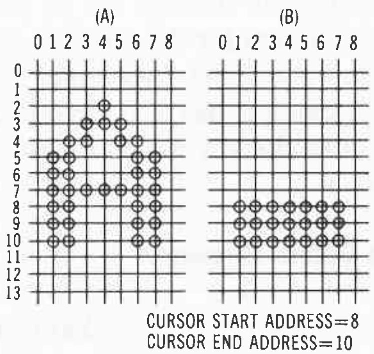


Fig. 2-83. Letter and cursor pixel activation within 7 by 9 of a 9 by 14 dot matrix.

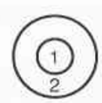
Figure 2-83B shows one possible size of cursor display. The INT 10 interrupt command can be used to change the cursor size and position within the array box.

While the first raster line of dot information is shifted into the display unit, the horizontal and vertical drive signals control when the serial dot stream for a particular raster is complete and when the next raster line should begin. After 14 raster lines are shifted into the display unit, one row of characters is produced on the screen. The circuitry then begins to produce the first raster line in the second row of characters. And so the process goes until the last raster line has been sent out over connector J3 completing the last row of characters in the display.

Color Graphics Adapter Card

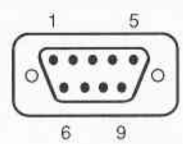
The IBM color/graphics card can generate alphanumeric characters like the monochrome card. (Refer to COMPUTERFACTS CSCS2-B for this discussion.) It can also produce bit-mapped graphics. The board is designed to function with the IBM-produced color display unit. It can also drive other monitors and standard home television receivers.

Three video connections are on the board. One connection is an RCA jack for composite video output, as shown in Fig. 2-84. A second video interface is a 9-pin DIN connector for direct video drive to an RGB monitor. This output consists of separate red, green, and blue signals plus intensity and ground. A third output available on a 4-pin Berg strip provides a connection point for composite video, power, and ground. This interface is used to connect an RF modulator so you can use a standard television receiver with the PC.



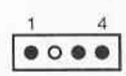
Pin	Signal
1	1.5-volt composite video
2	Chassis ground

RCA jack-composite video



Pin	Signal
1	Ground
2	Ground
3	Red
4	Green
5	Blue
6	Intensity
7	
8	Horizontal sync
9	Vertical sync

9 -Pin din connector-color direct



Pin	Signal
1	+12 volts
2	-
3	Composite video
4	Logic ground

4-Pin Berg strip-RF modulator connections

Fig. 2-84. The video connections on the color/graphics adapter card.

A light pen connection is also available, but the mouse is the most popular input device complementing the keyboard.

To the system board, the color graphics adapter card looks like 9 I/O addresses plus 16 Kbytes of memory. The nine I/O addresses are given in Table 2-28.

Color Adapter Board 6845 CRTC

The color/graphics card contains the same type 6845 CRT controller as is used on the mono-

Table 2-28. Registers and Latches Directly Addressable on the Color/Graphics Adapter Card

Hex Address	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Register Function
3D0	1	1	1	1	0	1	0	Z	Z	0	6845 CRTC registers
3D1	1	1	1	1	0	1	0	Z	Z	1	6845 CRTC registers
3D4	1	1	1	1	0	1	0	Z	Z	0	6845 address register
3D5	1	1	1	1	0	1	0	Z	Z	1	6845 data register
3D8	1	1	1	1	0	1	1	0	0	0	Mode control register
3D9	1	1	1	1	0	1	1	0	0	1	Color select register
3DA	1	1	1	1	0	1	1	0	1	0	Status register
3DB	1	1	1	1	0	1	1	0	1	1	Clear lt pen latch
3DC	1	1	1	1	0	1	1	1	0	0	Preset lt pen latch

(Z = don't care condition)

chrome adapter card. On the color card, however, the CRTC must be reprogrammed each time graphics modes are changed. Figure 2-85 shows the pin assignments for the 6845 CRTC used on the color adapter card (see CF (CSCS2-B), page 2).

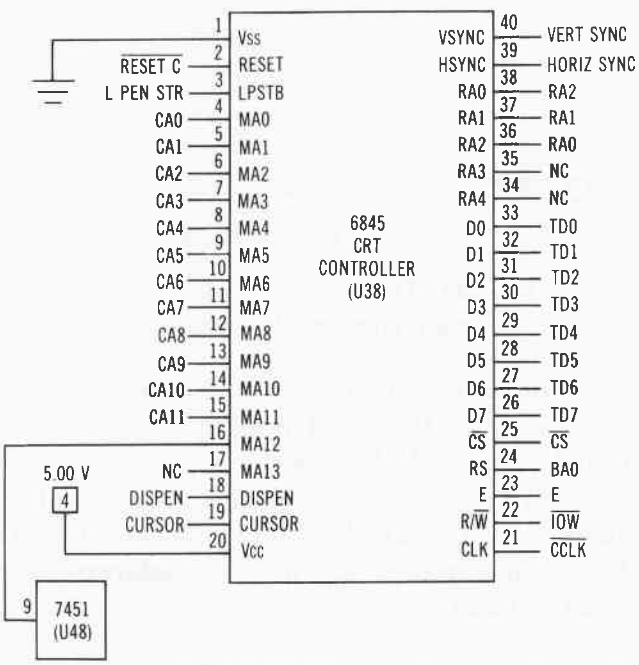


Fig. 2-85. Pin assignments for the 6845 CRT controller used on the color/graphics adapter card.

Reprogramming data enters and status data exits the CRTC as shown in Fig. 2-86. Hex addresses 3D0, 3D1, 3D4, and 3D5 access the 6845 I/O device. Pins A2 through A9 on the P2 expansion bus connector interface the 8-bit data bus (D0 through D7) of the 8088 CPU (U3) on the system board with the 74LS245 octal transceiver U66 on the color adapter card. Whenever DATA GATE is low and the output of 74LS08 2-Input AND (U41) is low, data flows from the transceiver data bus (TD0 through TD7) to the left out through the P2 connector as D0 through D7 data for the system board. When the pin 1 input to U66 goes high, data passes from the system data bus (D0 through D7) to the right out onto the transceiver data bus (TD0 through TD7).

6845 Chip Select Circuitry

Figure 2-87 shows the circuitry that generates the active low chip select signal CS* used by the 6845 CRTC U38. A binary 1 1 1 1 0 1 X X X X or X X X X X X 1 0 0 0 on the system address bus qualifies the inputs to 74LS32 OR gate U30 producing a low CS* signal out to pin 25 of U38. The first address qualifies 74LS08 AND U41, the 74LS138 decoder U18, and one input to 74LS32 OR U30 generating CS*. The latter address with bit A3 set qualifies the other OR input to U30.

6845 Enable Circuitry

The I/O read and write signals coming in from the system board expansion connector P2 are applied to a 74LS00 2-input NAND gate U15, as shown in Fig. 2-88. The ANDed output (pin 8) is applied to pin 1 of 74LS04 hex inverter U16 and the reset input (pin 13) and D input (pin 12) of 74LS74 dual D flip-flop U11. U11 is clocked by the system board signal CLK. The pin 9 Q output from U11 is the enable signal E that is applied to pin 23 of 6845 CRT controller U38.

6845 Clock Generation Circuitry

Figure 2-89 shows the circuitry that generates the control clock signal CCLK* that enters pin 21 of

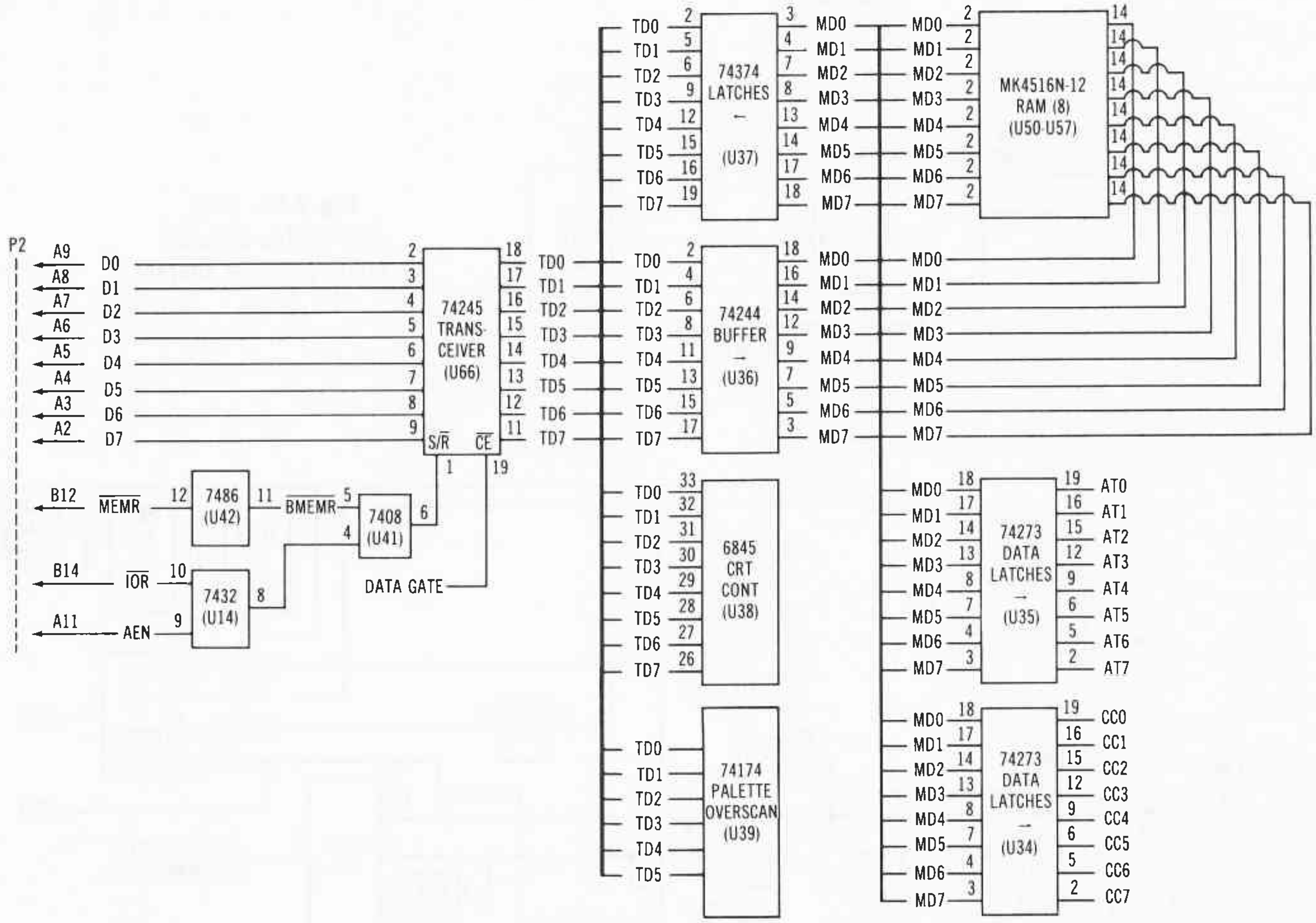


Fig. 2-86. Color adapter data bus circuitry.

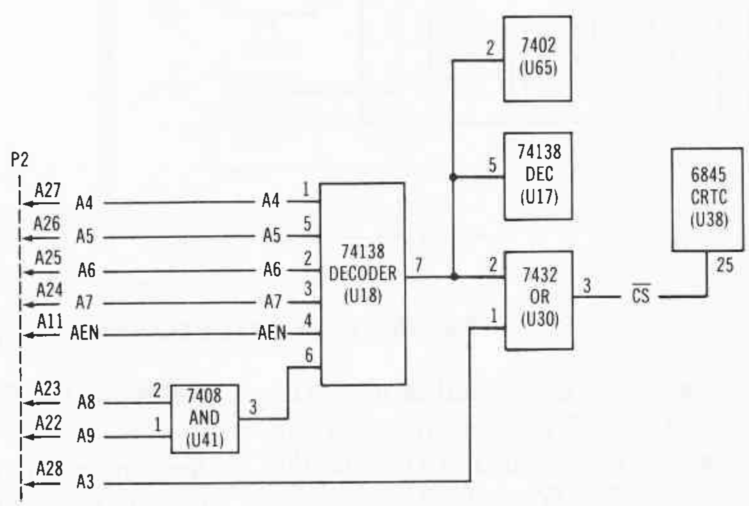


Fig. 2-87. Color/graphics adapter 6845 CRTC chip select circuitry.

6845 CRTC U38. A 14 MHz OSC signal from the expansion bus connector P2-B30 is inverted by 74LS04 U26 to produce the 14 MHZ clock signal. This signal is applied to the two 74LS174 timing generator chips U4 and U5 resulting in several special clock timing signals.

On the right side of Fig. 2-89 is a 74LS51 AND-OR-invert gate U27 that generates CCLK*

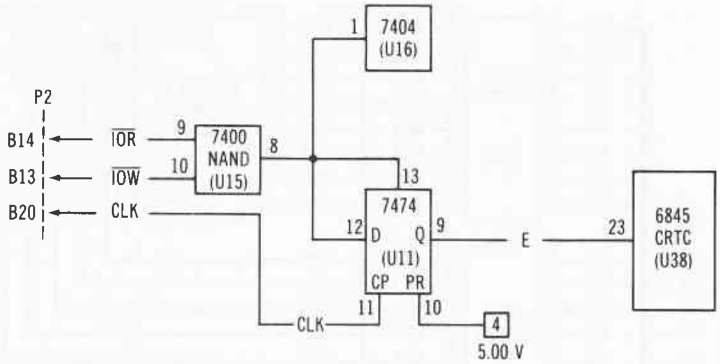


Fig. 2-88. 6845 chip enable circuitry on color/graphics adapter.

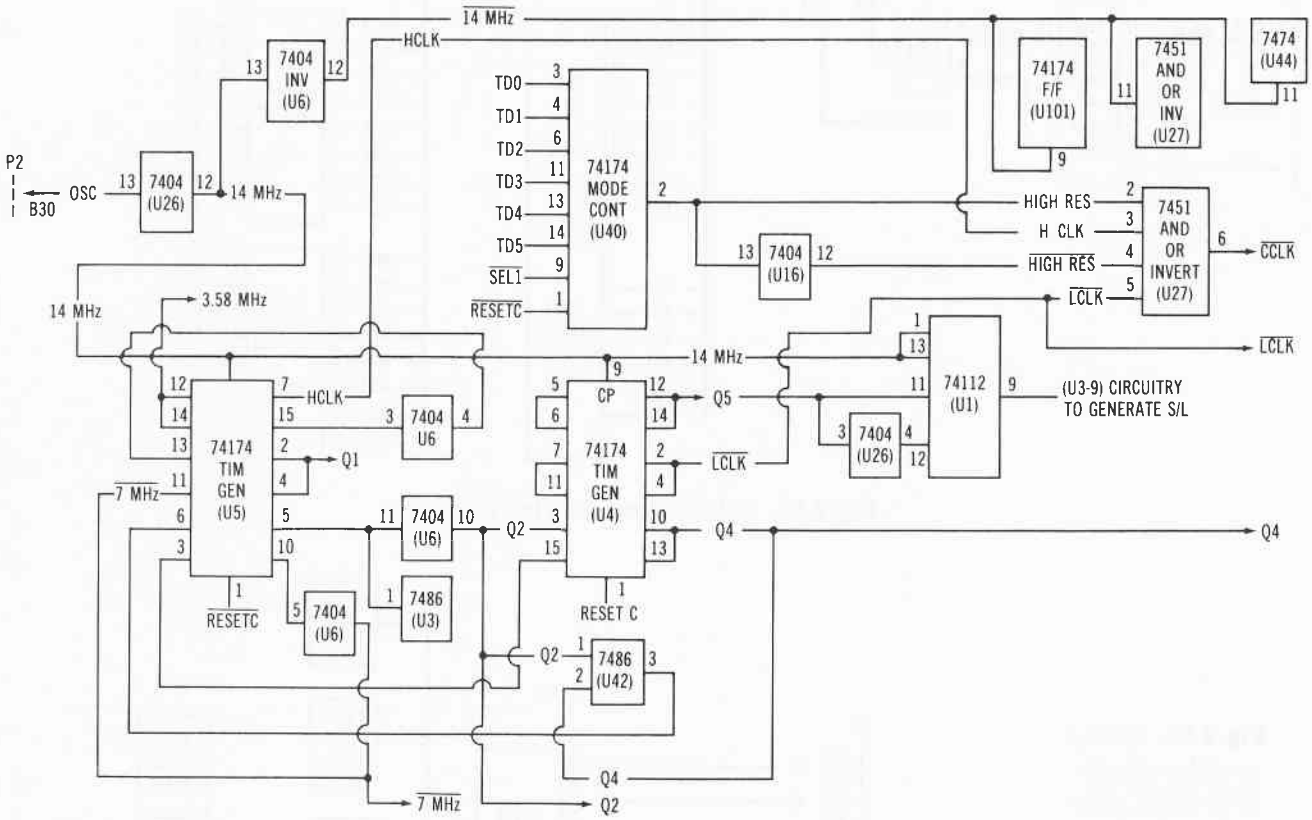


Fig. 2-89. Color 6845 CRTC clock circuitry.

whether high resolution is selected or not. The condition of HIGH RES is determined by the transceiver data bit TD0 on pin 3 of U40 and the pin 9 clock input SEL1*. When TD0 is high, the low-to-high transition of CCLK* transfers the TD0 high to its pin 2 HIGH RES output. HIGH RES is ANDed with the changing horizontal clock (H CLK) signal in U27 to produce a pulsing CCLK* for the 6845 CRTC U38.

Selecting the Color/Graphics Mode

Sending a byte of information from the system board to I/O address 3D8H causes the transceiver data byte to enter mode control register 74LS174 hex D flip-flop U40, as shown in Fig. 2-89. The output of U40 is high or low signal HIGH RES. When HIGH RES is logic high, it is ANDed with H CLK to produce an output CCLK* that clocks at the H CLK rate. When HIGH RES is LOW, input pins 4 and 5 to U27 qualify another AND gate inside U27 to produce a CCLK* signal that clocks at the LCLK* rate.

This means that two primary modes of operation are possible: one a high resolution (all points addressable, or bit-mapped graphics) mode and the other a low resolution (alphanumeric) mode like the monochrome card. Within these two modes, additional submodes are available. Both 40-column by 25-line and 80-column by 25-line alphanumeric modes are available with characters defined in either a 7 by 7 dot font pattern or a 5 by 7 dot font pattern within an 8 by 8 dot matrix array. In both text modes, up to 16 foreground colors and 8 background colors can be used. With either character font size, a single line is available for descenders. Because of this, the characters are not as well defined as those produced by the monochrome card. In addition, underlining is not used.

Blinking, highlighting, and reverse video are available in the black-and-white mode only. Selective character blinking can also be controlled.

In the graphics mode, each pixel is independently addressable so many character shapes can be generated. Three bit-mapped graphics modes are available: a nonsoftware-operating-system-supported low resolution color graphics mode with 160 dot rows and 100 pixel columns (pixels controlled in groups of two dots high by two dots wide), a software-supported medium resolution color graphics mode with 320 pixel rows and 200 pixel columns (each pixel individually controlled), and a software-supported high resolution black-and-white only graphics with 640 pixels in a row and 200 pixels in a column. In high resolution graphics each pixel is individually controlled.

Color Selection

Medium resolution can make each dot one of four color configurations–one of 16 preselected background colors, and three other preselected colors, as shown in Chart 2-1. Two sets of three-color palettes are available: color set 1 with green, red, and brown, and color set 2 with cyan, magenta, and white. The background colors include the eight basic colors produced by combinations of red, green, and blue, and an additional eight lighter versions of the same colors possible by using the intensity control bit.

Chart 2-1. Possible Colors in Medium Resolution Graphics

Black	Gray
Blue	Light blue
Green	Light green
Cyan	Light cyan
Red	Light red
Magenta	Light magenta
Brown	Yellow
White	Bright white

COLOR SET C0	COLOR SET C1
Green	Cyan
Red	Magenta
Brown	White

The color set is selected by sending a byte to I/O address 3D9H. This address accesses color-select circuitry. When a byte of data is sent to address 3D9H, the first six bits determine the background and foreground colors in the alphanumeric, and medium and high resolution modes. Bit 5 selects the active color set in medium resolution graphics.

Colors Available in Alphanumeric Mode

The foreground (character) and background colors for both the monochrome and color/graphics adapters are defined by the attribute byte as described in Table 2-29. The monochrome adapter will only produce the colors shown in Chart 2-1. Any other code will result in unrecognizable white characters on a white background.

With a color graphics card installed, the display foreground and background colors can be determined by Table 2-30. Note that the combinations of red, green, and blue alone are used to define the background color for characters in color mode. Sixteen colors are

Table 2-29. Alphanumeric Code Defining Foreground and Background Color on Both Monochrome and Color/Graphics Adapter Cards

Attribute Byte		Background Color	Character Color
7 6 5 4	3 2 1 0		
BL R G B	I R G B		
Bkground	Foreground		
B 0 0 0	I 0 0 0	Black	Black
B 0 0 0	I 1 1 1	Black	White
B 1 1 1	I 0 0 0	White	Black
B 1 1 1	I 1 1 1	White	White

Table 2-30. Background and Foreground Colors Available on the Color Adapter Card

Background Colors		Foreground Colors	
RGB	*Color*	*RGBI*	*Color*
000	Black	0000	Black
001	Blue	0010	Blue
010	Green	0100	Green
011	Cyan	0110	Cyan
100	Red	1000	Red
101	Magenta	1010	Magenta
110	Brown	1100	Brown
111	White	1110	White
		0001	Gray
		0011	Light blue
		0101	Light green
		0111	Light cyan
		1001	Light red
		1011	Light magenta
		1101	Yellow
		1111	High intensity white

available for each character with blinking available on a per-character basis.

Monitoring the Status of the Video

Executing an 8088 I/O IN instruction from hex address 3DA causes the contents of 74LS244 status register U24 to be read out of the adapter board onto the system board through expansion slot connector P2, as shown in Fig. 2-90.

The circuitry works as follows. An I/O access is initiated by the 8088 CPU pulling IOR* low on pin 9 of 74LS00 NAND U15. Its high pin 8 output is inverted by 74LS04 U16 to place a low on pin 4 of 74LS138 decoder U17. Pin 4 is an active low enable input for U17. Its other active low input (pin 5) must also be low to produce an output from U17. Pin 5 gets its signal from output pin 7 from another 74LS138 decoder (U18). The address from the system board to the I/O circuitry is 3DAH. In binary, this is 1 1 1 1 0 1 1 0 1 0. Thus A9=1, A8=1, A7=1, A6=1, A5=0, A4=1, A3=1, A2=0, A1=1, and buffered address bit BA0=0. With these conditions, 74LS08 AND U41 is qualified producing a logic high out pin 3. Active low A5 and AEN inputs to 74LS138 decoder U18 enable this chip. The input combination of A4, A6, A7, and the U41 output on pin 6 of U18 cause the output pin 7 to go active low enabling the downstream decoder U17.

The input conditions BA0, A1, A2, and A3 on pins 1, 2, 3, and 6 of U17 cause output pin 13 to go low producing (STATUS SEL)*. This signal is passed to the pin 19 output enable of 74LS244 status register U24 allowing the condition of light pen Switch (L PEN SW)*, light pen strobe (L PEN STR), display enable (DISPEN*), and vertical sync delay (VERT SYNC DLY) on pins 13, 15, 17, and 11 to pass through U24 and output as transceiver data TD0 through TD3.

Figure 2-90 shows that TD0 through TD7 are passed through 74LS245 transceiver U66 and exit as data bus information D0 through D7. The program running in the 8088 CPU receives the byte of data and uses D0 through D3 to determine the status of the video circuitry. An active high bit 0 indicates that an I/O video memory access can be made without interfering with the video going to the display. Bit 1 high indicates that a positive transition from the light pen has set the light pen's trigger. This trigger is reset with an I/O OUT command to 3DBH or system power-on. Bit 2 reflects the status of the light pen switch. This bit is low when the switch is on. A high in bit 3 position indicates that the raster is in vertical retrace and screen-buffer updating can be initiated.

Memory Utilization

Two types of memory are mounted on the adapter card. An 8K character generator ROM

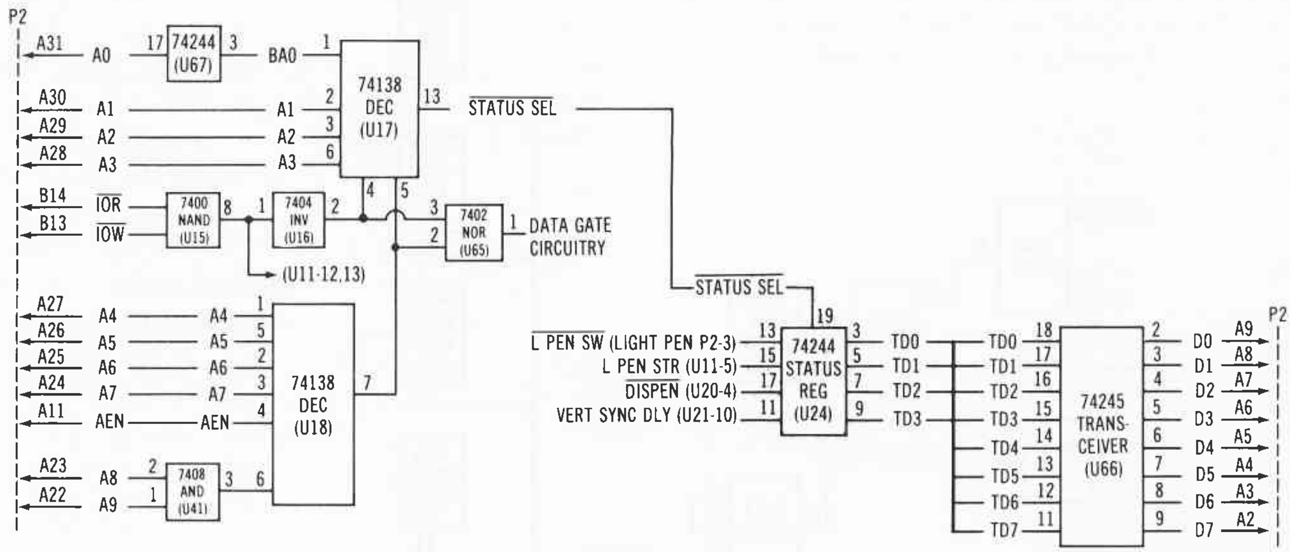


Fig. 2-90. Color status register circuitry.

Table 2-31. RAM Utilization for the Color/Graphics Adapter Card Modes

Mode	Amount of Memory per Screen	Screens of Storage
A/N (40x25)	1000 bytes character 1000 bytes attribute	8 total
A/N (80x25)	2000 bytes character 2000 bytes attribute	4 total
Low-resolution	(not supported in ROM)	
Medium-resolution	200 rows of 320 pixels, 4 pixels defined per byte = 16,000 bytes (C1-C0 per pixel)	1 (memory-mapped)
High-resolution	200 rows of 640 pixels, 8 pixels defined per byte = 16,000 bytes (Pixel P0-P7 per byte)	1 (memory-mapped)

contains dot patterns for 256 different characters in three different font styles. Two of the three font styles are used on the color card: a 7-high by 7-wide double-dot font, and a 5-wide by 7-high single-dot font. The desired font is jumper selected at connection P3. Inserting the jumper selects the single dot 5 by 7 font. Removing the jumper selects the double dot 7 by 7 font.

The other memory is a 16K byte dynamic RAM used to store character and color/attribute information. Table 2-31 lists the memory utilization for each of the video modes.

Alphanumeric data and bit-mapped graphics information are stored in 16K bytes of dynamic RAM. The I/O addresses reserved for this memory are from B8000H to B8FFFH. RAM ICs U50 through U57 are used to store the information which appears on the monitor screen. Storage and access function much like that on the monochrome adapter card. The memory on the color card is slower than the static RAM on the monochrome card so some blinking of the screen display can occur when performing a screen scroll function using the color card.

Color Adapter Board Reset Circuitry

Figure 2-91 shows the circuitry associated with the reset function on the color adapter board. RESET DRV from pin B2 of the system board expansion connector P2 is one input (pin 13) of 74LS86 quad 2-input XOR gate U68. The other input to U68 comes from the exclusive ORing of

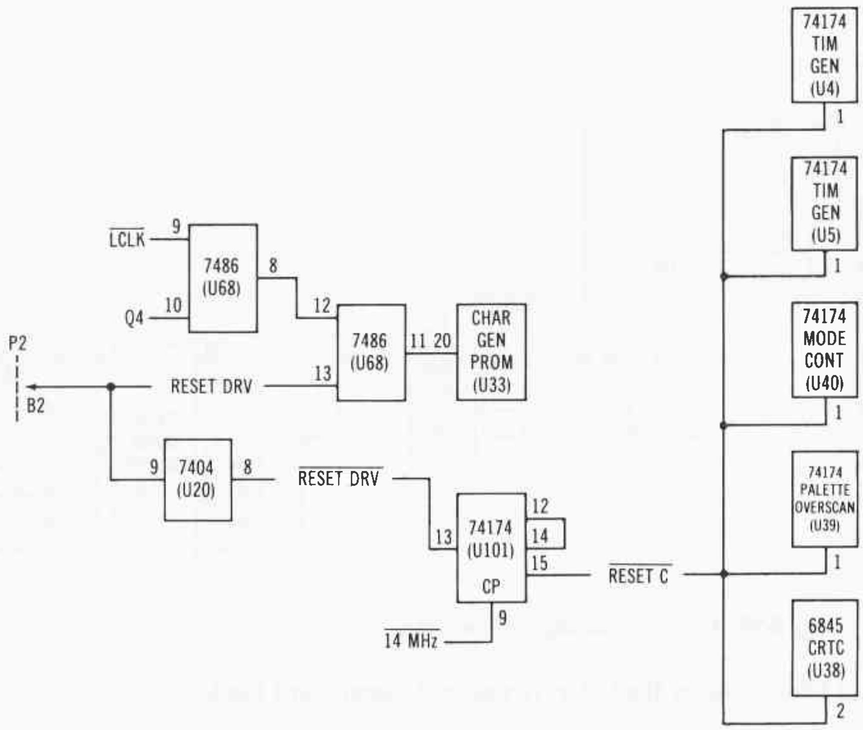


Fig. 2-91. Color reset circuitry.

LCLK* and Q4 in another gate of U68. The output of U68 (pin 11) is applied to pin 20 of character generator PROM U33.

The system board reset signal (RESET DRV) is also applied to 74LS04 hex inverter U20 to generate (RESET DRV)* on output pin 8. This signal becomes the D4 input to 74LS174 hex D flip-flop U101. The Q4 output on pin 12 is routed back into the D5 input (pin 14) to produce (RESET C)* on the Q5 output (pin 15). U101 is clocked by the 14MHz* signal that is generated elsewhere on the adapter board.

(RESET C)* is the primary reset signal for the board. It is connected to the pin 1 master reset input to four other 74LS174 hex D flip-flop chips, timing generators U5 and U14, the mode controller U40, and the palette overscan U39. This reset signal is also applied to the pin 2 reset input to 6845 CRT controller U38.

Video Output Signals

As described in Fig. 2-84, three video outputs are available on the color/graphics adapter: direct drive video and two composite video outputs.

Figure 2-92 covers the circuitry that develops the RGB and intensity direct drive video signals that are available at the edge connector P2. Color data is strobed through two 74LS153 color encoder multiplexers U9 and U10 to become red, green, blue, and intensity information onto output pins 7 and 9.

Multiplexer signals MUX A and MUX B determine the sequential outputs on pins 7 and 9. When the active enable inputs (STR) on pins 1 and 15 are low, the pins 7 and 9 outputs are determined by the select inputs MUX A and MUX B on pins 2 and 14. Table 2-32 lists the output for the various MUX A and MUX B input codes.

As shown in Fig. 2-93, the determination of the logic value for MUX A and MUX B can be quite complex. The alpha serializer data from 74LS166 U32 is ANDed with the pin 3 output from 74LS32 OR gate U14. Its inputs are the NANDed signals AT7, ENABLE BLINK, and CURSOR DLY and the pin 11 output from 74LS393 binary ripple counter U12. Counter U12 is clocked by VERT SYNC DLY. Pin 11 of U13 connects with input pin 4 of 74LS32 NOR U14. Its other input comes from the output of 74LS02 NOR gate U49. The inputs to U49 are the Q3 output of counter U12 and CURSOR DLY. NOR gate U14 combines its input with GRPH* and eventually

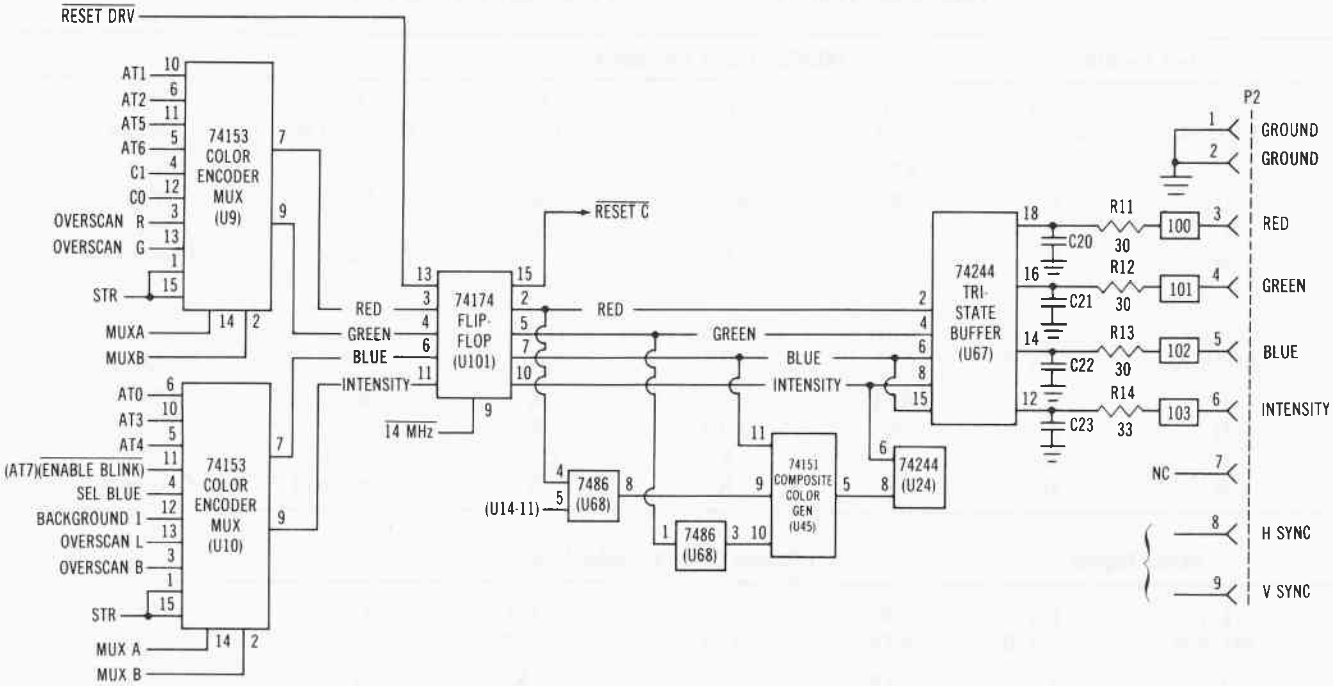


Fig. 2-92. Direct drive color circuitry.

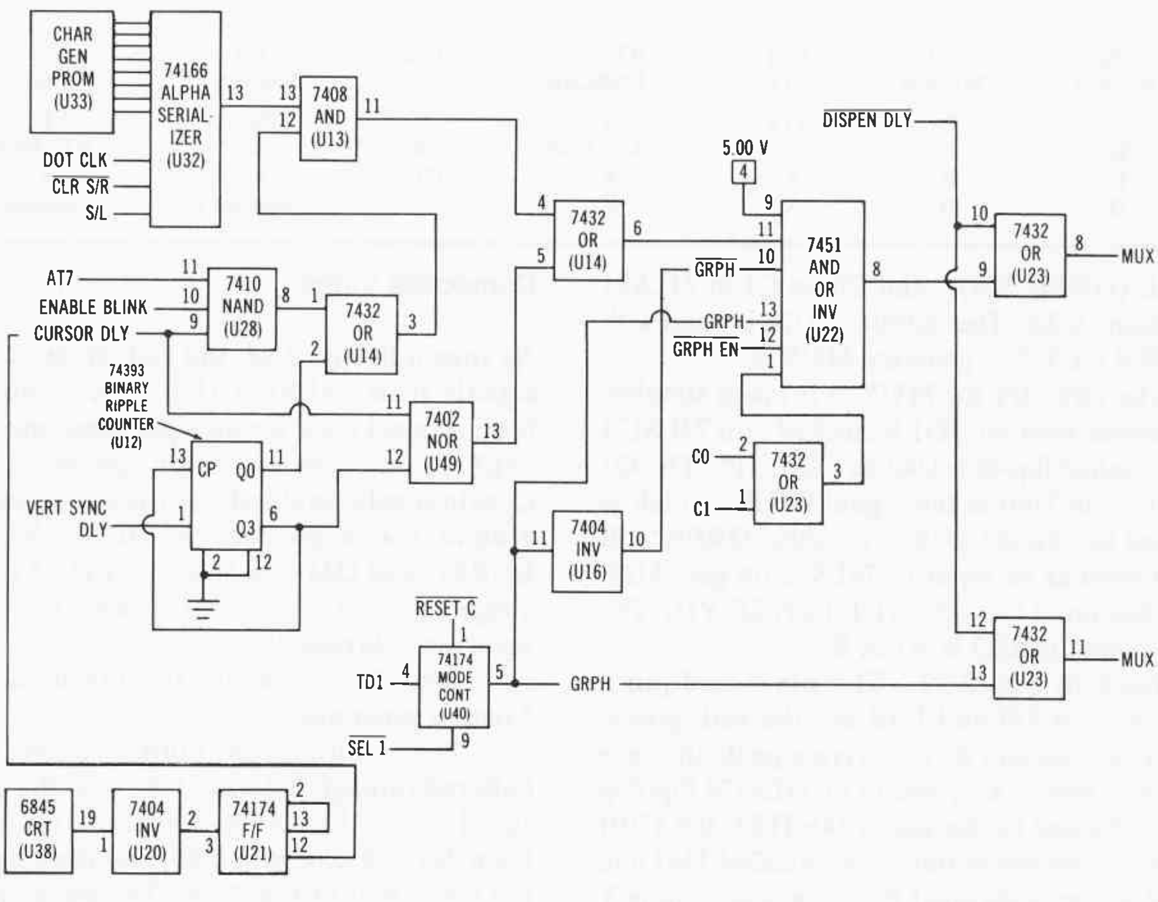


Fig. 2-93. Origination of MUX A and MUX B signals.

Table 2-32. Truth Table for Color Encoders U9 and U10

Select Inputs		74LS153 Color Encoder U9				
(14) MUX A	(2) MUX B	(6) AT2	(5) AT6	(4) C1	(3) Overscan R	(7) Output
L	L	AT2	X	X	X	AT2
H	L	X	AT6	X	X	AT6
L	H	X	X	C1	X	C1
H	H	X	X	X	Overscan R	Overscan R
(14) MUX A	(2) MUX B	(10) AT1	(11) AT5	(12) C0	(13) Overscan G	(9) Output
L	L	AT1	X	X	X	AT1
H	L	X	AT5	X	X	AT5
L	H	X	X	C0	X	C0
H	H	X	X	X	Overscan G	Overscan G

Select Inputs		74LS153 Color Encoder U10				
(14) MUX A	(2) MUX B	(6) AT0	(5) AT4	(4) Set Blue	(3) Overscan B	(7) Output
L	L	AT0	X	X	X	AT0
H	L	X	AT4	X	X	AT4
L	H	X	X	Set Blue	X	SET BLUE
H	H	X	X	X	Overscan B	Overscan B
(14) MUX A	(2) MUX B	(10) AT3	(11) AT7 ENBLNK*	(12) C1	(13) Overscan L	(9) Output
L	L	AT3	X	X	X	AT3
H	L	X	AT7.ENB	X	X	AT7.ENB
L	H	X	X	C1	X	C1
H	H	X	X	X	Overscan L	Overscan L

GRPH, (GRPH EN)*, and C0 OR C1 in 74LS51 AND-OR-Inv U22. The output of U22 is ORed with (DISPEN DLY)* to generate MUX A.

The circuitry for MUX B is much simpler. Transceiver data bit TD1 is clocked into 74LS174 mode control flip-flop U40 by (SEL 1)*. The Q1 output from U40 is the signal GRPH which is inverted by 74LS04 U16 to produce GRPH*. It is also used as an input to 74LS32 OR gate U23. The other input to U23 is (DISPEN DLY)*. The pin 11 output to U23 is MUX B.

Back to Fig. 2-92. The pin 7 and pin 9 outputs from U9 and U10 are the red, green, blue, and intensity direct drive signals that are applied to pins 3, 4, 6, and 11 of 74LS174 flip-flop U101. Clocked by the signal 14MHZ*, the U101 output signals are buffered by 74LS244 U67 and passed across individual RC networks to pins 3, 4, 5, and 6 of direct drive video connector P2.

Composite Video

As shown in Fig. 2-94, the red, green, and blue signals from 74LS174 U101 are combined to form a select code for an eight-input multiplexer 74LS151 composite color generator U45. Continuously enabled with pin 7 strapped to ground, U45 sequences the BLUE, YELLOW BURST, and U44 pins 9, 8, 6 (RED), 5 (CYAN), a logic high on input pin 12, and a logic low on input pin 4 through the chip.

Table 2-33 shows the truth table for the pin 5 output generation.

The multiplexed output from U45 is buffered through 74LS244 U24 with the intensity signal from 74LS174 flip-flop U101, delay signals from 74LS02 NOR gate U65, and the circuitry in the lower half of Fig. 2-94. The serial inputs to 74LS164 serial-in, parallel-out shift register U64

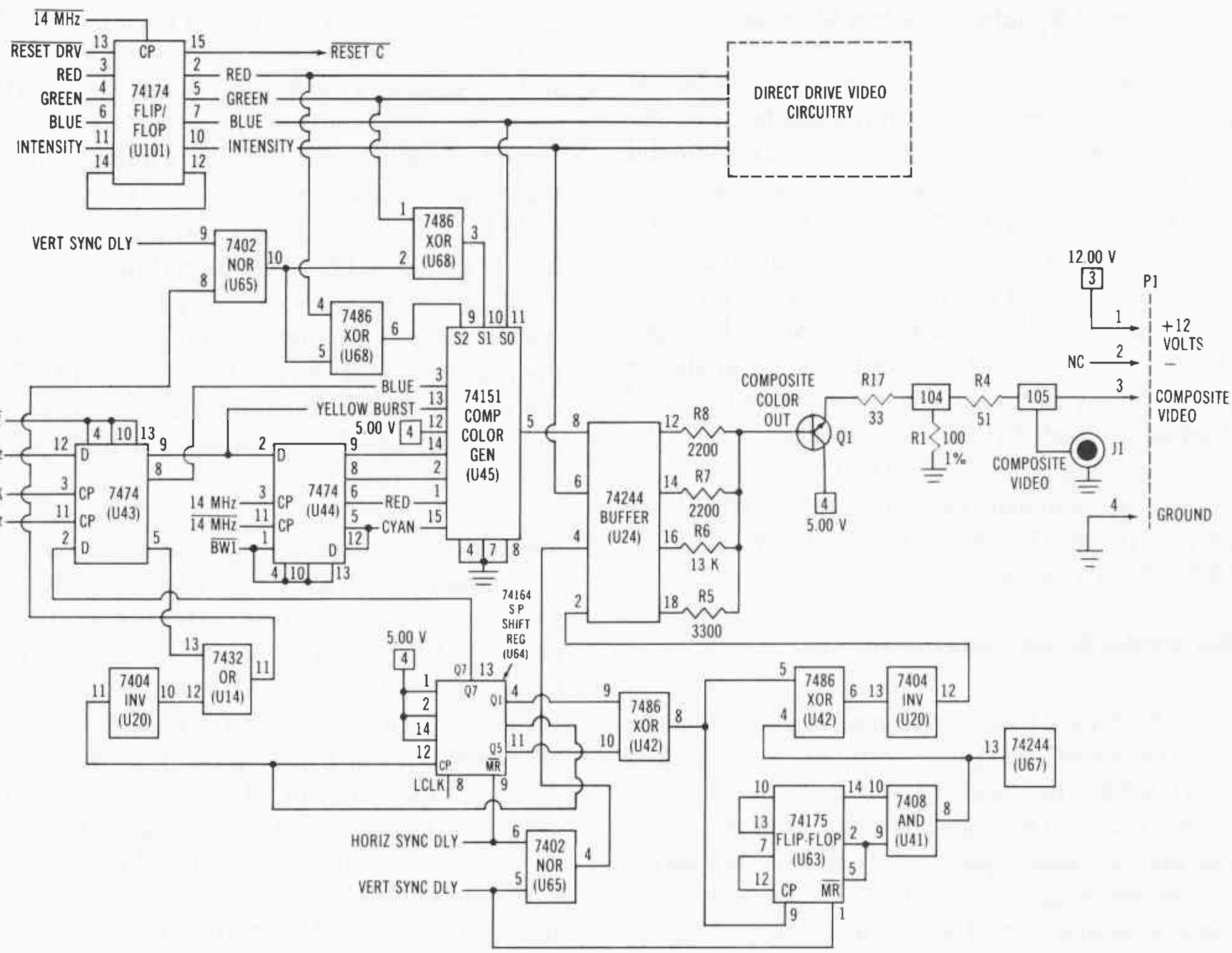


Fig. 2-94. Composite color circuitry.

are strapped high causing two of the eight outputs to become periodically high as clocked by the pin 8 input L CLK. Output pin 4 cycles between two clocks high then two clocks low in a 0 0 1 1 0 0 1 1 ... sequence. Every 32 clock cycles pin 11 toggles.

These two clocked outputs are passed through the XOR gate 74LS86 U42. The output of U42 is connected to another input (pin 5) to 74LS86 U42 and to the clock input to 74LS175 flip-flop U63. An ANDed output from U63 becomes the other input (pin 4) to U42. Its output gets inverted by U20 and passed to the 74LS244 buffer U24 as a timing signal that is combined with the other three inputs to U24 in the resistor-transistor-resistor circuitry on the output of U24. All four sequence signals from U24 are combined in composite color out transistor Q1 to produce the composite video signal that is available at pin 3 of composite video connector P1 or at the RCA jack J1.

Table 2-33. Composite Color Generator Truth Table

(9) S2	(10) S1	(11) S0	(4) I0	(3) I1	(2) I2	(1) I3	(15) I4	(14) I5	(13) I6	(12) I7	(5) Output
L	L	L	I0	X	X	X	X	X	X	X	Ground
L	L	H	X	I1	X	X	X	X	X	X	Blue
L	H	L	X	X	I2	X	X	X	X	X	U44-8
L	H	H	X	X	X	I3	X	X	X	X	Red
H	L	L	X	X	X	X	I4	X	X	X	Cyan
H	L	H	X	X	X	X	X	I5	X	X	U44-9
H	H	L	X	X	X	X	X	X	I6	X	Yel Brst
H	H	H	X	X	X	X	X	X	X	I7	High

Color Board Synchronization Signals

To lock-step the video signals with the horizontal and vertical sweep circuits in the display unit, the color/graphics adapter board generates special synchronization signals that are available at the 9-pin DIN connector J2. The 15.75 kHz horizontal drive and 60 Hz vertical drive signals from the color adapter card are generated by the circuitry shown in Fig. 2-95 (see also CF (CSCS2-B) pages 16, 17). Vertical and horizontal sync signals are generated by the 6845 CRT controller U38 and clocked through 74LS174 D flip-flop U21 by the pin 9 clock signal H CLK. The Q outputs of U21 become vertical sync delay (VERT SYNC DLY) on pin 10 and horizontal sync delay (HORIZ SYNC DLY) on pin 7.

Horizontal Drive Generation

The 15.75 kHz horizontal sync signal begins as HORIZ SYNC out pin 39 of U38. It is clocked by H CLK through U21 to become HORIZ SYNC DLY. This signal is applied to the active low master reset input (pin 9) of 74LS164 serial-to-parallel shift register U64. Because both of the AND inputs (pins 1 and 2) are strapped high, a logic high is clocked through the eight D-latches in U64 by input pin 8 clock signal LCLK. Outputs are taken from four of the eight stages: Q1 on pin 4, Q5 on pin 11, Q6 on pin 12, and Q7 on pin 13. The outputs of interest are the Q1 and Q5 stages. Pins 4 and 11 connect to 74LS86 XOR U42. When either Q1 or Q5 are high, U42 output pin 8 is high. When Q1 and Q5 are low, U42 pin 8 is low. When both Q1 and Q5 are high, U42 pin 8 is also low. The pin 8 output of U42 is the HORIZ SYNC signal that is buffered through U67 to connector J2 pin 8. Therefore, the clocking of a sequence of high inputs through the register under the clock control of LCLK and the master clear control of HORIZ SYNC DLY produces a 15.75 kHz signal out pin 8 of U42 through U67 to J2 pin 8.

Vertical Drive Generation—The 6845 CRTC pin 40 output (VERT SYNC) is clocked through U21 to become VERT SYNC DLY on U21 output pin 10. VERT SYNC DLY is applied to the master reset input to 74LS175 D flip-flop U63 (pin 1). Each time VERT SYNC (U38 pin 40) goes low, all the flip-flops in U63 are cleared. The Q0* output (pin 14) goes high applying a logic 1 to pin 10 of 74LS08 AND gate U41. Pin 4 of U63, the D3 input, is strapped to +5.00 volts causing the flip-flop to enter a high state upon the next low-to-high transition of the pin 9 clock input. Output Q3 (pin 2) connects to input D2 (pin 5). It also connects to pin 9 of U41. A logic high on both of the U41 inputs qualifies the AND

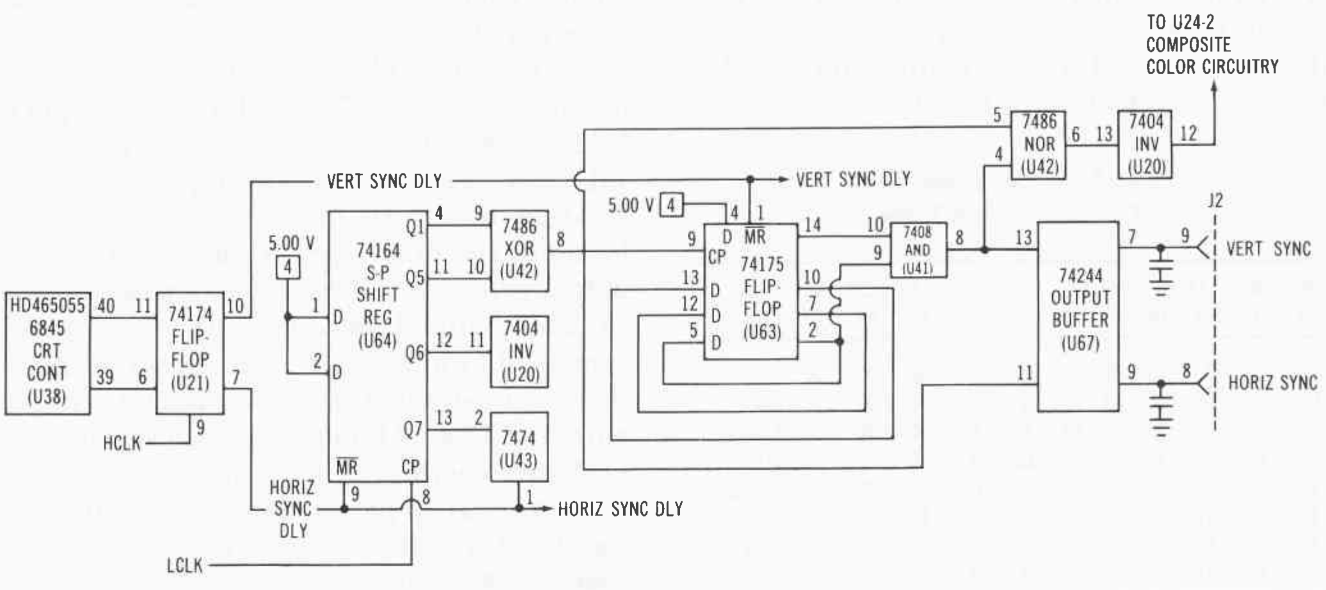


Fig. 2-95. Horizontal and vertical sync circuitry.

gate generating a high on pin 8. This high signal is buffered through 74LS244 U67 as a vertical sync signal at pin 9 of connector J2.

Meanwhile, back at U63, the pin 5 D2 input went high so on the next low-to-high clock transition, Q2 (pin 7) goes high. This output pin is connected to the D1 input pin 12. Output pin 10 (Q1) connects to D0 input (pin 13). And output pin 14 (Q3) connects to pin 10 of U41. Therefore, Q3 goes high and remains high for four clock cycles before Q3 returns low. Q3 remained high all during the cycle until another master reset pulse occurs on pin 1 momentarily clearing Q3 disabling pin 9 of U41. In this fashion, using the horizontal sync signal as a clock into pin 9 of U63, the occurrence of VERT SYNC DLY, and the four-step flip-flop of U63, the output of J2 pin 9 becomes a 60 Hz vertical sweep circuit synchronization signal.

FLOPPY DISK DRIVE INTERFACE

The IBM 5¼ inch diskette drive adapter that plugs into one of the expansion slots has connections for two internal and two external double density disk drives. The adapter works in the IBM System 34 double density format "Modified Frequency Modulation" (MFM) with write precompensation and an analog phase-lock loop for clock and data recovery. The adapter is buffered on the system I/O bus and uses DMA for data transfer to and from the storage disks in the drives. To the system board the diskette adapter (and hence the disk drives) looks like three I/O locations: an output register at location 3F2H, an input status register at location 3F4H, and a bidirectional data register at location 3F5H. (Refer to COMPUTERFACTS CSCS2-C for this discussion.)

The heart of the disk drive electronics is an NEC microprocessor D765 or equivalent floppy disk controller (FDC) labelled U6 in Fig. 2-96. The FDC controls the operation of up to four double density disk drives. It simplifies the architecture of write precompensation and phase-locked loop read circuitry. As the figure shows, U6 is comprised of a data bus interface buffer, DMA read/write control logic, a main status register and data register, serial interface control for the drives, and drive interface control for reading, writing, and head control.

Handshaking signals enable DMA interface with the DMA controller on the system board. The FDC will operate in both DMA and non-DMA modes. In the non-DMA mode, U6 generates an interrupt to the 8088 CPU on the system board every time a data byte is to be transferred. For DMA operation, the 8088 CPU loads a command into the FDC and data transfer occurs under control of the FDC and the DMA controller.

FDC U6 can execute up to 15 high level disk commands including formatting a disk, seeking, writing data, writing a deleteted track, reading data, reading ID, reading a track, reading deleted data, and sensing interrupt and drive status. Multiple 8-bit bytes specify which operation is to be performed.

Data synchronization and error checking is performed automatically by U6 for reliable data storage and retrieval. External circuitry is used to generate master clock and write clock signals for the FDC and for data separation during read operations. FDC U6 also generates control signals for start-up and data separator base frequency selection. Because the 765 FDC can interface to a large number of disk drives, the BIOS software sends commands to U6 to specify the track stepping rate, and the head load and unload times.

Figure 2-97 describes the pin assignments for the FDC designed into the IBM PC diskette adapter board. Some pins are not used. Pin 26 (MFM) is a flag output identifying the mode configuration of U6. Because the board operates in MFM all the time, this status condition is not required; therefore, pin 26 is not used.

Pins 28 and 29 (unit select 0, 1) are available to select one of four floppy disk drives in a system. A different drive select design is used on the diskette adapter board.

Finally, pin 36 (HDL) is not used to cause the drive read/write head to contact the disk. The drives used with this adapter have their own

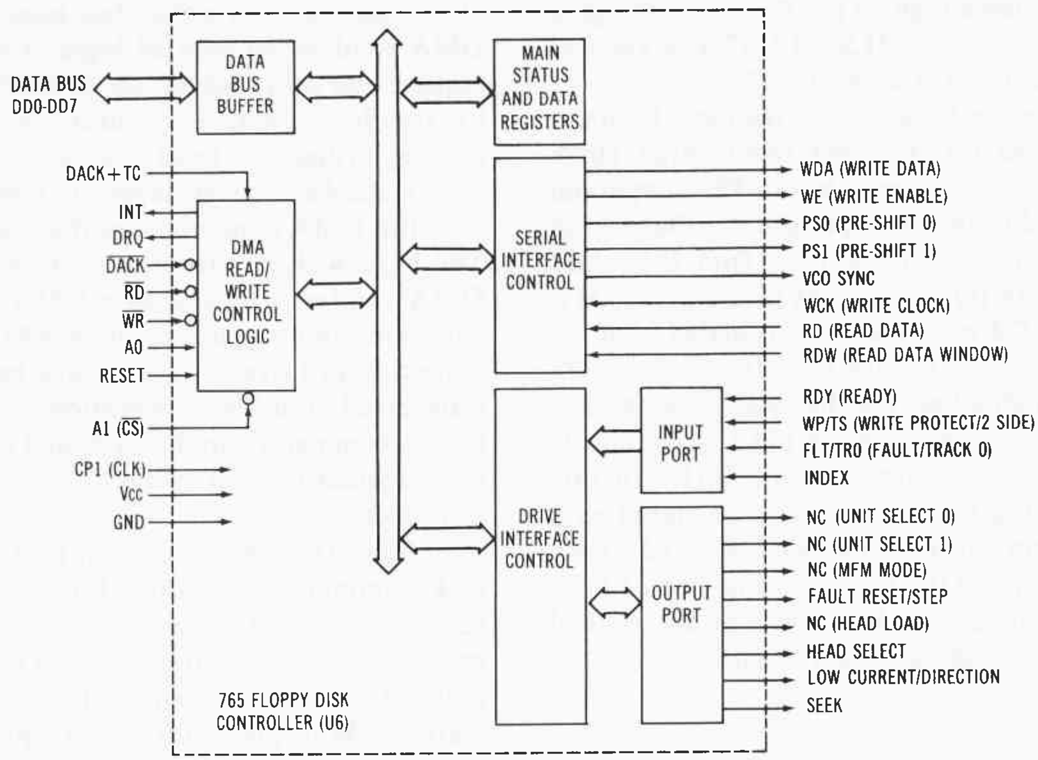


Fig. 2-96. The 765 FDC internal block diagram.

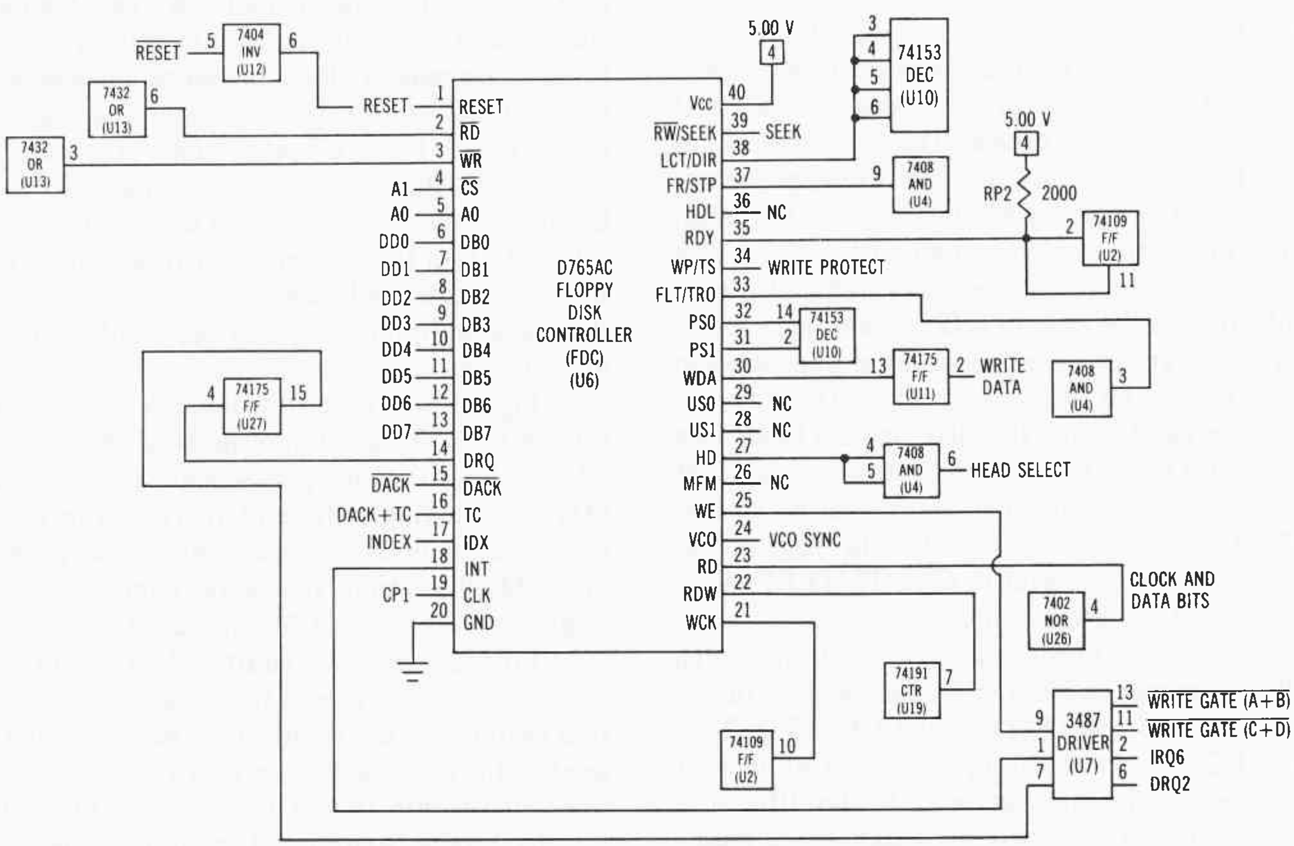


Fig. 2-97. Floppy disk controller pin assignments.

head-positioning system that moves the magnetic head so it contacts the desired track on the disk. A stepper motor and band assembly in the drive uses one-step rotation to cause a single-track linear movement of the head. Because no other system or operator intervention is needed during normal operation, a signal out pin 36 is not required.

Table 2-34 describes the function of each 765 FDC pin.

FDC Operation

The main status and data registers can be accessed by 8088 CPU using addresses 3F4H and 3F5H. The 8-bit read-only main status register contains information related to the condition of the FDC. This register can be accessed at any time. The 8-bit data register is actually a window into one of four registers in a stack. The stack stores data, commands, parameters, and disk drive status information. Bytes of data are read out or written into the data register to program the drive electronics or to pull out status information after execution of a command. Table 2-35 describes how the registers are accessed.

Main Status Register

Data is read from or written to the FDC registers by the combination of A0, RD*, WR*, and A1 (chip select). The eight bits in the main status register byte are defined, as shown in Table 2-36. A1 must be active low to enable A0, RD*, and WR* control of the registers.

FDC Operational Phases

Multibyte transfers of information between the 8088 CPU and the 765 FDC during disk drive command initiation and post-execution. A command consists of a command phase, an execution phase, and a result phase. Data byte transfer must occur in a specified order. The command code is sent first, followed by the other bytes in a prescribed sequence. A data book describing the 765 FDC lists the byte sequence required.

During the command phase, U6 receives the information necessary to perform an operation. The executing program transfers disk operation information to the FDC data register. This occurs after a system reset and after completion of a previous command.

During the execution phase, the FDC performs the instructed operation. This phase ends when the last byte of data has been transferred (as signaled by TC from the 8237 DMAC to the FDC) or the occurrence of an error.

After the disk operation has been executed, the FDC enters the result phase. In this phase, status and housekeeping information is available to the 8088 CPU. All the bytes (typically seven) available in the result phase must be read to complete the read data command. A new command will not be recognized until all the seven bytes have been read out. After the CPU reads the FDC data register information, U6 reenters the command phase again and is ready to accept another command.

Writing data to or reading data from the FDC data register during the command and result phases is initiated with the 8088 accessing the FDC main status register to determine if the data register is available. Bits 6 and 7 must be low and high respectively before a command byte can be written into U6. During the result phase, bits 6 and 7 must both be high to enable reading from the FDC main status register.

Data transfers to, or from, the disk drive occur in the execution phase. During DMA transfers, a DRQ signal is generated out pin 14 of U6. This signal is passed through 74LS175 flip-flop U27 and out pin 6 of 3487 driver U7 as DRQ2. DRQ2 signals the 8088 that a DMA request has been made. The 8237 DMA controller on the system board responds by generating DMA acknowledge 2 (DACK2*). This signal becomes DACK* and DACK&TC. DACK* enters pin 15 of U6 signaling acknowledgment of the request. RD* or WR* is also generated by the 8237 DMAC. During the last transfer of data, the DRQ signal is reset. After the last data transfer, pin 18 INT becomes active high producing IRQ6 out pin 2 of U7.

Table 2-34. 765 Floppy Disk Controller Pin Functions

Signal	Pin	I/O	Function
RESET	1	I	Reset: Places FDC in idle state. Pulls output lines low. Doesn't clear last specify command.
RD*	2	I	Read: Active low signal that allows data transfer from FDC to I/O data bus. Disabled when CS* high.
WR*	3	I	Write: Active low signal allowing data transfer to FDC from data bus. Disabled when CS* high.
A1	4	I	Address Bit 1 (chip select): Active low address bit signal that allows RD* and WR* to be enabled.
A0	5	I	Address bit 0 (data/status select): Determines if data register (A0=1) or status register (A0=0) contents can be passed to data bus.
DD0-DD7	6-13	I/O	Data bus: Bidirectional data bus interface that is disabled when CS* is high.
DRQ	14	O	DMA request: Active high signal used to generate DRQ2 DMA request to 8088 CPU.
DACK*	15	I	DMA acknowledge: Active low when DMA cycle is active and DMAC on system board is controlling data transfer.
DACK&TC	16	I	DMA acknowledge and terminal count: The active high result of combining the DACK2* and TC signals from the system board to indicate the end of a DMA transfer. Ends read/write/scan commands in DMA or interrupt mode.
INDEX	17	I	Index: Active high to indicate the head has just detected the beginning of a new disk track.
INT	18	O	Interrupt: An FDC interrupt request that produces IRQ6 for the system board circuitry.
CPI	19	I	CPI (clock pulse): 4 MHz single phase square wave clock used to pulse the FDC circuits.
GND	20		Ground: DC power return.
WCK	21	I	Write clock: Sets the floppy disk drive write data rate to a 250 ns 1 MHz pulse. Enabled for both read and write operations.
RDW	22	I	Read data wimdow: Phase-locked loop generated signal used to sample data from disk drive.
RD	23	I	Read data: Composite data from drive that contains clock and data information.
VCO SYNC	24	O	VCO Sync: Inhibits voltage controlled oscillator in phase-locked loop when low. Enables VCO in PLL when high.
WE	25	O	Write enable: Used to generate (WRITE GATE A&B)* and (WRITE GATE C&D)* signals that enable write data into the disk drive.
MFM	26	O	Modified frequency modulation: Status output—not used.
HD	27	O	Head (select): Selects magnetic head 1 when high, head 0 when low.
US0, US1	28, 29	O	Unit select 0, 1: not used.
WDA	30	O	Write data: The serial clock and data that is output to disk drive electronics.
PS0, PS1	31, 32	O	Pre-shift 0, 1: Write precompensation status signals that determine early, late, and normal timing signals.
FLT/TR0	33	I	Fault/track 0: Senses drive fault condition in read/write mode and track 0 condition in seek mode.
WP/TS	34	I	Write protect/two side: Senses write protect status in read/write modes and two side media in seek mode.
RDY	35	I	Ready: Tied high through RP2 to indicate disk drive always ready to send or receive data.
HDL	36	O	Head load: not used.
FR/STP	37	O	Fault reset/ step: In read/write mode this signal resets fault flip-flop in the disk drive. FR pulse issued at beginning of each read/write command. In seek mode, FDC (U6) outputs step pulses to move the head to another cylinder track.
LCT/DIR	38	O	Low current/direction: In read/write mode this signal lowers write current on inner tracks; in seek mode it determines the direction the head will move when it receives a step pulse.
RW*/SEEK	39	O	Read write/seek: Specifies read/write mode when low and seek mode when high.
Vcc	40		Vcc: +5 volt DC power.

IRQ6 indicates that the execution phase has ended and the result phase is beginning. It causes a program jump to an interrupt handling routine that examines the result bytes and resets the interrupt request. The terminal count (TC) output from the 8237 DMAC enters the drive adapter board and is ANDed with an inverted DACK2* signal to produce a DACK&TC input to pin 16 of U6. This indicates that the byte of data initialized for DMA count is now being transferred.

During non-DMA, transfer request bit 7 in the main status register and the INT signal on 765 FDC pin 18 are both high. INT becomes IRQ6 for the interrupt-driven IBM PC system. Master request (bit 7) is used in software controlled architectures where polling is used to determine the status of the system. When IRQ6 is received by the 8088 CPU, it responds by reading data from U6 (RD* pulled active low) or writing data to U6 (WR* pulled active low). This disables the transfer request. When a transfer request has been received by the 8088 CPU for the last data byte, the system board causes a high to occur on pin 16 (DACK&TC) of U6. This occurs before the last data byte has actually been sent (or received).

Table 2-35. Decoding for Register Access

A0	RD*	WR*	Function
0	0	1	Read main status register
1	0	1	Read data register contents
1	1	0	Write data register

* (all other code combinations are illegal)

Once pin 16 of U6 goes high, the FDC stops requesting data transfers. U6 will continue to read from or write data to the disk until the end of the current disk sector is reached. Data read from the disk after TC occurs will be discarded. A cyclic redundancy check will be made. During a disk write, once terminal count has been reached, data output shifts to zeroes and the remainder of the sector is filled with zero bytes.

Table 2-36. Main Status Register Bit Definition

Bit	Name	Description
0	DRIVE 0 BUSY	Drive 0 is in seek mode.
1	DRIVE 1 BUSY	Drive 1 is in seek mode.
2	DRIVE 2 BUSY	Drive 2 is in seek mode.
3	DRIVE 3 BUSY	Drive 3 is in seek mode.
4	FDC BUSY	FDC read/write command in proces.
5	NON-DMA MODE	FDC in non-DMA mode. Set during execution phase. Low when phase has ended.
6	DATA I/O	Direction of data transfer for data register and FDC. high = transfer from data register to 8088 CPU. Low = transfer from 8088 CPU to data register.
7	MASTER RQST	Indicates data register ready to send or receive data. Used with bit 6 to perform handshaking of "ready" and "direction" with 8088 CPU.

FDC (U6) Electronics

FDC U6 performs six functions on the disk drive adapter board: One, it manages the selection of up to four disk drives.

Two, it controls track selection by issuing timed step pulses that move the magnetic head from its current location over a track cylinder to another specified cylinder for data reading or writing. FDC U6 stores each cylinder number being accessed by the head and computes the stepping distance to the next cylinder. It also manages the head select signal to activate the correct side of the diskette.

Three, it monitors the track data until it senses a requested sector (sector selection). Seek time is specified at 6 ms track to track.

Four, it controls head loading at 35 ms and causes the head to hold for 15 ms settling time before writing or reading, and head loading after read/write operations. Therefore, the head is loaded 35 milliseconds before a read/write access. Following access, the head is held 15 milliseconds before reading or writing. The motor is held powered up for 250 ms before head cylinder movement occurs.

Five, the FDC outputs the READ DATA composite signal (clock and data) into a data separation circuit at 500K bits/second for the double-density disks so the clock and data can be converted into two signal streams. The serial data is also assembled into 8-bit bytes and transferred to memory every 16 microseconds. Data separation is achieved using a phase-locked loop (PLL). After synchronizing with the data stream, the separation logic provides a data window to the FDC that differentiates data from clock information. FDC U6 uses this window to reconstruct the data that was previously recorded on the disk.

Finally, the FDC electronics includes cyclic redundancy check (CRC) circuitry to check for standard soft errors. As data is written onto the disk, a 16-bit CRC value is computed and also stored on the disk. When the data is later retrieved off the disk, a CRC value is computed on the read data and compared to the stored CRC value of the original data. If a match occurs, all is well. A mismatch results in a CRC error and a read retry by the system.

Disk Drive Electronics

Inside each disk drive connected to the adapter board are circuits that translate digital command signals into electromechanical actions (for example, drive selection, head movement, and head loading) and that sense and provide disk or drive status (for example, ready to read/write, write fault, and write protect) back to the adapter board circuitry. There is also analog circuitry that senses, amplifies, and shapes data pulses read from, or written to, the disk by the magnetic head.

Table 2-37 describes the adapter board input and output signals.

Table 2-37. Disk Drive Adapter Input and Output Signals

Signal	Description
Outputs:	
DRIVE SELECT (A & B) (P2-12,14)	Enables drive I/O for a selected drive. All other drivers and receivers (except motor enable) are disabled.
MOTOR ENABLE (A & B) (P2-10,16)	Controls the spindle motor in the selected drive. Pulling one of these lines active low starts the specified drive motor.
STEP (A & B) (P2-20)	Causes the selected drive read/write head to move one cylinder track in or out for each pulse depending on the direction selected by the signal on P2 pin 18.
DIRECTION (A & B) (P2-18)	Causes the head to move one cylinder toward the spindle for each step pulse if active high and one cylinder away from the spindle if active low.
SEL HD 1 (A & B) (P2-32)	Selects the upper head (head 1) when active low. Selects head 0 when high.
WRITE DATA (A & B) (P2-22)	Causes a flux change to be recorded on disk for each low to high transition while write enable is high.
WRITE GATE (A & B) (P2-24)	Disables write current in head unless active low.
Inputs:	
INDEX (A & B) (P2-8)	A pulse from the selected drive each time the index mark is detected during disk revolution.
READ DATA (A & B) (P2-30)	Pulse occurs on this line for each flux change sensed by read head of selected drive.
TRACK 0 (A & B) (P2-26)	Active when the read/write head of the selected drive is over track 0.
WRITE PROTECT (A & B) (P2-28)	Pulled active by the selected drive if a write-protected disk is detected in the drive.

Data Recording Technique

MFM data recording is used by the double density disk drive circuitry for encoding and decoding data stored on floppy disks in the IBM PC system. In MFM encoding data bits are written inside a bit cell time. During the write data execution phase, data transfers between the 8088 CPU and the 765 FDC occur every 15 microseconds. The presence of a data bit represents a binary 1; the absence of a bit represents a binary 0. The data bits are written in the center of a bit cell with a clock bit written at the leading edge of the bit cell only if no data bit was written in the previous bit cell and no data bit is to be written in the present bit cell. This leads to a somewhat complex looking data/clock pattern but a denser data storage capability.

Disk Format

Each of the soft-sectored disks used in a PC disk drive has 40 tracks (cylinders) divided into 8 sectors per track (9 with DOS 2.0 and 2.1 operating systems) and 512 bytes per sector. This yields 327,680 bytes per disk in 8 sectors per track systems and 368,640 bytes per disk in 9 sectors per track systems.

Each of the 40 tracks on a floppy disk are partitioned into five sections, as shown in Table 2-38.

Each sector in a track is comprised of four fields as described in Table 2-39.

Table 2-38. Partitioning of a Track

Section	Function
Pre-index gap	Gap 5—written during formatting.
Index address marks	A unique code indicating the beginning of a data track. One index mark is written on each track during formatting.
Post index gap	Gap 1—used during read/write operations to synchronize data separator logic with data to be read from ID field of first sector. Writ-ten only during formatting.
Sectors	Four fields of data written during formatting and repeated for each sector on the disk. One field holds the data to be stored during write operations.
Final gap	Gap 4—written during formatting. Extends from last physical data field on track to physical index mark.

System Board Interface

With an understanding of how the disk drive and disk adapter circuitry generally function, it's appropriate to take a closer look at how the IBM adapter board implements MFM recording and data retrieval. Figure 2-98 shows the system board expansion interface to the circuitry on the disk drive adapter board.

Ten address bits are connected to the adapter board to access the three I/O location registers–3F2H for the 74LS245 digital output register (U30) in the lower left of Fig. 2-98; 3F4H for the FDC main status register; and 3F5H for the FDC data register. For all three of

Table 2-39. Sector Field Partitioning

Field	Function
Sector ID field	Consists of seven bytes written during formatting. Provides sector identification to FDC. Byte 1 is FDC-provided unique coding ID address mark specifying the beginning of ID field. Bytes 2, 3, and 4 are cylinder, head, and sector addresses provided by the disk operating system. Byte 5 is the DOS-supplied sector length code. Bytes 6 and 7 are 16-bit CRC character value for ID field. This value is computed by the FDC from the data in the first five bytes.
Post ID field gap	Gap 2—written during formatting. During later write operations, drive write circuitry is enabled during gap time. Trailing bytes of gap rewritten each time sector is written into. During read operations, trailing bytes of gap used to synchronize data separator logic with upcoming data field.
Data field	Length determined by operating system during formatting. Byte 1 is data address mark specifying beginning of data field. Last two bytes comprise CRC character.
Post data field gap	Gap 3—written during formatting. Separates preceding data field from next physical ID field on track. Contains programmable number of bytes. Following write operation, drive write logic is disabled during Gap 3. Size large enough to contain disk surface data discontinuity during drive write current turn on and off and to contain synchronization field for next sector's upcoming ID field.

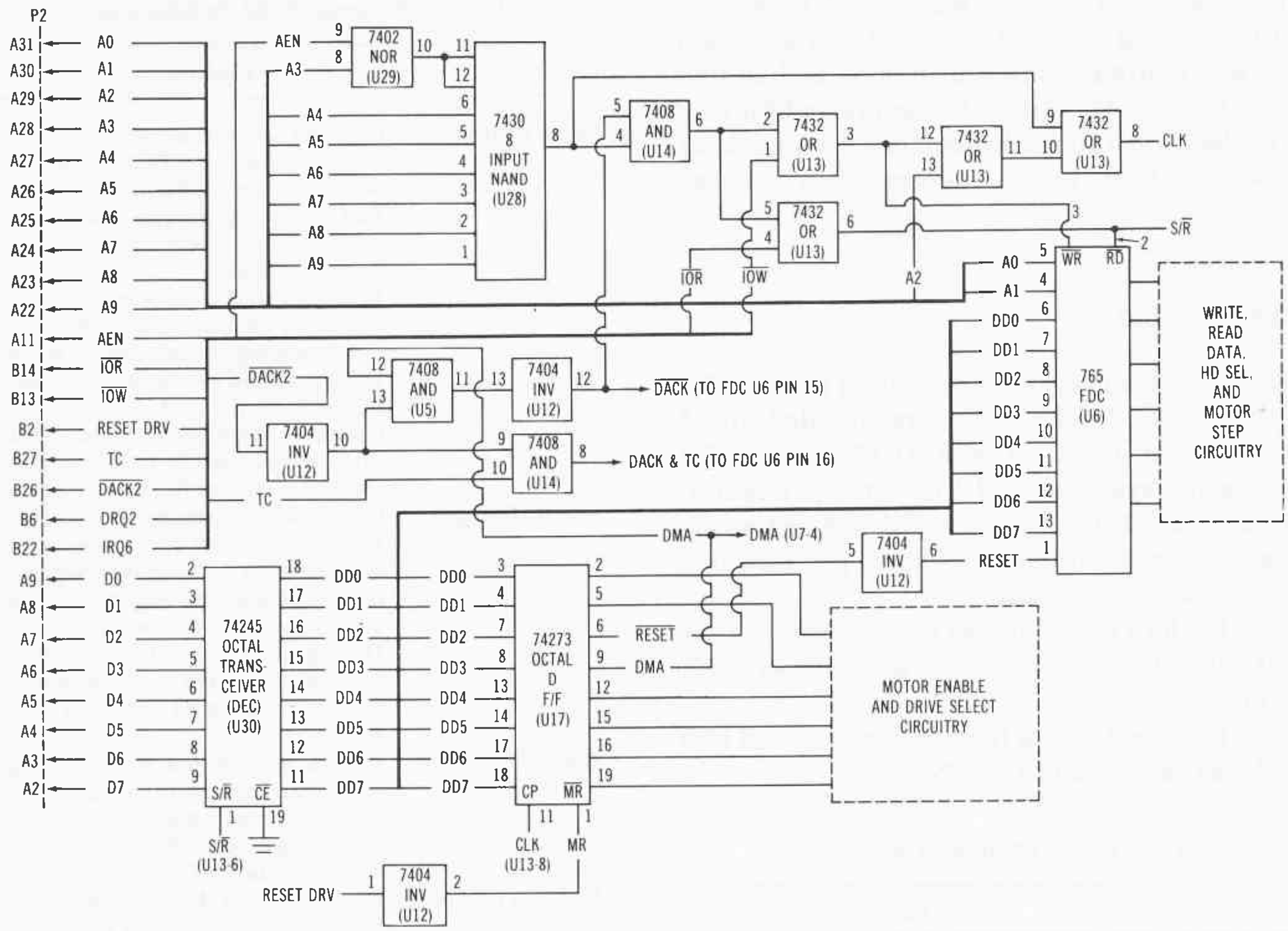


Fig. 2-98. System board to drive adapter board interface circuitry.

these addresses, address bits A4 through A9 are high and bit A3 is low.

Digital output register U30 is a bidirectional octal transceiver with direction of data flow controlled by the S/R* input on pin 1. This control signal is derived by the circuitry in the upper part of Fig. 2-98. Address bit A3 and address enable signal AEN are applied to the 74LS02 NOR gate U29 to produce the pin 11 and 12 inputs to 74LS30 8-Input NAND U28. The other six inputs to U28 are A4 through A9 directly off the address bus. The pin 8 output of U28 is ANDed with DACK* from U12 and applied to two separate inputs to 74LS32 U13. The top input (pin 2) is used to generate an input write control signal to pin 3 of 765 FDC U6. It is also used to generate a clock signal (CLK) that pulses data through 74LS273 octal D flip-flop U17 and into the motor enable and drive select circuitry. CLK also causes U17 to produce the DMA and RESET* pulses used elsewhere in the circuitry.

The other half of U13 receiving the output from U14 is on pin 5. This input combines with IOR* from the P2 expansion connector (pin B14) to produce S/R* out pin 6. This signal controls the direction of data flow through U30. It also acts as an active low control signal for the 765 FDC U6. This signal allows the transfer of data from U6 to the expansion I/O bus. It is disabled internally in U6 when A1, the FDC chip select (pin 4) is high.

The other two addresses 3F4H and 3F5H vary by the condition of bit A0, the DATA/STATUS SELECT input to U6 (pin 5). When A3 is low, and A4 through A9 are high (0 0 1 1 1 1 1 1 0 x x x), an active high A2 causes the generation of CLK out pin 8 of U13 (top right in

Fig. 2-98). CLK pulses the data bus to output DD3 (pin 8 of 74LS273 octal D flip-flop U17 as a pin 9 DMA signal. DMA is tied to control pin 4 of 3487 driver U7. This makes the qualifying code (0 0 1 1 1 1 1 1 0 1 x x). The condition of address bit A0 determines if the FDC data register (A0 = high) or main status register (A0 = low) will be passed to the data bus out pins 6 through 13 of U6.

Adapter Board Clock Circuitry

Figure 2-99 shows the circuitry on the disk drive adapter board that generates the CLK, CPI, 16 MHz, and 2 MHz clock signals. As described in the previous section, address bits A2 through A9 (CF (CSCS2-C), pages 4 and 21) are used to generate the CLK signal output from pin 8 of 74LS32 OR gate U13. The CLK signal is used to drive 74LS273 octal D flip-flop U17.

A 16 MHz voltage controlled oscillator is used to generate the remaining three clock signals (16 MHz, 2 MHz, and CPI) in the clock/data separator circuitry. Exiting pin 3 of U1, 16 MHz is passed across connector P3 to the pin 4 clock input of 74LS09 flip-flop U2 and pins 1 and 13 of 74LS112 dual JK flip-flop U22. The active high input of U2 is passed out the Q* output (pin 7) to clock a 74LS93 4-bit counter U3. U3 generates a 4 MHz CPI signal and a 2 MHz signal. CPI is used to clock 765 FDC U6 and a 74LS175 flip-flop U11 in the precompensation circuitry. The 2 MHz pulse stream out pin 9 of counter U3 clocks 74LS175 flip-flop U27 to pass the DMA request signal DRQ on input pin 4 out pin 15 as the DMA request 2 signal DRQ2 that is coupled through pin B22 of I/O connector P5 onto the system board.

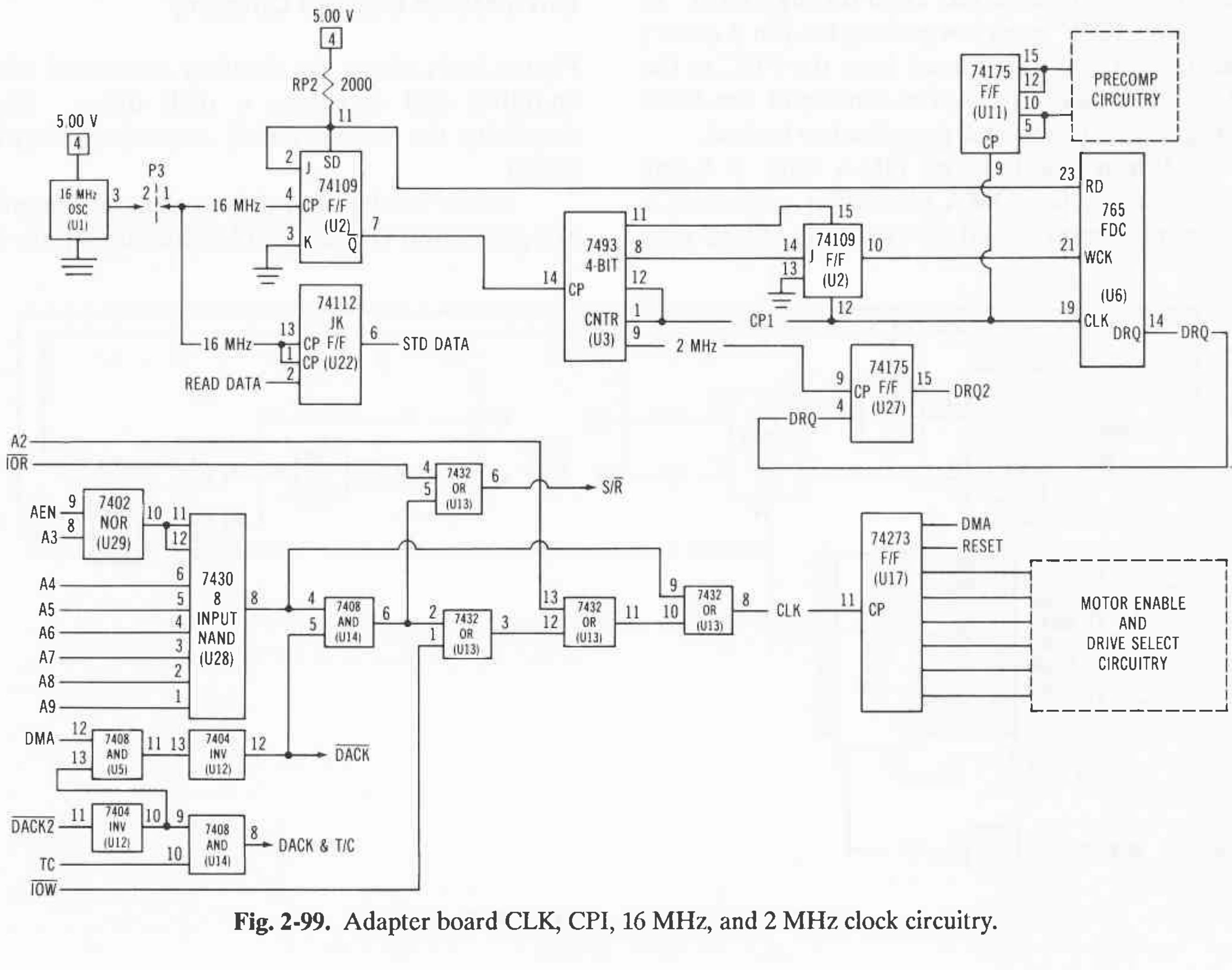


Fig. 2-99. Adapter board CLK, CPI, 16 MHz, and 2 MHz clock circuitry.

DMA Circuitry

Whenever I/O locations 3F4H or 3F5H are accessed, the clock signal CLK is generated and the internal registers of U6 are read. When U6 is ready to transfer a byte of data to or from the floppy disk, U6 pulls pin 14 (DRQ) high causing 3487 driver U7 to produce a DMA request signal (DRQ2) to pin B22 of P5, as shown in Fig. 2-100.

As discussed earlier in this chapter, DMA action occurs on the system board. The CPU relinquishes bus control to the 8237 DMA controller and it communicates with the drive adapter board to cause data transfer. The DMA controller generates an active low DMA acknowledge signal (DACK2*) that is inverted by U12 and ANDed with DMA from U17 to produce an active low DACK* signal for pin 15 of U6. Pin 15 active low disables U6 output pin 14 and selects the data register in U6 as the source, or destination, of data bus DD0 through DD7. In addition IOR* goes low pulling U6 pin 2 (RD*) so data can be transferred from the FDC to the I/O data bus. If a write command has been programmed, WR* will go active low instead.

When the byte of DMA data is being transferred, the DMA controller generates a terminal count signal (TC) that is ANDed with the now high DACK2* signal to produce a DACK&TC signal for U6 input pin 16. This signal indicates the end of a DMA transfer. This causes an interrupt signal to occur on U6 output pin 18 signifying the beginning of the FDC result phase. Pin 18 connects to pin 1 of 3487 driver U7. Under control of DMA on pin 4, U7 passes the interrupt signal out pin 2 as IRQ6 and through connector P5 onto the system board and into the programmable interrupt controller (PIC). The PIC, in turn, generates an interrupt to the 8088 CPU and an interrupt handler routine is accessed. When the first of the seven bytes of data is read out of the FDC during this result phase, the pin 18 interrupt signal is reset. Any data sheet on the 765 FDC part will describe the data bus contents during the various phases of controller operation.

Drive Motor Control Circuitry

Figure 2-101 shows the circuitry associated with enabling and selecting a disk drive. For simplicity, the drive A and B control circuitry is shown.

Motor enable and drive select commands are generated via the DMA data bus inputs to

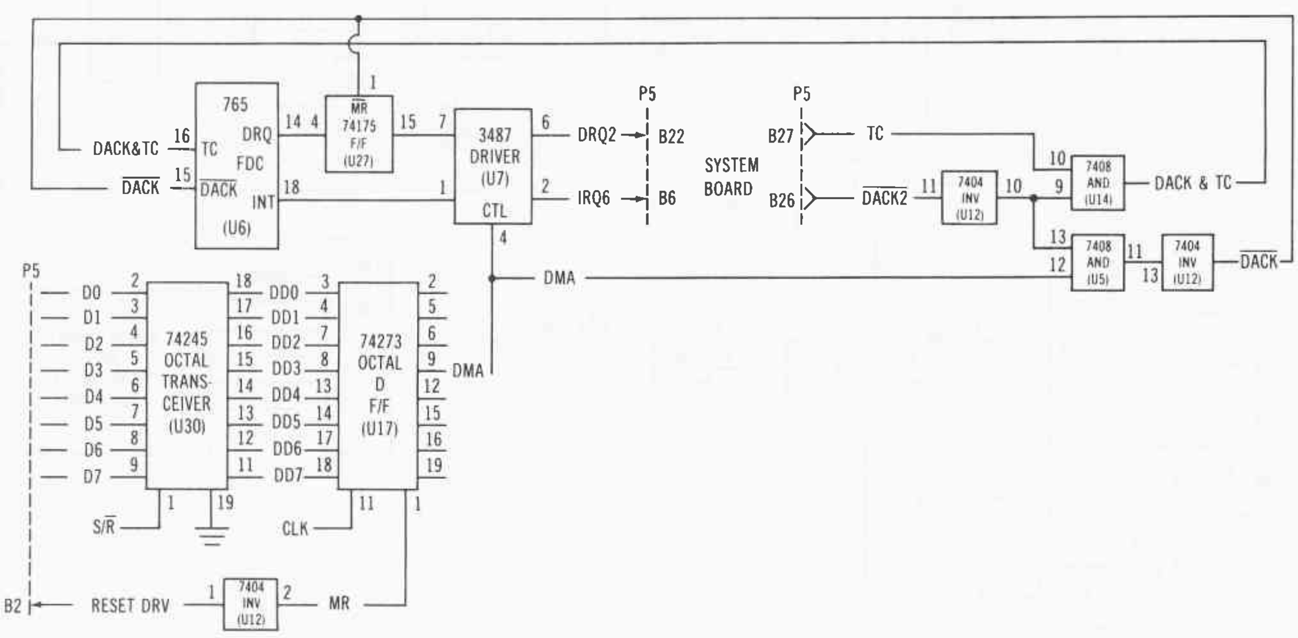


Fig. 2-100. Disk drive adapter DMA circuitry.

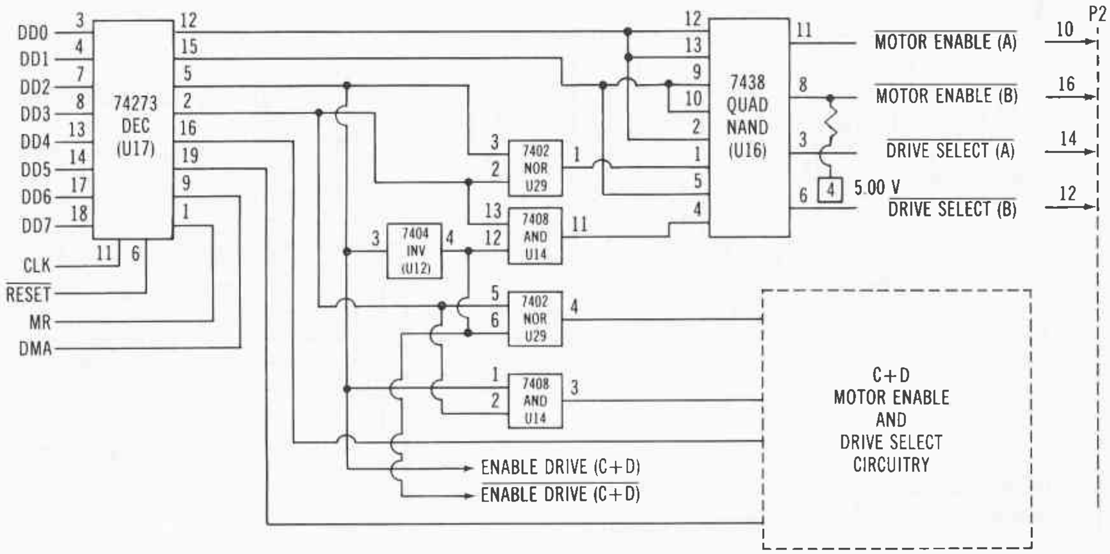


Fig. 2-101. Drive motor control circuitry.

74LS273 octal D flip-flop U17. The outputs from pins 2, 5, 12, 15, 16, and 19 are applied to a logic circuit of an inverter, a NOR gate, an AND gate, and a 74LS38 Quad NAND gate U16 to produce active low signals (MOTOR ENABLE A)*, (MOTOR ENABLE B)*, (DRIVE SELECT A)*, AND (DRIVE SELECT B)* at the output of U16.

The pin 5 output of U17 is also used as an active high ENABLE DRIVE C&D signal that is applied to the pin 3 input of 74LS04 inverter U12 and the pin 1 output enable of 74LS240 octal tristate buffer U16 in the drive to FDC read circuitry (described later). Inverter U12 complements this enable signal to produce (ENABLE DRIVE C&D)*. This signal is applied to another output enable pin (pin 19) of buffer U16.

Disk Drive Write Circuitry

Figure 2-102 is a block diagram of the drive write circuitry found on the disk drive adapter board. This circuitry generates the composite clock/data bit stream that becomes (WRITE DATA A&B)* and passes out over pin 22 of P2. It also generates a direction signal (DIR A&B)* out pin 18 of P2, a select head 0/1 signal (SELECT HEAD 1 A&B)* on P2 pin 32, and a step pulse out pin 20 of the same connector.

The combination of 75LS153 dual 4-line to 1-line multiplexer U10 and 74LS175 quad D flip-flop U11 generate a MFM serial clock/data stream that is output from U11 pin 2 to both the A&B and C&D drive circuitry. This signal is input to pins 1 and 2 of 74LS38 quad NAND gate U9 to produce an active low output signal (WRITE DATA A&B)* on pin 3. During the command phase of 765 operation, a set of nine bytes are sent to the FDC. This information includes the drive to select, the cylinder address, the head to select, the sector address, the sector size, the final sector number of the current track, the gap length between sectors (excluding the VCO synchronization field), and the effective sector size, so the FDC can write additional zeroes in case the write command completes before the end of a sector has been reached.

The execution phase begins and FDC U6 loads the head (if not already loaded), waits the specified 35 millisecond head load time, and begins reading sector ID fields. When a match is made between the requested sector address and the sector address read from the disk, the FDC reads data a byte at a time from the 8088 CPU and outputs the data to the magnetic head. The drive head writes this information into the data field area for that sector on the disk. When the data field is loaded, the 765 FDC computes a CRC value on the data and writes two CRC bytes

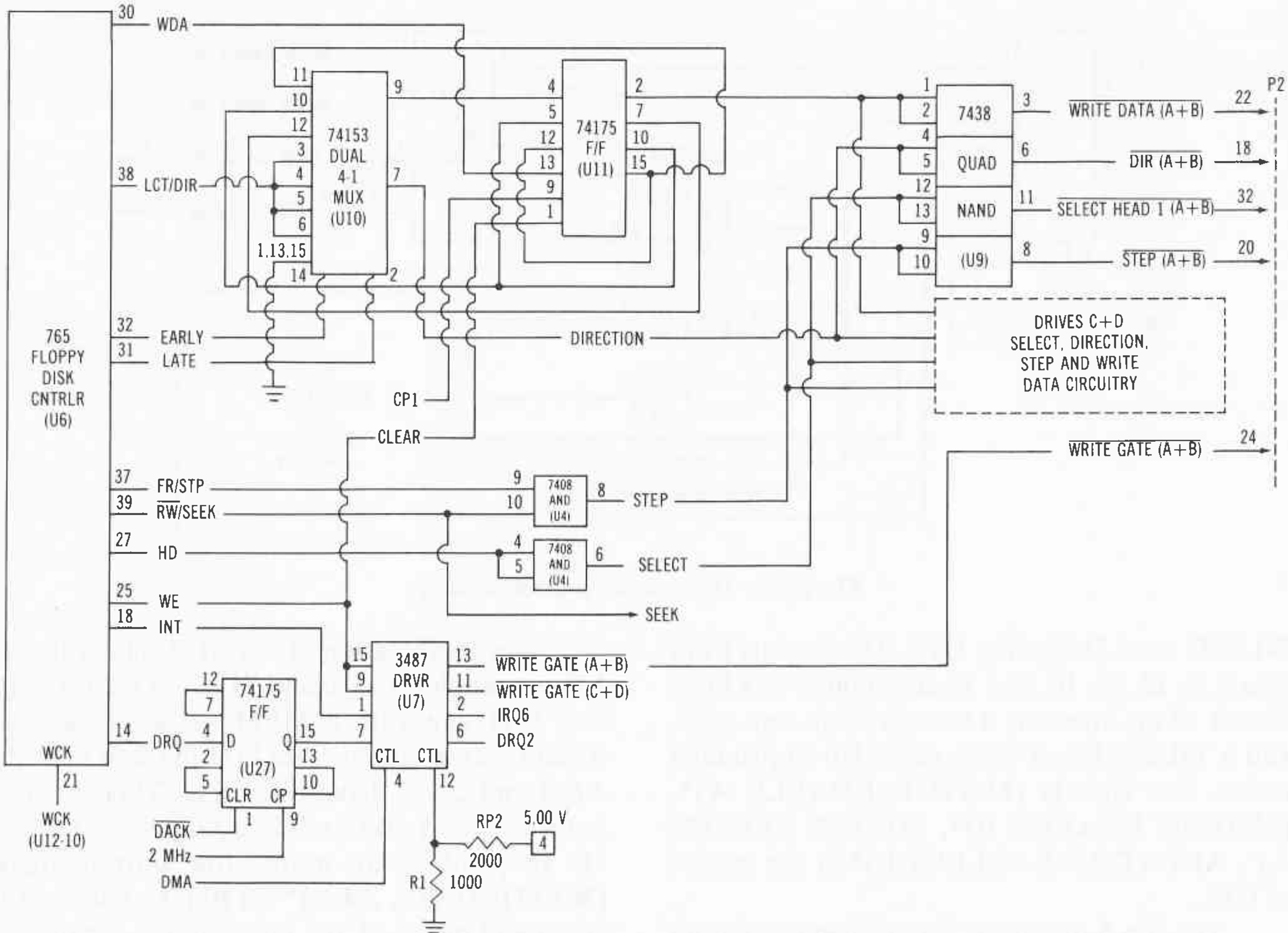


Fig. 2-102. Disk drive adapter write circuitry.

at the end of the data field. The FDC reads the ID field of the sector and compares the CRC bytes. If an error is detected, an error flag bit (bit 5) is set in the status register and the write data command terminates. Data transfers between the 8088 CPU and the FDC occur every 15 microseconds.

During the seek portion of the write cycle, FDC pin 38 outputs a logic value that determines the direction of head movement when a step pulse is received. A high causes the head to move (step) in; a low causes head movement to step out. When the write begins, pin 38 is used to lower the write current on the inner tracks of the disk.

FDC pins 31 and 32 are used by the pre-compensation circuitry of 74LS153 U10 and 74LS175 U11 to time-position clock and data pulses in the write data stream so that later playback will be able to properly separate out the clock and data from the signal stream. Preshift cancels predictable playback data shifts when MFM recorded data is retrieved from a floppy disk. A write clock signal (WCK) is input on pin 21 of 765 U6 (see also Fig. 2-97) to produce a 250 nanosecond clock signal that occurs at a 1 MHz rate. During a disk write operation, U6 specifies that a data bit should occur early, normal, or late relative to the write clock pulse. The early and late signals out pins 32 and 31 respectively are used to preshift the bit 250 nanoseconds before or after the write clock transition. If both output signals are low, no preshift occurs.

During the write mode, U6 pin 37 is also active. At the beginning of the write command, a fault reset pulse is issued to reset a fault flip-flop in the disk drive. When seek begins, pin 37 outputs step pulses that move the drive read write head to another cylinder track. During seek, pin 39 is high. The signals out pins 37 and 39 are ANDed by 74LS08 U4 to produce a predetermined number of step pulses during the seek cycle. These step pulses are passed through 74LS38 NAND U9 to produce active low (STEP A&B)* pulses.

FDC pin 27 is a signal that determines which head is to be selected. When U6 output pin 27 is high, read/write head 1 is selected. This signal is inverted in the 74LS38 NAND U9 to produce an active low select head 1 signal (SELECT HEAD 1 A&B)* out pin 11 of U9.

Pin 25 on U6 is a write enable output that is applied to a 3487 driver U7 to generate active low (WRITE GATE A&B)* and (WRITE GATE C&D)* signals out pins 13 and 11 respectively. These active low signals enable write current in the selected read/write head. Bringing these lines high disables the write current in the head.

Disk Drive Read Circuitry

Figure 2-103 shows the disk drive to adapter board input circuitry. Connector P2 brings composite read/clock data, write protect status, index information, and track 0 information from drives A and B into the 74LS240 octal inverter tristate buffer U18. Connector J1 handles the same signals for drives C and D.

Regardless of which drive inputs the data, four outputs from U18 provide composite read data, write protect, index, and track 0 information into the board circuitry. Buffer driver U18 pins 9 and 12 connect to provide READ DATA from any of four drives to the phase-lock loop clock and data recovery circuitry.

Output pins 5 and 16 combine to provide a logic signal representing the condition of write protection on the selected drive's disk to pin 34 of U6. If a write-protected disk is mounted in the selected drive, WRITE PROTECT goes high. This input signal sets bit 6 of status register 3 in U6.

U18 pins 3 and 18 combine to form an INDEX signal that is passed into pin 17 of U6. When active high, INDEX indicates that the head has just detected the beginning of a new disk track.

Finally, U18 pins 7 and 14 are combined to produce TRACK 0. During a seek mode operation, the detection of TRACK 0 causes this

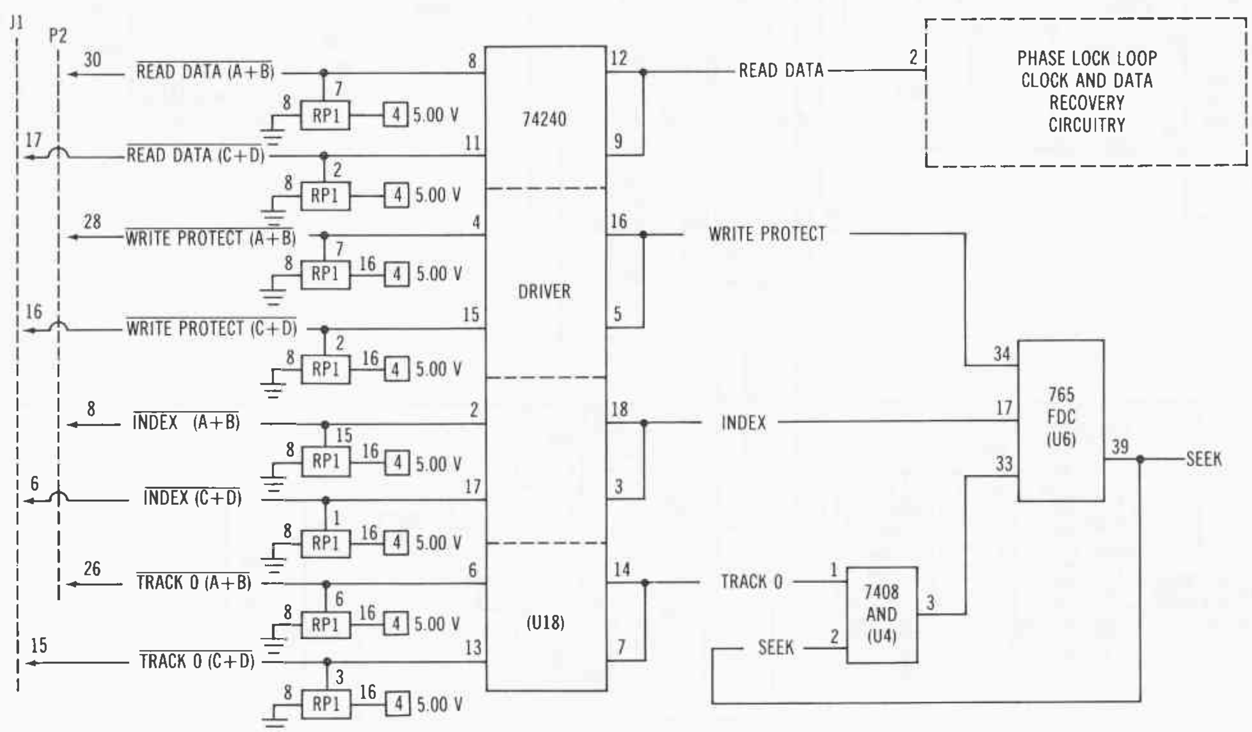


Fig. 2-103. Disk drive to adapter board input circuitry.

signal to go high. This sets bit 4 in FDC U6 status register 3.

Data Recovery Circuitry

During a read operation, the composite clock/data bit stream is buffered through U18 to a phase lock loop clock and data recovery circuitry, as shown in Fig. 2-103. Figure 2-104 expands the READ DATA handling circuitry to show the phase lock loop (PLL) pulse shaper, phase comparator, PLL oscillator, and FDC input read data and data window circuitry. The phase lock loop constantly analyzes the frequency of an input signal and locks another oscillator to the input frequency.

Composite clock/data bits are clocked into 74LS112 JK flip-flop U22 by a 16 MHz clock signal on pins 1 and 13. The FDC pin 24 output VCO SYNC is used to preset the READ DATA part of the dual flip-flop pair to the high state (output pin 6 held low) whenever VCO SYNC goes low. When VCO SYNC is low, it inhibits the voltage controlled oscillator in the phase-locked loop causing it to idle at its center frequency. After the read/write head has been loaded and the 35 nanosecond head load time has elapsed, VCO SYNC goes high enabling the pulse shaping and PLL circuitry. This circuitry is disabled in the gap between the ID field and the data field and in the gap after the data field before the next sector ID field to blank out erroneous data noise from head write current

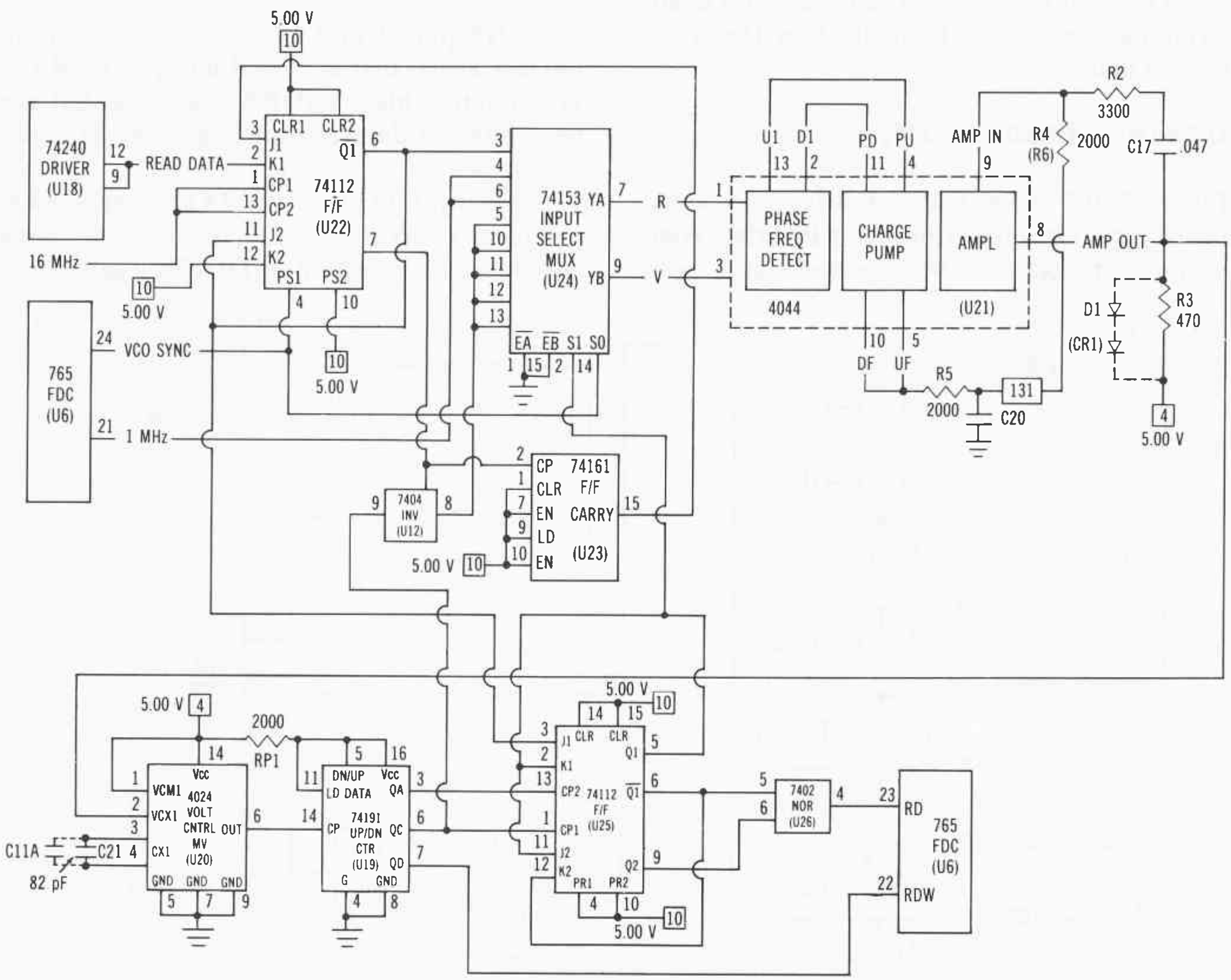


Fig. 2-104. Phase lock loop clock and data recovery circuitry.

turn on and off during gap time. VCO SYNC also serves as one of the two select signals for 74LS153 input select multiplexer U24.

A 4044 phase frequency detector (U21) is used as a phase-locked loop to compare the frequency of input data from the disk drive with the frequency of a 4024 voltage controlled multivibrator U20 functioning as a variable local oscillator. PLL U21 determines the clock and data bit positions in the READ DATA signal by sampling each bit. The phase relationship between a data bit and the PLL generated data window is constantly fed back to adjust the position of the data window causing U21 to track the READ DATA frequency changes and reproduce the same information that was sent from the system board to the drive electronics for storage.

In Fig. 2-104, 74LS112 U22 and 74LS153 serve to shape the data pulses before presenting to the input (pin 1) of PLL U21. At the output of U21 is an analog filter circuit that produces an error voltage from the PLL pump up (PU) and pump down (PD) signals derived from the phase difference between the PLL local oscillator U20 output and the READ DATA input.

The frequency difference AMP OUT of U21 is passed to pin 2 of 4024 voltage controlled oscillator (multivibrator) U20 to raise or lower its frequency so it better matches that of the READ DATA input signal. PLL U21 synchronizes the oscillator frequency of U20 to that of the READ DATA input during the reading of the "all zeroes" synchronization field off the track of the floppy disk. This field precedes the ID field and the data field.

Input select multiplexer U24 generates reference (R) and variable (V) inputs to 4044 phase frequency detector U21. The phase difference between READ DATA on the R (pin 1) input and the VCO U20 signal on the V (pin 3) input is compared in the phase frequency detect portion of U21. Loop "lock-on" occurs when both U1 (pin 13) and D1 (pin 2) remain high. This occurs when all the negative transitions of READ DATA R and V coincide. This circuit only responds to transitions and is independent of waveform duty cycle or amplitude variations. The outputs U1 and D1 are recycled back into pins 4 and 11 of the charge pump section as pump down (PD) or pump up (PU) error signals. If the READ DATA pulse occurs early compared with the VCO U20 variable pulse, the PU duration will be shorter than the PD duration. Likewise, if a READ DATA pulse occurs late, PU is held high longer than PD. The difference between the PU active time and the PD active time represents the difference between the READ DATA bit rate and the PLL clock rate. If PD is active longer than PU, the input bit rate is slower than the PLL clock.

The PU and PD signals into the charging pump produce the error voltages down frequency (DF) on pin 10 and up frequency (UF) on pin 5. These signals are applied to an analog RC filter network including an amplifier circuit inside U21. The DF and UF outputs from U21 are filtered and amplified to produce an error voltage out U21 pin 8. The relationship of PU and PD active times modifies the PLL oscillator time constant via the filter output to produce a VCO error voltage. This error voltage is passed to input pin 2 of the 4024 voltage controlled multivibrator oscillator U20 and causes the pin 6 output frequency to vary relative to the amount of error voltage.

Capacitor C21 (82 pF) is connected across pins 3 and 4 of U20 to control the operating frequency range of this oscillator. In some designs, a second 82 pF capacitor (U11A) is connected in parallel with C21.

The pin 6 output of U20 is connected to input pin 14 of 74LS191 up/down counter U19. Pin 5 (U*/D) is strapped high through a 2K resistor RP1 causing U19 to operate in the countdown mode. Output Qa (pin 3) functions as a pin 13 clock input for 74LS112 flip-flop U25. Pin 6 clocks another part of U25 to enable a composite READ DATA signal from output pin 6 of the 74LS112 input PLL pulse shaper flip-flop U22 in the upper left of Fig. 2-104 to clock out the Q1* (pin 6) and Q2 (pin 9) lines of U25 through 74LS02 NOR gate U26 into pin 23 of U6.

Pin 7 of U19 outputs a data window signal that is passed to pin 22 of 765 FDC U6. This signal (RDW) is used to isolate the data bits contained in the READ DATA composite input signal entering pin 23 of U6. After isolation of the data bits from the READ DATA bit stream, U6 assembles the data bits into 8-bit bytes for transfer to the 8088 CPU or system board memory.

SUMMARY

In this chapter, a detailed analysis was conducted into the operation of the IBM PC system board, keyboard, display, and disk drives. Knowledge to this level is required by technicians who desire to apply an intimate understanding of the PC electronics to achieve quick and correct troubleshooting of IBM PC computer problems.