..................................DX Single Chip Solution..
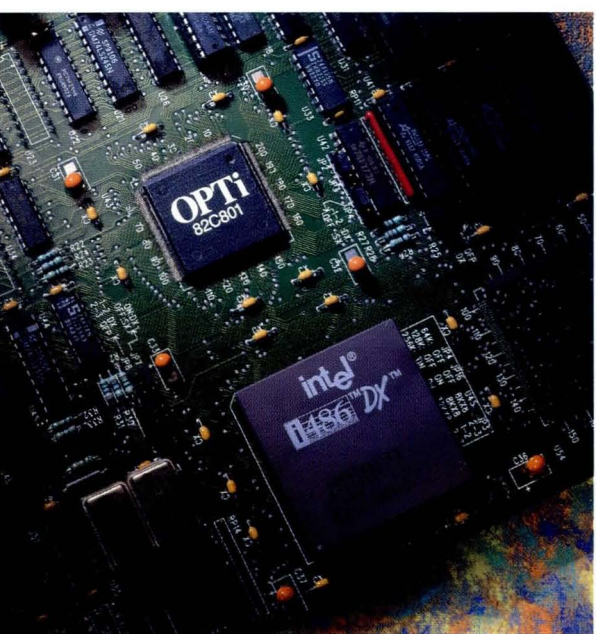
The 82C801 SCWB2 can be summarized in four words: integration, performance, features and reliability. The best value for the OEM/system house.

The SCWB2 is the result of an engineering team driven by the need to provide the fastest, most reliable solutions in the smallest, most cost effective package and having complete confidence in compatibility and reliability of the product. With a feature set that doesn't take a back seat to any solution in the market.

From the 50 MHz Write back Cache to complete local bus support, this chip is everything a system designer needs to provide his customer with state-of-the-art solutions for high performance PCs in the market today —and for some time to come.

The SCWB2 is designed for the OEM/system house who needs a single chip, local bus, lightning performance, design flexibility, 8 banks, quick-to-market, and cost effectiveness.

Features/Benefits

- Supports 486 SX/DX/DX2 and 487SX

- Single chip PC/AT solution: one 208 pin CMOS plastic flat package

- 1X and 2X clock source, supporting systems running from 16 to 50 MHz

- Write back direct mapped, bank interleave cache with size selections: 64, 128, 256, and 512K

- Supports 2-1-1-1, 3-1-1-1, 2-2-2-2, and 3-2-2-2 cache burst cycles

- Programmable cache and DRAM read/write cycles

- Built in TAG auto invalidation circuitry

- Programmable cache and DRAM read/write cycles

- Supports eight banks of 256K, 1M, and 4M DRAMs for configurations up to 64MB

- Supports 3-2-2-2 DRAM burst cycles

- Hidden refresh, slow refresh, and CAS before RAS refresh supported

- Comprehensive VESA VL and OPTi high performance local bus support

- Low power, high speed 0.8 μ CMOS technology

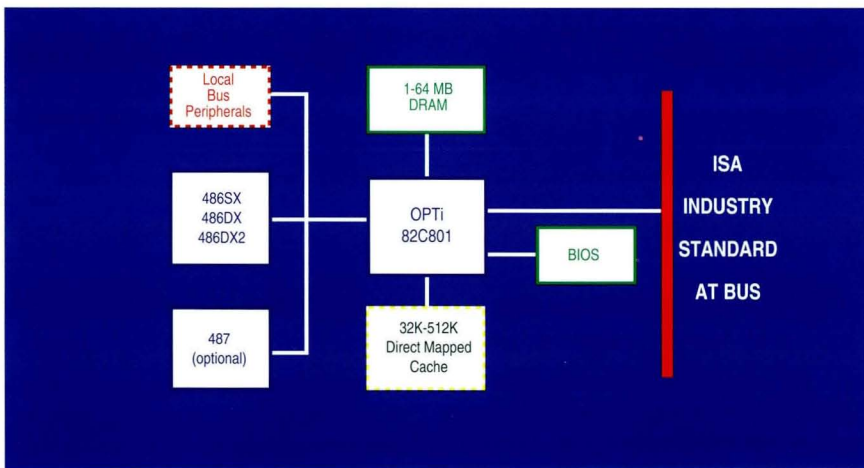- Integrated peripherals controller

OPTi

The 82C801 provides a total 486SX/486DX and 486DX2 solution for 1X/2X frequencies ranging from 16-50 MHz. The chip integrates a CPU state machine, a write back cache controller, a local DRAM controller, AT Bus State machine and the 82C206 integrated peripheral control logic into a single 208 pin PQFP package. The memory subsystem consists of up to 8 banks of 256K/1M/4M DRAM with hidden refresh. The cache controller supports write back cache sizes fro 32K to 512K. The chip has extensive, seamless local bus support.

The 82C801 provides the ideal solution for the customer who demands a quality, reliable, performance product which is the best in its field and is still cost effective.

Vital Statistics	82C801SCWB2
Frequency	16/20/25/33/40/50
PALS	0
Write back Cache size	32K - 512K
DRAM capacity	64M
DRAM speed	80 ns
Video/system BIOS shadow/cache	Yes
Synchronous AT bus clock	8.33/8.25/8.33
Full local bus support w/bus mastering	Yes
Landmark Speed 2.0 @66 MHz	223.05
Power meter v1.3 (MIPs) @66 MHz	29.304
Norton SI v6.0 (CI) @66 MHz	144.2
Byte v1.3 (CI) @66 MHz	17.29

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