Maestro-1™ *Audio*Drive® Solution Product Brief

DESCRIPTION

The Maestro-1™ PCI audio accelerator is part of ESS Technology's new generation of architecture that not only meets the demands of advanced PC audio applications, but also enables the integration of a complete multimedia subsystem on either a single adapter or motherboard. Maestro-1's functionality and interfaces are compliant with all major industry standards, including the Audio Subsystem Specification of PC97, Windows® 95 DirectSound™, Windows® Sound System®, AC'97 CODEC Interface, and PCI 2.1 Bus Specification.

The dual audio-engine Maestro-1 architecture consists of a 64-voice, pipelined, wavetable synthesizer and a proprietary programmable audio signal processor. Together they can simultaneously and efficiently handle multiple audio streams of different data types, high-quality music synthesis, and voice compression and decompression.

The Maestro-1 provides a high-performance PCI interface, while retaining full compatibility to existing DOS games through hardware emulation. The PCI bus is required for PC audio hardware to smoothly reproduce high-fidelity audio from Internet, MIDI, wave, and conferencing sources. The PCI bus achieves high-performance functionality by enabling the transfer of multiple, independent data streams. PCI improves data transfer efficiency by at least 20 times over the ISA bus. This is crucial for low-latency audio applications, such as Internet interactive audio.

Microsoft's DirectSound API is accelerated by digitally mixing up to 32 PCM streams of any frequency down to a single output stream of 48 kHz. Hardware acceleration frees the CPU to perform other tasks, such as video processing.

The Maestro-1's Wave Processor (WP) provides high-quality wavetable synthesis cost-effectively by storing the downloadable table samples in system memory. With ESS's WaveCache™ technology, the samples are retrieved using the PCI bus during playback. Each channel/stream has an independent pan, tremolo, vibrato and tone filter. The synthesizer also performs advanced audio effects such as reverb, chorus, flange, echo and 3-D spatial enhancement.

The Maestro-1 achieves complete DOS game compatibility through three major schemes: PC/PCI DMA, Distributed DMA, and Transparent DMA. Transparent DMA requires no sideband signals and is compatible with all Pentium® and Pentium Pro® chipsets with no constraints.

The Maestro-1 audio accelerator is available in an industry-standard 208-pin Plastic Quad Flat Package (PQFP).

FEATURES

- DOS game compatibility

System Interface

- 32-bit PCI Bus master, PCI 2.1 compliant
- < 0.5% PCI Bus Bandwidth for playing 16-bit/stereo/44.1KHz

Wavetable Synthesis

- 64-channel 50 MHz pipelined Wave Processor
- 1-8 MB Wavetable Memory downloadable in either system memory or local ROM/DRAM/FlashROM
- Programmable pan, tremolo, vibrato, rate conversion and tone filtering per channel
- Programmable effects including reverb, chorus, flange, echo

DirectSound Acceleration

- Digital mixing up to 32 data streams
- Hardware sample rate convert to 48 KHz from any sample rate

3-D Sound

- 3-D positional audio under DirectX™ 5.0
- Enhanced effects (reverb, chorus, echo, vibrato, etc.)
- AC-3 decode acceleration
  - External DSP for hardware AC-3 decode
  - Active Movie AC-3 filter acceleration option

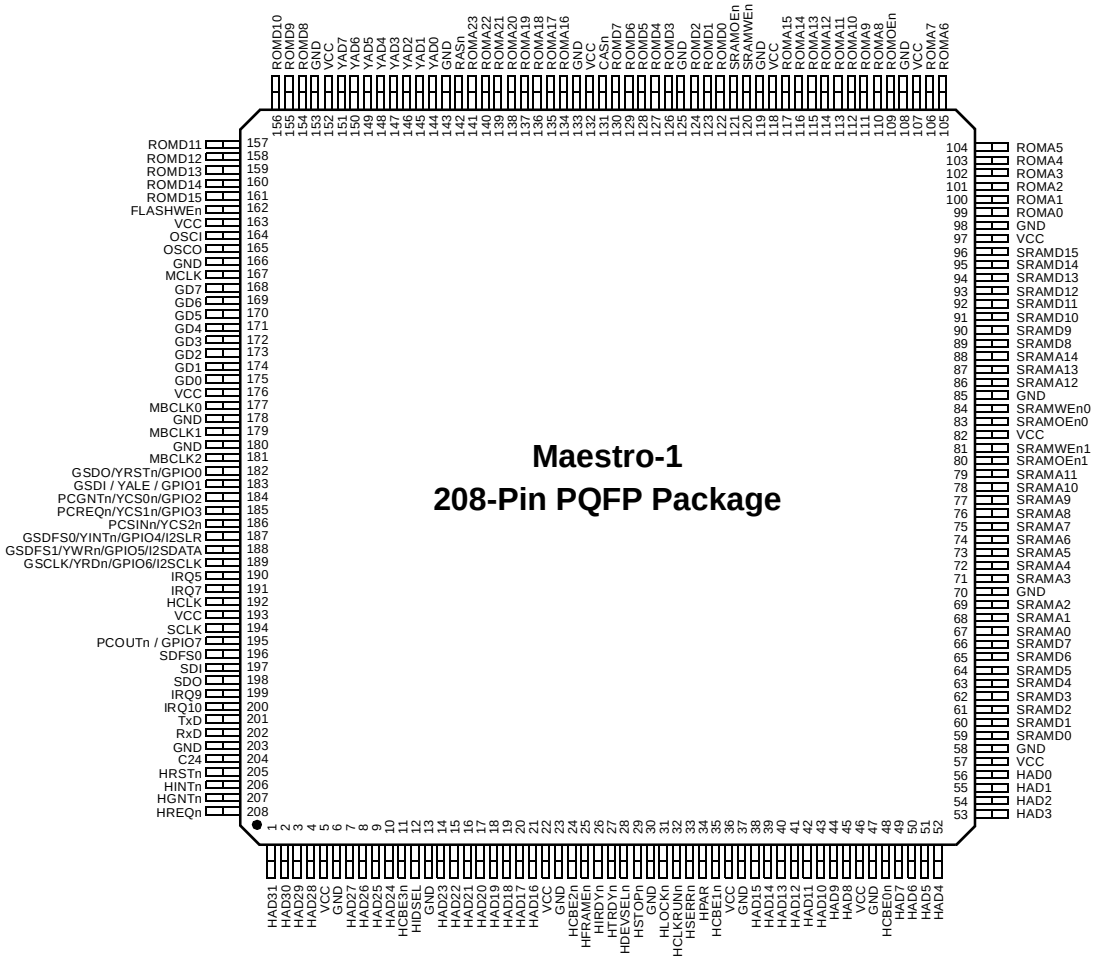
Software Compatibility

- Sound Blaster™ Pro
- Ad Lib™
- Windows Sound System
- Windows95
- DirectSound
- Microsoft® Active X™

Hardware Interfaces

- MPU-401 interface with FIFO
- High-performance game port
- General-Purpose I/O port
- 8-Bit peripheral interface
- I^2S digital audio Input
- Programmable audio CODEC interface:
  - PT-101 Audio CODEC
  - AC'97 CODEC Interface
  - Other 16-bit CODECs

PINOUT



PIN DESCRIPTION

O = Output - 24mA (PCI output)
Ob = Output - 4mA
Oc = Output - 24mA (PCI sustain output driver)
Od = Output - 24mA – Open drain
Oe = Output - 8mA
Of = Output - 16mA
Og = Output - 24mA
Oh = output with slew rate -12 mA
I = Input - TTL
Ib = Input - CMOS Schmitt trigger
Ic = Input - TTL Schmitt trigger
Id = Input - CMOS Schmitt trigger with internal pull-up
Ie = Input - TTL with internal pull-up
If = Input - TTL Schmitt trigger with internal pull-up

Name	Number	I/O	Definition
Host Interface PCI Bus Pins (51)			
HAD[31:0]	1:4,7:10,14:21,38:45,49:56	I/O	Multiplexed address and data lines
HCBE[3:0]n	11,24,35,48	I/O	Multiplexed command/byte enable
HRSTn	205	Ic	Reset
HPAR	34	I/O	Parity
HCLK	192	I	PCI bus clock
HFRAMEn	25	I/Oc	Cycle frame
HIRDYn	26	I/Oc	Initiator ready
HTRDYn	27	I/Oc	Target ready
HSTOPn	29	I/Oc	Stop transaction
HLOCKn	31	I/Oc	Lock
HIDSEL	12	I	ID select
HDEVSELn	28	I/Oc	Device select
HREQn	208	O	Request
HGNTn	207	I	Grant
HINTn	206	Od	Interrupt request
HSERRn	33	Od	System error
HCLKRUNn	32	I/Oc	Clock running

Name	Number	I/O	Definition
DRAM/SRAM/ROM Interfaces (58)			
YAD[7:0]	151:144	I/O	8-Bit peripheral data: YAD[7:0]
ROMA[23:0]	142:134,117:110,106:99	O	Either ROM or DRAM access. ROM = ROMA[23:0], or DRAM = Reserved[23:12], DRAMA[11:0]
RASn	142	O	DRAM/SRAM control.
CASn	131	O	DRAM/SRAM control.
SRAMWEn	120	O	DRAM/SRAM control.
ROMOEn	109	O	ROM output enable.
ROMD[15:0]/ RAMD[15:0]	161:154,130:126,124:122	I/O	Either ROM (ROMD[15:0]: ROM data), or DRAM/SRAM (RAMD[15:0]: RAM data) access.
SRAMOEn	121	O	SRAM control.
FLASHWEn	162	O	Flash ROM control.
MCLK	167	I	MPCI bus clock
MBCLK[2:0]	181,179,177	O	Buffered MPCI bus clocks
AC'97 CODEC Interface (4)			
SCLK	194	I/Oe	Serial clock. Default is output. Pull SRAMA[1] low to set to the input. Must be less than 24.576 Mhz. Tentatively, this frequency is set at 12.5 Mhz (should be within the range of 10-15 Mhz). Data is transmitted after a rising edge of SCLK, and sampled on a falling edge of SCLK.
SDFS0	196	Oe	Serial data frame sync. New data frames are marked by a LO to HIGH transition on SDFS0 one serial clock period before the frame begins. The transition back from HI to LO may occur at any time provided the HI and LO times of SDFS0 are at least one SCLK period in duration each.
SDI	197	I	Serial data in
SDO	198	Oe	Serial data out
IRQ Pins (4)			
IRQ5	190	Og	ISA IRQ5
IRQ7	191	Og	ISA IRQ7
IRQ9	199	Og	ISA IRQ9
IRQ10	200	Og	ISA IRQ10
MPU-401 Interface (2)			
TxD	201	Of	MIDI transmit data
RxD	202	Ic	MIDI receive data
Game Port Interface (8)			
GD[7:4]	168:171	Id	Game port data
GD[3:0]	172:175	Ib/Oh	Game port data
Clocks (3)			
OSCI	164	I	49.152 MHz crystal input
OSCO	165	Ob	49.152 MHz crystal output
C24	204	Ob	24.576 MHz clock output. For CODEC clock source.
SRAM Interface (35)			
SRAMA[14:11]	88:86,79	Ie/Oe	SRAM address. SRAMA[14:11] is at input state only during the Reset period. Inputs are latched during reset to define Bit [15:13] and Bit [8] of 16-bit Subsystem ID at the offset 2Eh of PCI Config. Space.
SRAMA[10]	78	Ie/Oe	SRAM address. SRAMA10 is at input state only during the Reset period. If NC (with internal pull-up): second CODEC is disabled. If 0: Enable second CODEC.
SRAMA[9:2]	77:71,69	Ie/Oe	SRAM address. SRAMA[9:2] is at input state only during the Reset period. Inputs are latched during reset to define Bit [7:0] of 16-bit Subsystem ID at the offset 2Eh of PCI Config. Space.
SRAMA[1]	68	Ie/Oe	SRAM address. SRAMA1 is at input state only during the Reset period. If NC (with internal pull-up): SCLK = Output. If 0: SCLK = Input.
SRAMA[0]	67	Ie/Oe	SRAM address. SRAMA0 is at input state only during the Reset period. Pull this pin low to enable local DRAM interface.
SRAMD[15:0]	96:89,66:59	I/Ob	SRAM data.
SRAMOEn[1:0]	80,83	Ie/Oe	SRAM output enable. SRAMOEn[1:0] is at input state only during the Reset period. Inputs are latched during reset to define Bit [9] and Bit [11] of 16-bit Subsystem ID at the offset 2Eh of PCI Config. Space.
SRAMWEn[1:0]	81,84	Ie/Oe	SRAM write enable. SRAMWEn[1:0] is at input state only during the Reset period. Inputs are latched during reset to define Bit [10] and Bit [12] of 16-bit Subsystem ID at the offset 2Eh of PCI Config. Space.
Second CODEC Interface (5)			
GSCLK *	189	Oe	Multipurpose pin. GSCLK, YRDn, GPIO6, or I2SCLK. When used as GSCLK = serial clock. Must be less than 24.576 Mhz. Data is transmitted after a rising edge of SCLK.
GSDFS0 *	187	Oe	Multipurpose pin. GSDFS0, YINTn, GPIO4, or I2SLR. When used as GSDFS0 = serial data frame sync 0. New data frames are marked by a LO to HIGH transition on SDFS0 one serial clock period before the frame begins. The transition back from HI to LO may occur at any time provided the HI and LO times of SDFS0 are at least one SCLK period in duration each.
GSDFS1 *	188	Oe	Multipurpose pin. GSDFS1, YWRn, GPIO5, or I2SDATA. When used as GSDFS1 = serial data frame sync 1. New data frames are marked by a LO to HIGH transition on SDFS1 one serial clock period before the frame begins. The transition back from HI to LO may occur at any time provided the HI and LO times of SDFS1 are at least one SCLK period in duration each.
GSDI *	183	Ie	Multipurpose pin. GSDI, YALE, or GPIO1. When used as GSDI = serial data in.
GSDO *	182	Oe	Multipurpose pin. GSDO, YRSTn, or GPIO0. When used as GSDO = serial data out.

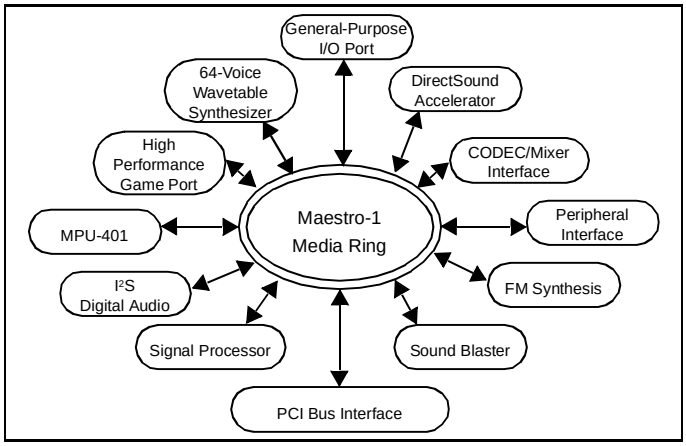
Name	Number	I/O	Definition
PC/PCI Interface (4)			
PCGNTn *	184	Ie	Multipurpose pin. PCGNTn, YCS0n, or GPIO2. When used as PCGNTn = PC/PCI grant.
PCREQn *	185	Oe	Multipurpose pin. PCREQn, YCS1n, or GPIO3. When used as PCREQn = PC/PCI request.
PCSINn *	186	Ie/Oe	Multipurpose pin. PCSINn, or YCS2n. When used as PCSINn = PC/PCI serial IRQ input. COMPAQ: serial IRQ input/output
PCOUTn *	195	Oe	Multipurpose pin. PCOUTn, or GPIO7. When used as PCOUTn = PC/PCI serial IRQ output.
Peripheral/ISDN Interface (8)			
YRSTn *	182	Oe	Multipurpose pin. GSDO, YRSTn, or GPIO0. When used as YRSTn = reset. A "low" on this pin forces both LAPD and LAPB devices into reset state. The minimum pulse length is 1.8 µs.
YALE *	183	Oe	Multipurpose pin. GSDI, YALE, or GPIO1. When used as YALE = address latch enable. A "high" on this pin indicates an address valid on the multiplexed address/data bus (AD7-0).
YCS0n *	184	Oe	Multipurpose pin. PCGNTn, YCS0n, or GPIO2. When used as YCS0n = chip select 0. A "low" on this line selects LAPD device for read/write operation.
YCS1n *	185	Oe	Multipurpose pin. PCREQn, YCS1n, or GPIO3. When used as YCS1n = chip select 1. A "low" on this line selects LAPB device for read/write operation.
YCS2n *	186	Oe	Multipurpose pin. PCSINn, or YCS2n. When used as YCS2n = chip select 2. A "low" on this line selects U interface device for read/write operation.
YINTn *	187	Ie	Multipurpose pin. GSDFS0, YINTn, GPIO4, or I2SLR. When used as YINTn = interrupt. This pin is shared by both LAPD and LAPB devices.
YWRn *	188	Oe	Multipurpose pin. GSDFS1, YWRn, GPIO5, or I2SDATA. When used as YWRn = write. Active-low. This signal indicates a write operation. It is common to both LAPD and LAPB devices
YRDn *	189	Oe	Multipurpose pin. GSCLK, YRDn, GPIO6, or I2SCLK. When used as YRDn = read. Active-low. This signal indicates a read operation. It is common to both LAPD and LAPB devices.
General-Purpose I/O Pins (7)			
GPIO0 *	182	Ie/Oe	Multipurpose pin. GSDO, YRSTn, or GPIO0. When used as GPIO0 = GPIO0.
GPIO1 *	183	Ie/Oe	Multipurpose pin. GSDI, YALE, or GPIO1. When used as GPIO1 = GPIO1.
GPIO2 *	184	Ie/Oe	Multipurpose pin. PCGNTn, YCS0n, or GPIO2. When used as GPIO2 = GPIO2.
GPIO3 *	185	Ie/Oe	Multipurpose pin. PCREQn, YCS1n, or GPIO3. When used as GPIO3 = GPIO3.
GPIO4 *	187	Ie/Oe	Multipurpose pin. GSDFS0, YINTn, GPIO4, or I2SLR. When used as GPIO4 = GPIO4.
GPIO5 *	188	Ie/Oe	Multipurpose pin. GSDFS1, YWRn, GPIO5, or I2SDATA. When used as GPIO5 = GPIO5.
GPIO6 *	189	Ie/Oe	Multipurpose pin. GSCLK, YRDn, GPIO6, or I2SCLK. When used as GPIO6 = GPIO6.
GPIO7 *	195	Ie/Oe	Multipurpose pin. PCOUTn, or GPIO7. When used as GPIO7 = GPIO7.
I²S Interface (3)			
I2SLR *	187	Ie	Multipurpose pin. GSDFS0, YINTn, GPIO4, or I2SLR. When used as I2SLR = I²S left right latch.
I2SDATA *	188	Ie	Multipurpose pin. GSDFS1, YWRn, GPIO5, or I2SDATA. When used as I2SDATA = I²S data input pin.
I2SCLK *	189	Ie	Multipurpose pin. GSCLK, YRDn, GPIO6, or I2SCLK. When used as I2SCLK = I²S clock.
Power Pins (34)			
VCC		Pwr	+5 volts
GND		Pwr	Ground

* These pins share more than one function.

DIGITAL CHARACTERISTICS

Symbol	Parameters	Min	Max	Unit
VIH1	Input high voltage: all digital inputs except Xtal[2:1]	2.4	Vdd+0.3	V
VIH2	Input high voltage: Xtal[2:1]	2.4	Vdd+0.3	V
VIL	Input low voltage: all digital inputs	-0.3	0.8	V
VOH	Output high voltage	2.4		V
VOL	Output low voltage		0.4	V
	Input leakage current	-10	10	µA
	Output leakage current	-10	10	µA

BLOCK DIAGRAM



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