Winbond Electronics Corp.

16K × 8 HIGH-SPEED CMOS STATIC RAM

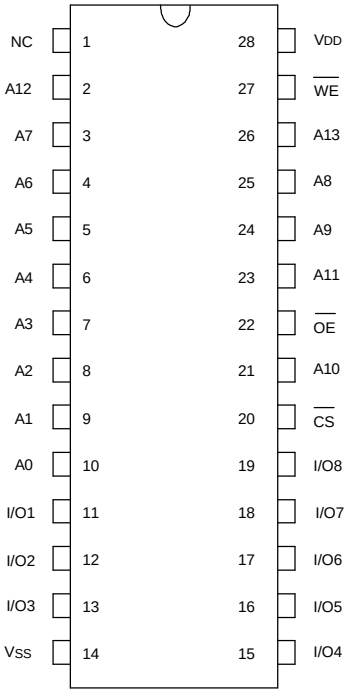
GENERAL DESCRIPTION

The W24129A is a high-speed, low-power CMOS static RAM organized as 16384 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

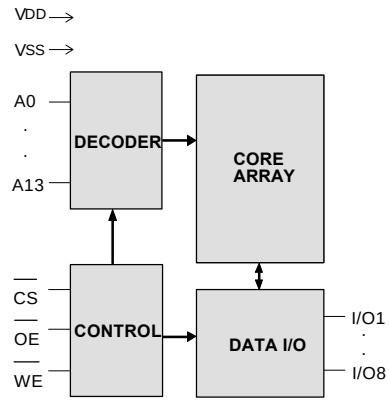
FEATURES

- High-speed access time: 12/15 nS (max.)
- Low-power consumption:
  - Active: 400 mW (typ.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Available packages: 28-pin 300 mil SOJ and skinny DIP

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A13	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VDD	Power Supply
VSS	Ground

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Input/Output to V_{SS} Potential	-0.5 to V_{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O1-I/O8	V_{DD} CURRENT
H	X	X	Not Selected	High Z	I_{SB},I_{SB1}
L	H	H	Output Disable	High Z	I_{DD}
L	L	H	Read	Data Out	I_{DD}
L	X	L	Write	Data In	I_{DD}

OPERATING CHARACTERISTICS

(V_{DD} = 5V ±5%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}	-		-0.5	-	+0.8	V
Input High Voltage	V_{IH}	-		+2.2	-	V_{DD} +0.5	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}		-10	-	+10	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SS} to V_{DD}, $\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		-10	-	+10	µA
Output Low Voltage	V_{OL}	I_{OL} = +8.0 mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0 mA		2.4	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CS}$ = V_{IL}, I/O = 0 mA Cycle = MIN	12	-	-	160	mA
			15	-	-	150	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH} Cycle = MIN, Duty = 100%		-	-	30	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{DD} -0.2V		-	-	5	mA

Note: Typical characteristics are at V_{DD} = 5V, T_A = 25° C.

CAPACITANCE

(V_{DD} = 5V, T_A = 25° C, f = 1 MHz)

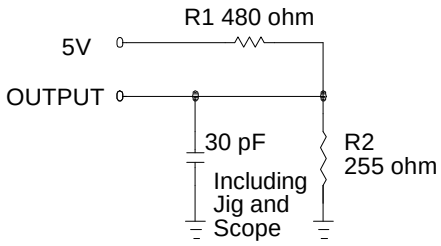
PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	8	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	10	pF

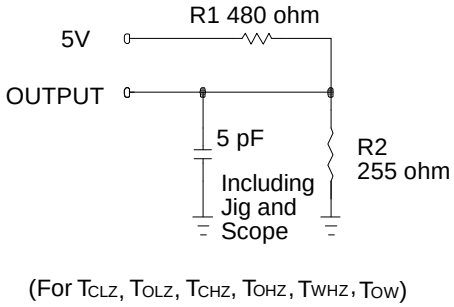
Note: These parameters are sampled but not 100% tested.

AC TEST CONDITIONS

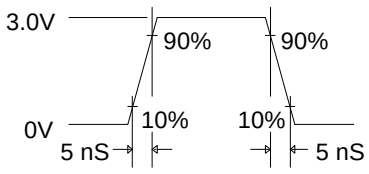
PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 30 pF, I_{OH}/I_{OL} = -4 mA/8 mA

AC TEST LOADS AND WAVEFORM





(For T_{CLZ}, T_{OLZ}, T_{CHZ}, T_{OHZ}, T_{WHZ}, T_{OW})



AC CHARACTERISTICS

(V_{DD} = 5V ±5%, V_{SS} = 0V, T_A = 0 to 70° C)

Read Cycle

PARAMETER	SYM.	W24129A-12		W24129A-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	12	-	15	-	nS
Address Access Time	T_{AA}	-	12	-	15	nS
Chip Select Access Time	T_{ACS}	-	12	-	15	nS
Output Enable to Output Valid	T_{AOE}	-	6	-	7	nS
Chip Selection to Output in Low Z	T_{CLZ}*	3	-	3	-	nS
Output Enable to Output in Low Z	T_{OLZ}*	0	-	0	-	nS
Chip Deselection to Output in High Z	T_{CHZ}*	-	6	-	7	nS
Output Disable to Output in High Z	T_{OHZ}*	-	6	-	7	nS
Output Hold from Address Change	T_{OH}	3	-	3	-	nS

* These parameters are sampled but not 100% tested.

Write Cycle

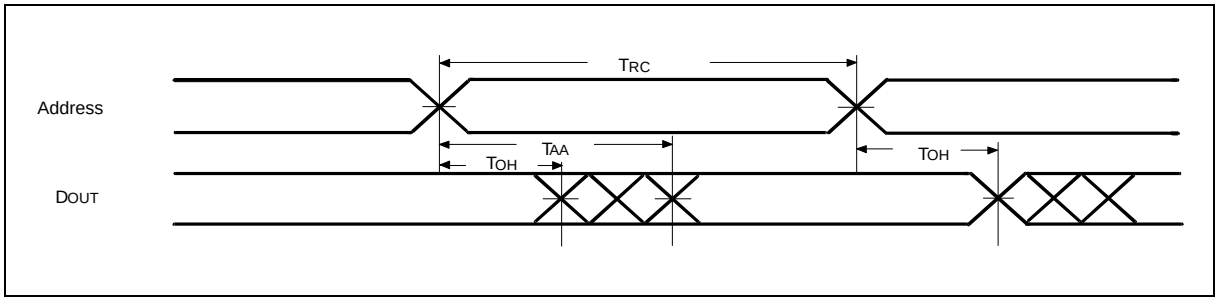
PARAMETER		SYM.	W24129A-12		W24129A-15		UNIT
			MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		T_{WC}	12	-	15	-	nS
Chip Selection to End of Write		T_{CW}	10	-	13	-	nS
Address Valid to End of Write		T_{AW}	10	-	13	-	nS
Address Setup Time		T_{AS}	0	-	0	-	nS
Write Pulse Width		T_{WP}	10	-	10	-	nS
Write Recovery Time	$\overline{CS}$, $\overline{WE}$	T_{WR}	0	-	0	-	nS
Data Valid to End of Write		T_{DW}	7	-	9	-	nS
Data Hold from End of Write		T_{DH}	0	-	0	-	nS
Write to Output in High Z		T_{WHZ}*	-	7	-	8	nS
Output Disable to Output in High Z		T_{OHZ}*	-	7	-	8	nS
Output Active from End of Write		T_{OW}	0	-	0	-	nS

* These parameters are sampled but not 100% tested.

TIMING WAVEFORMS

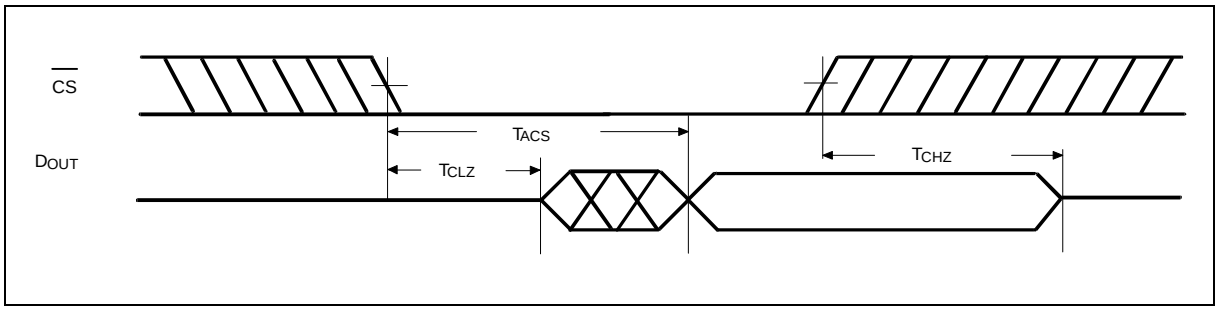
Read Cycle 1

(Address Controlled)



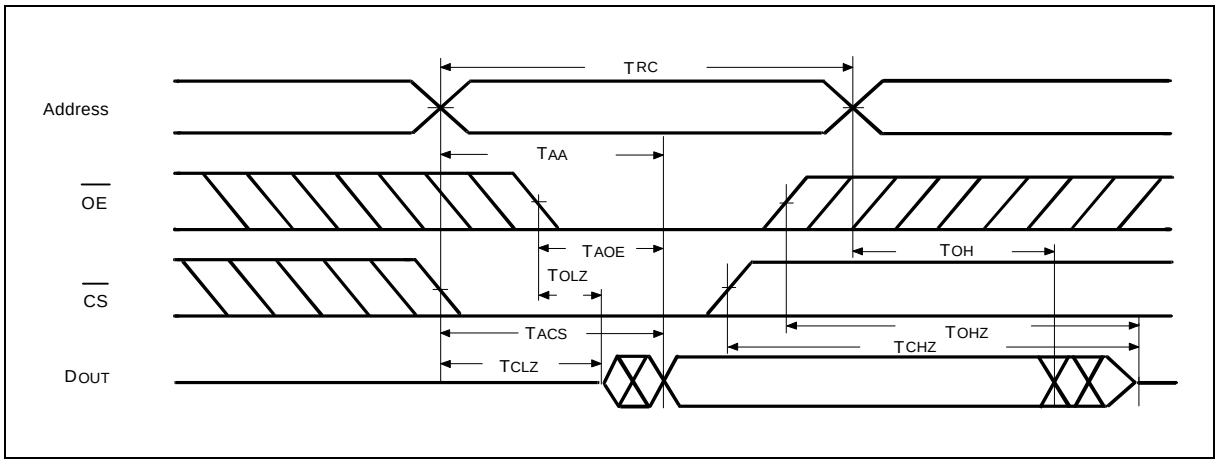
Read Cycle 2

(Chip Select Controlled)



Read Cycle 3

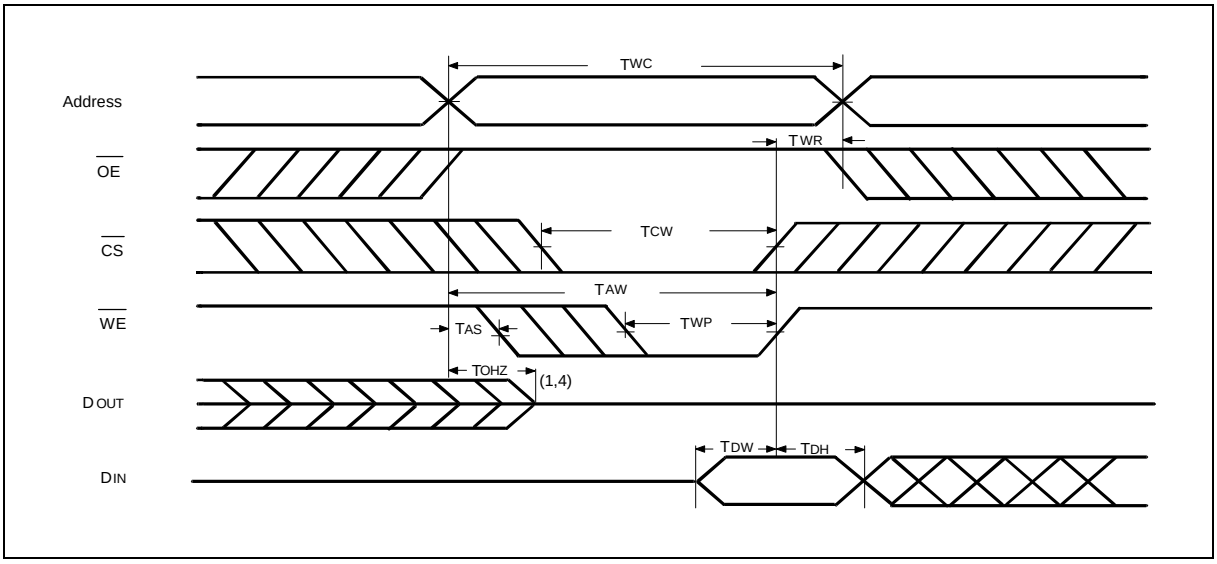
(Output Enable Controlled)



Timing Waveforms, continued

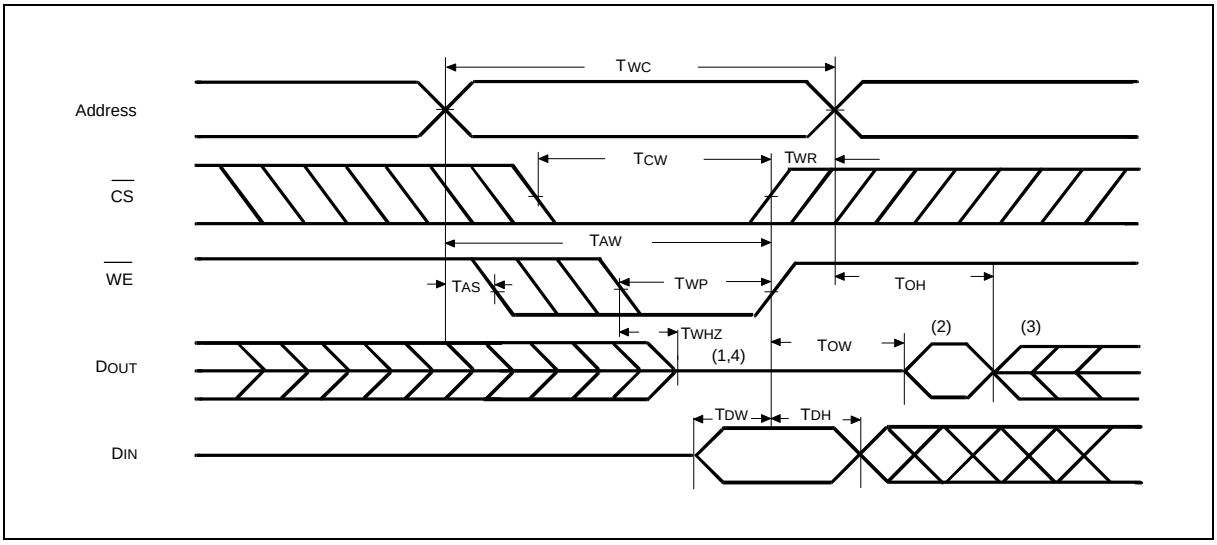
Write Cycle 1

($\overline{OE}$ Clock)



Write Cycle 2

($\overline{OE}$ = VIL Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ±500 mV from steady state with CL = 5 pF. This parameter is guaranteed but not 100% tested.

ORDERING INFORMATION

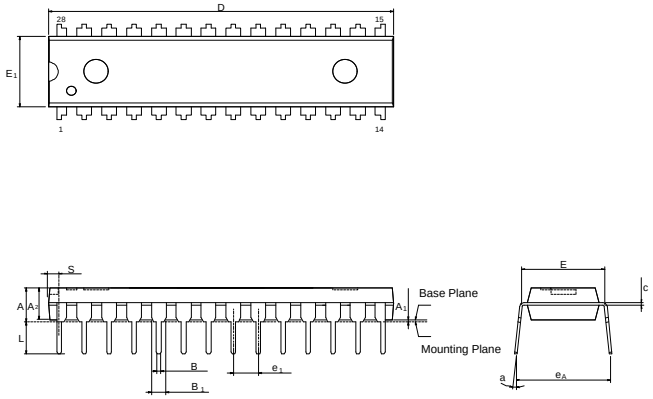
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24129AK-12	12	160	5	300 mil skinny DIP
W24129AK-15	15	150	5	300 mil skinny DIP
W24129AJ-12	12	160	5	300 mil SOJ
W24129AJ-15	15	150	5	300 mil SOJ

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

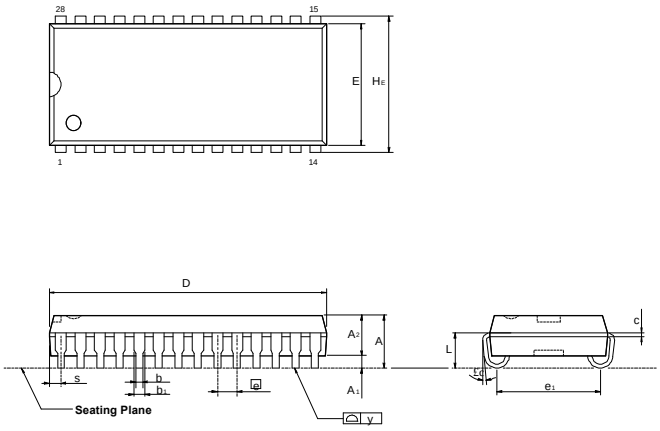
28-pin P-DIP Skinny



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.175	—	—	4.45
A_1	0.010	—	—	0.25	—	—
A_2	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.388	1.400	—	35.26	35.56
E	0.300	0.310	0.320	7.62	7.87	8.13
E_1	0.283	0.288	0.293	7.19	7.32	7.44
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0°	—	15°	0°	—	15°
e_A	0.330	0.350	0.370	8.38	8.89	9.40
S	—	—	0.055	—	—	1.40

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

28-pin Small Outline J Band



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A_1	0.027	—	—	0.69	—	—
A_2	0.095	0.100	0.105	2.41	2.54	2.67
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	0.710	0.730	—	18.03	18.54
E	0.295	0.300	0.305	7.49	7.62	7.75
e	0.044	0.050	0.056	1.12	1.27	1.42
e_1	0.245	0.265	0.285	6.22	6.73	7.24
H_E	0.327	0.337	0.347	8.31	8.56	8.81
L	0.077	0.087	0.097	1.96	2.21	2.46
S	—	—	0.045	—	—	1.14
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and are determined at the mold parting line.
4. Controlling dimension: Inches.
5. General appearance spec. should be based on final visual inspection spec.

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