Cat. No. 25-1516

Tandy 1000 SL

Technical Reference Manual

TANDY®

The Technical Reference Manual for the Tandy 1000 SL describes the computer hardware components and their relationships to one another, as well as the BIOS (Basic Input Output Services).

The information in this manual is intended for hardware and software designers, engineers, programmers, and anyone who requires an understanding of the design and operation of the computer.

Timing diagrams for devices used in the system architecture, Schematics, specifications, switch settings and jumpers, and a theory of operation are provided for the following hardware sections:

Main Logic Board
Devices
Power Supplies
Keyboards
Disk Drives

The Software section contains the following:

A Quick Reference list of software interrupts
(for all device, I/O, and system status services)
Keyboard ASCII and scan codes
An MS-DOS memory map

The information in this manual is a supplement to and based on a working knowledge of the following literature:

The 1000 SL Installation and Operation Guide (Packaged with th computer)

The Intel iAPX 86/88/186/188 User's Manual-Programmers Reference. Intel order number 210911-003

The Intel iAPX 86/88/186/188 User's Manual-Hardware Reference. Intel order number 210912-001

AP-67 8086 System Design. Intel order number 230792-001

This Intel literature may be ordered directly from Intel at the followin number: 1-800-549-4725

Tandy 1000SL
Page Insertion Guide

Important Customer Note:

A gray stripe has been printed along the right edge of the title page of each of the sections to facilitate your finding the beginning of the section.

Also, a tabbed divider for each section has been provided for insertion at this point.

- Exploded view: Insert at the end of the Assembly/Disassembly section

- Foldout schematic pages: Insert at the end of the Main Logic Board section

Schematics	C8000302 - Rev B Sheets 1 of 7 thru 7 of 7
Schematic	C8000308 - Rev B Sheet 1 of 1

- Foldout PCB art: Insert after the Main Logic Board schematics

Silkscreen Layer 1 Component Side Layer 2 GND Plane Layer 3 + 5V Plane Layer 4 Solder Side	1700378 - Rev B

- Foldout schematic page: Insert at the end of the 67 Watt Single Input Power Supply section

Schematic	Model No. 8790085

- Foldout schematic page: Insert at the end of the 67 Watt Dual Input Power Supply section

Schematic	Model No. 8790084

- Foldout keyboard art pages: Insert after the Fujitsu Keyboard information in the Keyboard section

Keyboard Unit Assembly	N860-4703-U001
Block Diagram	4700
Circuit Specification	N86C-4700-0001
Circuit Specification	N86C-4700-0101

Foldout schematic page: Insert after the Fujitsu Custom IC Pin Signal sheet 2 of 3 in the Keyboard section

Schematic	Fujitsu Custom IC Pin Signals & Function	Sheet 3 of 3

Foldout TEAC schematic pages: Insert after the Section 3 - Maintenance portion of the Disk Drive section

PCBA Front Opt #N Total Diagram	FD-55R FD-55BR/FR/GR Sheets 1 of 3 thru 3 of 3
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Introduction

Introduction

General Description

The Tandy® 1000 SL is modular in design to allow maximum flexibility in system configuration. The computer consists of a main unit, and a detachable keyboard with coiled cable. The main unit is supplied with one internal 5¼-inch 360K floppy disk drive. The standard types of monitors used with the Tandy 1000 SL are the monochrome and the color RGB monitor. Since these units are modular, you can place them on top of the main unit or at any convenient location.

The Tandy 1000 SL comes standard with 384K of system RAM. An optional 256K RAM can be added on the system board to expand the memory to a full 640K bytes, the maximum RAM allowed by the system memory map.

Other features include a parallel printer port, a serial port, two built-in joystick interfaces, a speaker for audio output, a microphone jack, and a headphone jack with volume control.

Specifications Summary

- 8086 CPU running at 8 MHz, 0 wait state, switchable to 4 MHz
- Socket for 8087 numerical coprocessor
- 384K bytes DRAM upgradeable to 640K bytes (16-bit data bus)
- 4 Mbit BIOS ROM with MS-DOS® and Deskmate® (16-bit data bus)
- Tandy 1000 SL video controller that supports:
  - 128K bytes DRAM (used as system and video memory)
  - alphanumeric mode
  - graphics modes including:
    - 160 X 200 16-color
    - 320 X 200 4-color
    - 320 X 200 16-color
    - 640 X 200 2-color
    - 640 X 200 4-color
- 8237-5 DMA controller that supports:
  - 3 DMA channels
  - 8-bit transfers
  - 4 MHz clock speed
- 8259A interrupt controller for 8 interrupts
- 8254 interval timer that supports:
  - system interrupt timing
  - sound timing
- Custom keyboard interface controller
- 101-key Enhanced keyboard
- Custom parallel printer port
- Serial port (RS-232-C)
- Audio interface circuit that supports:
  - internal 8-OHM speaker
  - headphone jack with user accessible volume control
  - microphone input
- Joystick interface for two joysticks
- Custom floppy disk controller circuit that supports:
  - 5¼-inch 360K floppy disk drives
  - 3½-inch 720K floppy disk drives
- One 5¼-inch 360K floppy disk drive
- Five 10" 8-bit expansion slots
- Reset button and support logic
- 67-Watt power supply

Optional Features

- Real-time clock w/battery
- 8087 numerical math coprocessor
- 256K DRAM upgrade (16-bit data bus memory)
- 5¼-inch 360K floppy disk drive
- 3½-inch 720K floppy disk drive
- Add-in hard disk drives
- Hard disk card (20/40 meg)
- Display adapter boards that support mono, EGA, or other special video modes
- 300, 1200, or 2400 baud modem boards

Assembly/Disassembly

System Assembly/Disassembly (Including Exploded Views)

The following instructions explain how the major subassemblies are removed from the Tandy 1000 SL. Re-assembly of major sub-assemblies is accomplished by reversing the order of the removal procedures.

1. Top Cover Removal

a. Remove the (2) screws from the side of the computer at the rear.

b. Slide the cover forward enough to clear the power button, volume knob, and disk drive eject button and off.

2. 5¼-inch Floppy Drive Removal

a. Remove the top cover.

b. Unplug all cables from the disk drive.

c. Remove the (3) screws attaching the drive to the drive mounting tower.

d. Slide the drive forward out of the drive mounting tower.

3. Power Supply Removal

a. Remove the top cover.

b. Remove the rear panel by slightly bending the hooks on each side near the bottom and rotating enough to clear the sheet metal and then lift up.

c. Remove all cables from the main logic board and disk drives.

d. Remove the arm attached to the power supply switch.

e. Remove the (2) screws from the rear of the computer and (1) screw from the side that secure the power supply to the rear of the machine.

f. Slide the power supply up and out.

4. Main Logic Board Removal

a. Remove the top cover.

b. Unplug all cables and remove all the adapter boards from the system.

c. Remove the power supply.

d. Remove the back of the chassis by removing (2) screws at the rear of the computer and pulling the back of the chassis to the rear and down to clear the (3) hooks in the bottom of the chassis.

e. Remove spring clip from volume control knob post.

f. Remove the (11) screws holding the main logic board in place.

g. Remove the main logic board by carefully pulling straight back from under the drive support and out of the chassis.

NOTE: WHEN REPLACING THE MAIN LOGIC BOARD, BE SURE THAT THE VOLUME CONTROL KNOB POST SLIDES INTO THE VOLUME CONTROL POT CORRECTLY.

MECHANICAL BILL OF MATERIAL - TANDY 1000 SL

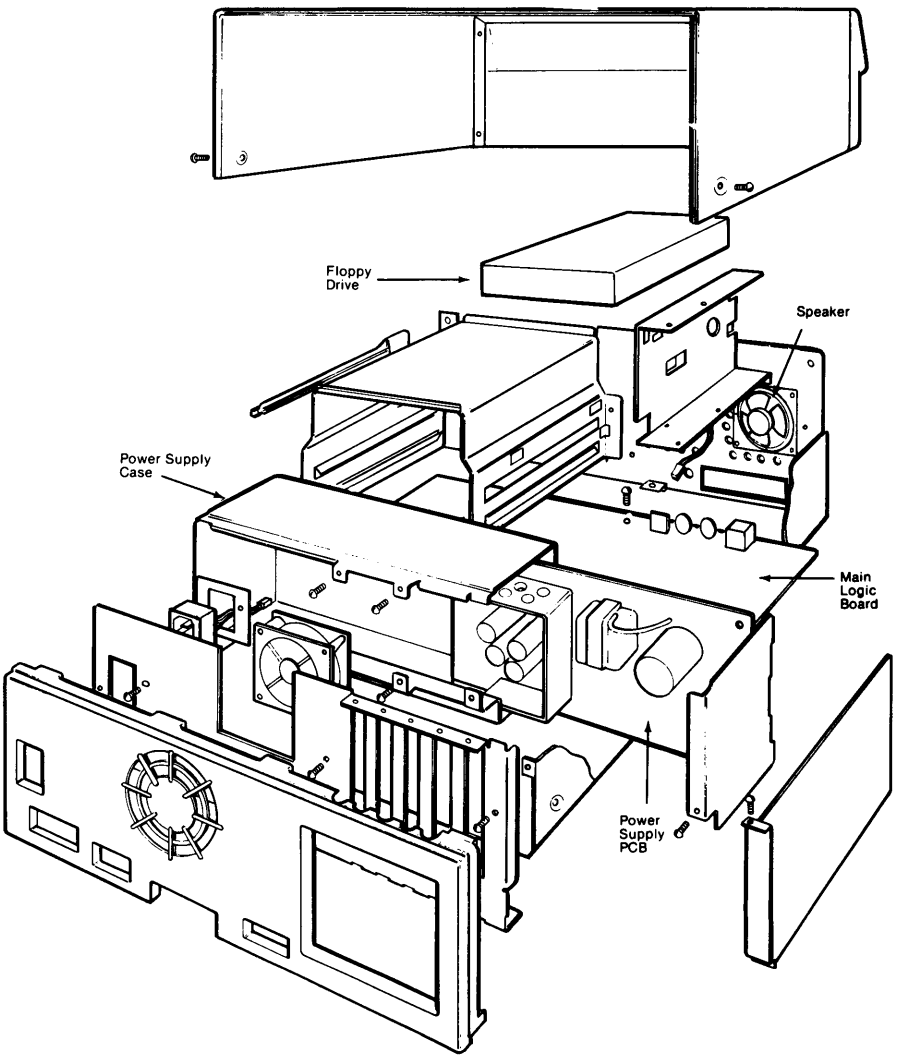
TANDY 1000 SL FINAL ASSEMBLY

QTY.	DESCRIPTION	PART NUMBER
1	CHASSIS - WELDMENT	8729709
5	PANEL - OPTION SLOT	8729562
5	SCREW - #4-40 X 3/16	8569333
4	FOOT	8590179
4	RIVET - #1661-0512	8565014
1	PC BOARD - MAIN LOGIC	8859024
1	PC BOARD - FRONT & BACK (BREAK APART BD)	8859110
11	SCREW - #6-32 X 1/4	8569326
4	JACKNUT - #4-40 X 3/16	8569341
4	SHIELDING STRIP	8729658
1	KNOB - VOLUME CONTROL	8719624
1	CLIP - HAIRPIN	8559080
1	CHASSIS - POWER SUPPLY	8729690
3	SCREW - #6-32 X 5/16	8569339
1	POWER SUPPLY - 67 WATT	8790084
	INT'L	
	DOM.	8790085
	DOM.	8790091
4	SCREW - #6-32 X 5/16	8569339
1	DC HARNESS	8709857
1	SWITCH - POWER	8489111
1	SWITCH - POWER	8489112
	INT'L	
2	SCREW - M3 X 5 PPH	8569293
1	BUTTON - POWER	8719625
1	ACTUATOR - POWER SWITCH	8719620
1	RECEPTACLE - AC	8519246
1	HARNESS - AC	8709868
1	HARNESS - AC INT'L	8709873
2	CAPACITOR - 1000 PFD, 400V	8352106
1	TORROID - CORE FAIRRITE	8419030
2	NUT - KEPS, #6-32	8579004
1	FAN - 80MM; 12 VDC	8790424
4	SCREW - #10 TAPIT THREAD	8569301
1	ENDPLATE - POWER SUPPLY	8729691
2	SCREW - #6-32 X 5/16	8569339
1	CHASSIS - REAR	8729693
1	DISK DRIVE - 5 1/4" TEAC	8790136
3	SCREW - M3 X 5 PPH	8569293
1	CABLE - SIGNAL	8709856
2	RAIL - 5 1/4" DRIVE	8719603
2	CLIP - GROUNDING, DRIVE	8529064
2	SCREW - #6 - 32 X 1/4 PHILLIPS PAN HD	8569098
1	BRACKET - HARD CARD	8729704
1	SCREW - #6-32 X 5/16	8569339
1	SPEAKER W/CABLE	8490013
4	SCREW - #6-32 X 5/16	8569339

MECHANICAL BILL OF MATERIAL - TANDY 1000 SL

TANDY 1000 SL FINAL ASSEMBLY

QTY.	DESCRIPTION	PART NUMBER
1	PANEL - REAR	8719602
1	BEZEL - FRONT	8719598
2	PIN-GUIDE	8739038
5	SCREW - #6 X 3/8	8569294
1	CASE - TOP	8729686
4	SCREW - #10-24 UNC X 3/8" PHILLIPS OVAL HEAD MACHINE SCREW	8569354
1	BUTTON - RESET, FRONT	8719440
1	BUTTON - RESET, REAR	8719441
1	SPRING - RESET BUTTON	8739018
1	LABEL - SERIAL UL/FCC,	87891644
1	CORD - POWER 18/3 60/C	8709057
1	LABEL - SERIAL, CSA	87891645
1	NAMEPLATE	8719618
1	LABEL - SERIAL, INT'L	87891646
1	LABEL - SERVICE ADVISEMENT (6 LANG)	87891571
1	LABEL - CAUTION (6 LANG)	87891572
1	LABEL - EARTH GROUND INT'L	87891253
1	LABEL - VIDEO, MONOCHROME COMMAND	87891648
1	KEYBOARD ASSEMBLY	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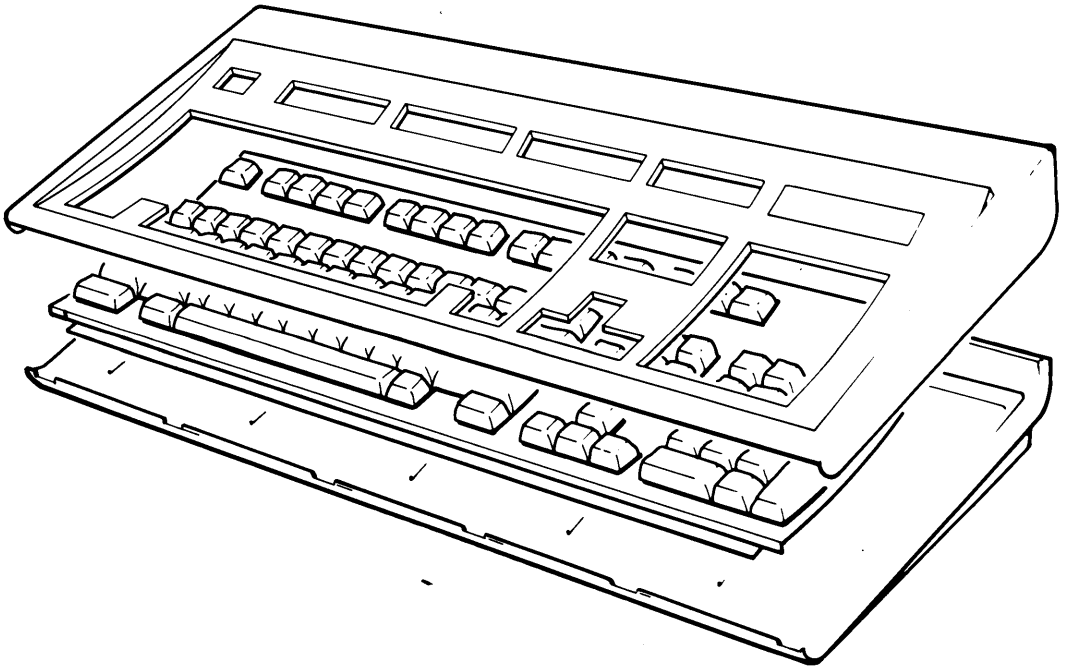
Drive
Speaker
Power Supply
Case
Main
Logic
Board
Power
Supply
PCB



Main Logic Board

Main Logic Board

Introduction

The main unit is the heart of the Tandy 1000 SL. It houses the main logic assembly, system power supply, and floppy disk drive.

The main logic assembly is a large board mounted to the bottom of the main unit and interconnected to the keyboard, power supply, and disk drive by a series of cables.

The power supply is a 67W switching regulator type, designed to provide adequate power capacity for a fully configured system that has all the option slots in use.

The floppy disk drive uses 5¼-inch double-sided, double-density diskettes to read, write, or store data. These are soft sector diskettes. The disk drive assembly comes installed in the main unit. All system programs, with the exception of the system startup sequence, are stored on diskette.

Switch Settings and Jumper Pin Configurations

Main Logic Board

Jumper	Function	Default
E1-E2	Select Video Interrupt on IRQ5	E2-E3
E2-E3	Normal Video Interrupt	

Sound Input/Output Satellite Board

Jumper	Function	Default
E1-E2	Select Direct Line Audio Input	E2-E3
E2-E3	Select Mic Audio Input	

Theory of Operation

8086 Microprocessor

The 8086 (U29) is a high-performance 16-bit microprocessor with internal and external 16-bit data paths, one megabyte of memory address space, and 64K of I/O address space. The 8086 communicates with the rest of the system via a 20-bit multiplexed address/data/status bus and a command bus.

8087 Numerical Math Coprocessor

The 8087 (U21) performs high-speed arithmetic and logarithmic functions and trigonometric operations that increase the performance of an 8086 system. Performance increases are obtained by the 8087's ability to perform math calculations faster than the 8086, and also by executing math instructions in parallel with the 8086.

Clock Generation

Clocks required by the system are generated by TTL oscillator Y2, Y1 and the custom IC 8079024 (U41). There are two independent clock circuits supplied by a Dual Oscillator Clock (Y2,Y1) from which all other clocks, excluding video clocks, are derived.

The 24 MHz Clock is routed into the custom IC 879024, which generates the output signal CPUCLK. The Clock Switch circuitry required to toggle the 8086 Microprocessor between 8 MHz and 4 MHz mode, as well as the logic to prevent any short cycling during a clock switch cycle, are implemented in the custom IC 879024 IC. If Bit 3 is asserted during an I/O write to Port 062 (hex), then the output signal CPUCLK operates the 8086 in 8 MHz mode. If Bit 3 is negated low during an I/O write to Port 062 (hex), the output signal CPUCLK operates the 8086 in the 4 MHz mode. When Reset is generated, the signal RESET is asserted and defaults the Tandy 1000 SL to the 4 MHz mode.

The custom IC 879024 Chip also controls wait states to insert the proper number of wait states required for a two clock mode of operation. Zero to three wait states are inserted in all 8-bit Memory and I/O cycles, in both 8 MHz and 4 MHz modes. These wait states are separately programmable. During all 16-bit memory cycles, either zero or one wait state is inserted in both the 8 MHz and 4 MHz modes. These values are programmable and will be discussed later in the section "Wait State and Ready Logic".

Command and Control Signal Generation

The command and control signals required for the Tandy 1000 SL operation are generated by the 8079024 custom IC. The command signals are decoded from the CPU status signals S0- through S2- during the Ts cycle. The decoded signals indicate the type of cycle that is to be executed (MEMR-, MEMW-, IOR-, IOW-, INTA-). The control signals CPUALE, BUSALE control the external latching of addresses onto the bus. Direction, enabling of the data bus buffers, and start a memory cycle is determined internal to the 8079024 custom IC. The following table indicates the decoding of the CPU status signals.

S0-	S1-	S0-	Type of Bus Cycle
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Code Access
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	None: Idle

CPU Status Signal Decoding.

A0 and BHE- are decoded to determine the data transfer width to and from the CPU. The following table shows the data transfer width depending on the state of A0 and BHE-.

BHE-	A0	Width of Data Transfer
0	0	Word Transfer
0	1	Byte Transfer D8 - D15 (odd address)
1	0	Byte Transfer D0 - D7 (even address)
1	1	Not Used

Data Transfer Width Decode.

DRAM Control

The CPU address decode for the Dynamic Random Access Memory (DRAM) array is generated by the 8079024 custom (U41). These signals are latched by ALE internally to the 8079024 custom IC and held for the complete cycle. The address decode signals are RAS0-, RAS1-, RAS2-, RAS3-, and CAS-. Memory configurations supported by the Tandy 1000 SL are 256K, 512K, or 640K bytes (in addition to 128K of video memory). The following table shows the different options available on the 8079024 custom IC.

Memory Option	MCONFIG1	MCONFIG0	System Memory	Total System Memory*
0	0	0	256K	384K
1	0	1	512K	640K
2	1	0	512K	640K
3	1	1	640K	768K

* Note: Total system memory includes 128K of video memory. Memory Option 0 is the power up default.

Memory Configurations.

The signals WEL- and WEH- provide write control. For a 16-bit access, both are asserted at the same time and are controlled by MEMW- (memory write). For an 8-bit access, the appropriate signal is asserted according to the state of A0 (high byte or low byte).

Refresh Control

Refresh timing is derived internal to the 8079024 custom IC (U41) and provides a 512 count, 8 msec, RAS only refresh for internal memory, and a 256 count, 4 msec, RAS only refresh for the bus.

BIOS ROM Control

The 8079024 custom IC (U41) provides the CPU address decode used for the ROM select. The signals generated are called ROMCS0- and ROMCS1 (ROM Chip Select). The 8079024 custom IC then generates the ROM Page Selects (RP0-RP4) and Chip Enable for the BIOS ROMs CU16 and CU17. These outputs are decoded from Address Bits A16-A19 and IOD0-IOD4. RP0-RP4 may be programmed by writing to Port FFE8 hex Bits 0 - 4. The appropriate ROM page selects are multiplexed with I/O decodes, and appear on DEC0-DEC2 during a memory address cycle in the ROM area.

Reset Circuit

The 8079024 custom IC (U41) controls the system reset required either to initialize the complete system after power-up or to reboot. The reset output signals, RSTIN-, is active low and generated when a power-up condition is detected or when the reset button on the front of the computer is pressed.

The RSTIN- signal is supplied to the 8079024 custom IC which produces the RESET signal. The RESET signal is used as a general system reset. The 8079024 custom IC (U41) also internally controls the RESET signal to meet the requirements of the 8086 during a detected shutdown condition.

Wait State and Ready Logic

Wait state control is implemented internally to the 8079024 custom IC. The function of the wait state control logic is to match the speed of the various devices in the Tandy 1000 SL to the speed of the 8086 CPU. A programmable wait state generator is contained within the 8079024 custom IC and can be accessed by writing to Port FFE9 hex. The following is a table of programmable wait states and their default values.

Port FFE9h

Bit(s)	Default	Description
0	0	Internal Memory Wait States 0 = 0 wait states 1 = 1 wait states
1,2	0,0	External Memory Wait States 00 = 0 wait states 01 = 1 wait states 10 = 2 wait states 11 = 3 wait states
3,4	0,0	I/O Cycle Wait States 00 = 0 wait states 01 = 1 wait states 10 = 2 wait states 11 = 3 wait states
5	0	DMA Cycle Wait States 0 = Write Strobe wait 1 = Standard 8137 Write Strobe
6	0	Internal Video Wait States 0 = 0 wait states 1 = 1 wait states
7	1	OSCIN Select 0 = 28.63636 MHz 1 = 24 MHz

Programmable Wait State Control

Another method is controlled by the device being accessed, using the IOCHRDY signal input to the 8079024 custom IC. If a device requires additional wait states within the bus cycle, the device should negate IOCHRDY low until it can service the bus cycle. After the required number of wait states have been inserted, the device should assert IOCHRDY, causing the READY output of the 8079024 custom IC to be asserted high, which tells the CPU to terminate the cycle.

(Note: IOCHRDY should not be held low for longer than 15 usec).

NMI Logic

In the Tandy 1000 SL, the Non-Maskable Interrupt (NMI-) indicates an I/O error condition, or Numerical Math Coprocessor 8087 error condition. Both error conditions are being generated internal to the 8079024 custom IC.

8087 Control Logic

The 8087 Numerical Coprocessor is connected to the 8086 address and data lines in parallel. The 8087 will monitor the 8086 CPU status (S0-S2) and Queue status (QS0-QS1) in order to decode instructions in synchronization with the CPU. For resynchronization, the 8087 NPBUSY signal is used to tell the CPU that the 8087 is executing an instruction. The 8087 also has the capability of informing the 8086 of an error or exception by using the NPINT signal. This signal is sent to the 8079024 custom IC which then generates the proper codes to the 8086. The 8087 will use the RQ/GT0- signal to gain control of the bus for data transfers.

CPU Address Buffers

The 8079024 custom IC provides the buffering of the address lines to the system. A0-A19 are buffered and latched for the expansion bus slots and I/O peripherals. ALE is used to latch A0-A11 internal to the 8079024 custom IC and CPUALE is used to latch A12-A19 externally. The addresses are held for the complete bus cycle. A0-A19 are also used to address the BIOS ROMS and DRAM/DMA Control. The multiplexed address lines MA0-MA8 are also generated and buffered to the DRAM memory by the 8079024 custom IC.

Data Buffers and Conversion Logic

The 8079024 custom IC provides the data buses, buffers, and drivers for D0-D15 to the system. Two data buses are generated, IOD0-IOD7 for the expansion bus slots, and AD0-AD15, which is routed to the 8086 CPU, 8087 Coprocessor data bus, ROM, and DRAM. The direction and control of the data buffers are provided internal to the 8079024 custom IC. Conversion logic is also implemented in the 8079024 custom IC. This conversion logic allows data to be transferred from the lower to upper or upper to lower data byte to meet the requirements of the CPU or receiving device.

I/O Decode

The 8079024 custom IC accomplishes the I/O Address decoding. This IC provides all the necessary chip select signals to the system. The DEC0-, DEC1-, and DEC2- output signals of the 8079024 custom IC are encoded device select lines that are fed directly to the KFIT custom IC (U30) and 8079021 custom IC (U40), in which I/O address decoding is generated.

Floppy Disk Controller

The on-board Floppy Disk Controller (FDC) and KFIT custom IC (U30) interface the system to the Floppy Disk Drive (FDD). Up to two internal 5¼-inch 360K or one 5¼-inch and one 3½-inch FDDs can be accommodated.

The FDC circuit can be organized into the following subsections:

- uPD765A FDC Chip
- System Interface
- Clock Generation
- Precompensation
- Data Separator
- Disk Drive Interface

uPD765A Chip. The uPD765A FDC chip (EU4) integrates most of the control logic necessary to:

- interface the serial bit stream to or from the FDD to the parallel bus of the system
- implement the commands necessary to operate the FDD
- maintain information about the status of the FDD

During a read or write data operation to the FDD, the FDC chip generates a DMA request for a byte transfer to or from memory. The FDC chip continues to generate DMA requests until the preprogrammed amount of data is transferred as signified by generation of a Termination Count (DMATC) Signal. After the DMATC is reached, the FDC chip generates an interrupt to the system through INT so that status and result data can be serviced.

System Interface. Various ICs, along with the KFIT custom IC, latch and buffer data to and from the system. A DOR Write (Digital Output Register) is generated on an I/O write to Port 3F2 (hex). This signal latches the data byte that is bit defined as the Drive Select, DS0-, DS1-, and DS2-, Motor On, MTRON-, DMA, (FDCDRQ), Interrupt Request (FDCINT), and a reset signal (FDCRST-) to the FDC controller U12.

Clock Generation. The FDC Support IC (U18) generates all clocks required by the Floppy Disk circuit. These clocks are derived from a 16 MHz input signal. FDCCLK, required by the FDC Controller (U12), is derived by dividing the 16 MHz clock by 4. The resulting 4 MHz clock is also used as a delay counter for the DMA request signal DRQ as well as a reference clock for the write precompensation circuit. The 4 MHz clock also generates a 250 nanosecond pulse at a frequency of 500 KHz. The 500 KHz signal is used as a write clock for the FDC Controller.

Precompensation. The precompensation circuit is implemented internally to the FDC Support IC (U18). The write data bit can be shifted either early or late in the serial bit stream, depending on the requirements of the Floppy Disk Drive. This function is programmable and controlled by the FDC IC signals PS0 and PS1.

Data Separator. The FDC Support IC (U18) also contains the data separator circuit. The data separator recovers the clock and data signals from the serial bit stream of the Floppy Disk Drive. The FDC Support IC supports only MFM or Double-density mode.

Disk Drive Interface. All FDC outputs to the FDD are driven by high current 7414 SCHMITT trigger buffers or 7416 open collector inverters. All FDC inputs from the FDD are buffered by 74HCT14 SCHMITT triggered inverters. The inputs are pulled up on-board by 1K terminating resistors. All outputs should be terminated on the last FDD by 1K resistors.

Interrupt Controller

The Interrupt Controller is contained in the KFIT custom IC (U30) and supplies the maskable interrupt input to the CPU. The KFIT custom IC has eight interrupt inputs controlled through software commands. It can mask (disable) and prioritize (arrange priority) to generate the interrupt input to the CPU. The eight interrupts are assigned as follows:

#0	Timer Channel 0	Software Timer
#1	Keyboard	Keyboard Code Received
#2	Interrupt on the Bus	Optional Bus Interrupt
#3	Interrupt on the Bus	Modem (COM2)
#4	Interrupt on the Bus	RS-232 (COM1)
#5	Vertical Sync/HDC	Hard Disk Controller/ Video Vertical sync
#6	Floppy Disk Controller	Optional Bus Interrupt
#7	Printer/Sound/DMA	Optional Bus Interrupt

Interrupts 0 and 1 are connected to system board functions as indicated in the chart. Interrupts 2-7 are connected directly to the Expansion Bus, with the normal assigned functions listed in the chart.

Video Controller

The next major block of the Tandy 1000 SL is the video interface circuitry. This custom part contains all the logic necessary to generate an IBM-compatible color video display. The video interface logic consists of the 100-pin custom video circuit (U26), four 64K X 4 DRAMS (U6, U7, U8, and U9), a 74LS273 latch (Ul4), a 16K X 8 character ROM, and associated logic for generating RGBI or Monochrome video.

The Tandy 1000 SL video interface circuitry controls 128K of memory. This DRAM is shared by the CPU and the video. Normally, the video requires only 16K or 64K for the video screen, and the remainder of the 128K is available for system memory use.

The Tandy 1000 SL video interface custom circuit is composed of a 6845 equivalent design, dynamic RAM address generation/timing, and video attribute controller logic.

Normal function of the video interface custom circuit is as follows. After the 6845 is programmed with a correct set of operating values, a 6:1 multiplexer generates the address inputs to the dynamic RAMs. This MUX switches between video (6845) address and CPU address as well as between row and column address. Also, the video interface chip provides the RAM timing signals and generates a wait signal, VIDWT-, to the CPU for proper synchronization with the video RAM access cycles.

The outputs from the RAM chips are only connected to the video interface custom circuit, so all CPU read/write operations are buffered by this part. During a normal display cycle, video data from the RAM chips is first latched in the Video Attribute latch and the Video Character latch. The video interface requires a memory organization of 64K X 16 and latches 16 bits of memory during each access to RAM. From the output of the two latches, the data is supplied to the character ROM for the alpha modes or to the shift registers for the graphics modes. A final 2:1 MUX switches between foreground or background in the alpha modes.

From the 2:1 MUX, the RGBI data is combined with the PC color select data and latched in the Pre-Palette latch. This latch synchronizes the RGBI data before it is used to address the Palette. The Palette mask MUX switches between incoming RGBI data and the Palette address register. During a CPU write to the Palette, this address register selects one of the 16 Palette locations. Also, the Palette mask MUX allows any of the input RGBI bits to be set to zero.

The Palette allows the 16 colors to be remapped in any desired organization. Normally, the Palette is set for a 1:1 mapping (red = red, blue = blue, and so on) for PC compatibility. However, instantly changing the on-screen colors is a powerful tool for animation or graphics programs.

After the Palette, the RGBI data is resynchronized in the Post Palette register. The final logic before the RGBI data is buffered off the chip in the Border MUX. This MUX allows the Border to be replaced with any color selected by the border color latch. This latch is normally disabled in PC modes, but it is used in all PC jr modes.

Timer

The final Tandy 1000 SL function other than I/O is the timer found in the KFIT custom IC (U30). This part is composed of three independent programmable counters. The clock for all three counters is 1.1931 MHz, which is derived from 14.318 MHz/12. Counters 0 and 1 are permanently enabled. Counter 2 is controlled by port Hex 0061, Bit 0. Counter 0 is connected to system interrupt 0 and is used for software timing functions. Counter 1 is used for refresh function timing. Counter 2 is connected to the sound circuit and its output can be read at port Hex 0062, Bit 5.

Joystick Interface

The joystick interface contained in the 8079021 custom IC (U40) converts positional information from hand-held joysticks (1 or 2) into CPU data. Each joystick provides one or two push-buttons and X, Y position for a total of four bits each. Two joysticks can be used.

The joystick handle is connected to two potentiometers mounted perpendicular to each other; one for X position, one for Y position. Through the cable, the main logic board applies +5 VDC to one side and ground to the other of the pots. The pot wiper is the position signal: a voltage between 0 and +5 VDC. This signal is applied to one input of a comparator HU2. The other comparator input is the reference signal (a ramp between 0.0 to +5.0 volts).

When the position signal is equal to or less than the reference signal, the comparator output goes true. This comparator output is the X or Y position data bit. The ramp is reset to 0.0 VDC whenever an I/O Write is made at Port 200/201 Hex. The joystick information is "read" by the CPU at Port 200/201 Hex through U40.

Keyboard Interface

The next I/O function of the Tandy 1000 SL is the Keyboard interface custom circuit, part of the KFIT custom IC. The heart of this custom part is several read/write registers that are used to control the keyboard interface logic. For the interface to the keyboard connector, a 164-type shift register is used to load the serial data and allow the CPU to read it as 8 parallel bits.

Sound Circuit

The sound circuit is one of the five I/O functions of the Tandy 1000 SL. The circuit provides sound output for the internal speaker as well as for an external sound circuit.

The main source of sound in the Tandy 1000 SL is the 8079021 custom IC (U40). It contains the equivalent of a 76496 complex sound generator. This device has three tone generators and one white noise generator. Each tone generator can be programmed for frequency and attenuation. Also, this device has an audio input pin connected to the gated output of timer channel 2. This audio input signal is mixed with the sound generator signal and supplied to the audio output pin.

The output of the 76496 enables Port 61, Bit 4, which turns off the audio signal to the speaker, headphone jacks, and external audio output. The output of the 76496 is routed to audio amplifiers HU3 for the external audio output and HU4 for the internal speaker and headphone jacks. The volume of the internal speaker can be adjusted by a user-accessible volume control (HR14). When the headphone jack is used, the internal speaker is disabled.

Additional Sound Features (DAC)

An additional feature of the Tandy 1000 SL sound circuitry is a Digital to Analog Converter (DAC). The DAC is controlled by read/write Ports C4-C7. The DAC can be used to convert pre-recorded digital sound, voice, or music into analog audio output. A microphone jack and audio input circuitry are provided for recording analog sound, voice or music, and converting it to digital data. Bit programming data for these ports is available in the data sheets on the 8079021 custom IC located in the "Devices" section of this manual.

DMA Controller

The major components of the Direct Memory Access (DMA) circuit consists of an 8237A-5 equivalent DMA controller, DMA control logic, and a bi-directional address buffer internal to the 8079024 custom IC.

A DMA Operation. When a DMA operation is requested by software or by a peripheral through a DREQ line, the 8079024 custom IC initiates a Bus Hold Request to the 8086 CPU. The 8079024 custom IC arbitrates the CPU Hold Request from the internal DMA controller to the CPU.

When the CPU acknowledges the Hold request, the CPU control, address, and data lines are tri-stated. The 8079024 custom IC controls the direction and enables the memory or peripheral address and data buses that correspond to the requested DMA operation.

During the DMA operation, the 8237A-5 internal to the 8079024 custom IC acts as the bus master and, along with the associated logic, generates all bus control signals and address and data signals. The DMA transfers continue for the number of counts and to the destination address that was previously programmed into the DMA registers. See the device data sheet and the I/O map for complete descriptions of the registers, their locations, and their functions.

I/O devices can extend the DMA bus cycle by controlling the IOCHRDY signal of the expansion bus. Setup times must be observed for IOCHRDY to be recognized.

RS-232 Serial Port Interface

The RS-232 Port is a single-channel, asynchronous communications port. The heart of the serial port is the 8079021 custom IC (U40) that functions as a serial data input/output interface. It performs serial-to-parallel conversion on data characters received from a peripheral device or modem and parallel-to-serial conversion on data characters received from the CPU.

Status information reported includes the type and condition of the ACE's transfer operations as well as any error conditions detected during serial data operations. The 8079021 custom IC includes a programmable Baud Rate Generator that allows operation from 50 to 9600 Baud. The 8079021 custom IC is supplied with a clock of 24 MHz from the main Crystal Oscillator. The 8079021 can be tailored to the user's requirements by being able to remove start bits, stop bits, and parity bits. It supports 5, 6, 7, or 8 data bit characters with 1, 1½, or 2 stop bits. Diagnostic capabilities provide loopback functions of transmit/receive and input/output signals.

The 8079021 custom IC serial port is programmed by selecting the I/O address 3F8 - 3FE hex and writing data out to the port. Address Bits A0, A1, and A2 are used to define the modes of operation by selecting the different registers to be programmed or read. One interrupt is provided to the system from IRQ4.

Parallel Printer Port Interface

The final I/O interface of the Tandy 1000 SL is the Printer Interface contained in the 8079021 custom IC (U40). This part supplies all the signals required to interface to a typical parallel printer. These signals are 8 data out lines, plus various handshake control signals. Also, the printer interface generates an interrupt to the CPU if enabled.

Expansion Ports

System Expansion Bus

This section identifies the I/O interface requirements for the 8-bit, PC-compatible option cards. Each of the five slots has a 62-pin connector socket.

The following connector pin assignment is used on the PC option slots; this connector socket has 62 pins.

Pin	Signal Name	I/O	Pin	Signal Name	I/O
A1	NMI-	I	B 1	GND	GROUND
A2	IOD7	I/O	B 2	RESET	O
A3	IOD6	I/O	B 3	+5V	POWER
A4	IOD5	I/O	B 4	IRQ2	I
A5	IOD4	I/O	B 5	-5V	POWER
A6	IOD3	I/O	B 6	DRQ2	I
A7	IOD2	I/O	B 7	-12V	POWER
A8	IOD1	I/O	B 8	N/C	
A9	IOD0	I/O	B 9	+12V	POWER
A10	IOCHRDY	I	B10	GND	GROUND
A11	HLDA	O	B11	MEMW-	O
A12	A19	O	B12	MEMR-	O
A13	A18	O	B13	IOW-	O
A14	A17	O	B14	IOR-	O
A15	A16	O	B15	DACK3-	O
A16	A15	O	B16	DRQ3	I
A17	A14	O	B17	DACK1-	O
A18	A13	O	B18	DRQ1	I
A19	A12	O	B19	REFRSH-	O
A20	A11	O	B20	BCPUCL	O
A21	A10	O	B21	IRQ7	I
A22	A9	O	B22	IRQ6	I
A23	A8	O	B23	IRQ5	I
A24	A7	O	B24	IRQ4	I
A25	A6	O	B25	IRQ3	I
A26	A5	O	B26	DACK2-	O
A27	A4	O	B27	DMATC	O
A28	A3	O	B28	BUSALE	O
A29	A2	O	B29	+5V	POWER
A30	A1	O	B30	14MHz	O
A31	A0	O	B31	GND	GROUND

Expansion Bus Signal Description

The following signal descriptions for the System I/O Bus are for PC bus-compatible option cards. Note that all signal lines are TTL compatible levels and that I/O adapters should be designed with a maximum of two low power Shottky (LS) loads per line.

BCPUCLK (B20). BCPUCLK is the System clock and has a period of 125ns in 8 MHz mode, or 250ns in 4 MHz mode. It has a 50% duty cycle and is used only for synchronization with the CPU. It is not intended for uses requiring a fixed frequency.

A0 through A19 (A12-A31). These lines are 20 address bits used to address memory and I/O devices within the Tandy 1000 SL. They are gated on the system bus when the BUSALE signal is high and are latched on the falling edge of the BUSALE signal. Generation of these signals is accomplished by the CPU or a DMA controller. A0-A19 are active high.

BUSALE (B28). BUSALE is a Buffered Address Latch Enable generated by the CPU Control IC. It is used to latch valid addresses from the CPU, and can be used by an I/O board to indicate a valid CPU address, in conjunction with HLDA. BUSALE is active high.

HLDA (A11). HLDA is an Address Enable signal used to remove the CPU and other devices from the bus to allow DMA transfers to take place. During HLDA active, the DMA controller has control of the address bus, the data bus, the READ command lines, and the WRITE command lines. HLDA is active high.

IOD0 through IOD7 (A2-A9). These signals are the data bus I/O Bits 0 through 7 from the CPU to memory and I/O devices on the bus. IOD0 is the least significant bit (lsb), and IOD7 is the most significant bit (msb).

BRESET (B2). BRESET is used to reset or initialize the expansion logic during power-up time, line voltage outage, or when the Reset switch on the front panel is pressed. BRESET is active high.

NMI- (A1). This signal indicates an uncorrectable system error when active. The NMI- signal provides the system board with parity information about memory or devices on the bus. NMI- is active low.

IOCHRDY (A10). This signal is used to lengthen I/O or memory cycles when driven low by the active device. (This signal should not be held low more than 15 microseconds.) Any slow device using this line should drive it low immediately upon detecting its valid address and a READ or WRITE command. See the timing diagram for setup times. IOCHRDY is active high (Ready condition).

IRQ2 through IRQ7 (B4, B21-B25). These signals are used to tell the CPU that an I/O device needs attention. The Interrupt Requests are prioritized with IRQ2 having the highest priority and IRQ7 the lowest. An Interrupt Request is generated when any IRQ signal is driven high and held high until the CPU acknowledges the interrupt.

IOR- (B14). IOR- is a read signal that instructs an I/O device to drive its data onto the data bus (IOD0-IOD7). This line can be driven by the CPU Control IC or by the DMA controller. IOR- is active low.

IOW- (B13). IOW- is a write signal that instructs an I/O device to read, or latch, the data from the data bus (IOD0-IOD7). This line can be driven by the CPU Control IC or by the DMA controller. IOW- is active low.

MEMR- (B12). MEMR- is a read signal that instructs a memory device to drive its data onto the appropriate data bus (IOD0-IOD7). This line can be driven by the CPU Control IC or by the DMA controller through the CPU Control IC. MEMR- is active low.

MEMW- (B11). MEMW- is a write signal that instructs a memory device to read, or latch, the data from the appropriate data bus (AD0-AD15 for 16-bit memory, IOD0-IOD7 for 8-bit memory). This line can be driven by the CPU Control IC or by the DMA controller through the CPU Control IC. MEMW- is active low.

DRQ1, DRQ2, and DRQ3 (B18, B6, B16). These lines are asynchronous DMA requests by peripheral devices to gain DMA service. They are prioritized with DRQ1 having the highest priority, DRQ2 next, and DRQ3 lowest. A DMA request is generated by driving a DRQ line active high and holding it until the corresponding DACK (DMA acknowledge) signal goes active. DRQ1, DRQ2, and DRQ3 perform only 8-bit transfers. All DRQ lines are active high.

DACK1-, DACK2-, and DACK3-, B17, B26, B15). These lines are DMA acknowledge signals used to acknowledge DMA requests DRQ1, DRQ2, and DRQ3. All DACK signals are active low.

REFRSH- (B19). This signal is used to indicate a refresh cycle that can be used by a memory board to refresh Dynamic memory. REFRSH- is active low and 4 cycles are generated every 62.5 usec.

DMATC (B27). DMATC is a signal that provides a pulse when the terminal count for any DMA channel is reached. DMATC is active high.

14MHz (B30). 14 MHz is an oscillator signal that is a high-speed clock with a 70 nanosecond period (14.31818 megahertz). It has a 50% duty cycle.

Memory Map

Address	Name	Allocated Function
00000-7FFFF	512K System RAM	System Memory
80000-9FFFF	128K System/Video RAM	System Memory and Video Display Memory or System Memory
A0000-BFFFF	128K Video RAM	Reserved for Graphics Display Memory
C0000-DFFFF	128K Expansion Memory	Reserved for Above Board
E0000-FFFFF	128K BIOS ROM	Reserved For BIOS

I/O Port Map of System

I/O Port Map Summary

Block	Usage	Function
0000-001F	0000-001F	DMA Function
0020-003F	0020-0027	Interrupt Controller
0040-005F	0040-0047	Timer
0060-007F	0060-006F	PIO Function
0080-009F	0080-009F	DMA Page Register
00A0-00BF	00A0	NMI- Mask Register
00C0-00DF	00C0-00C7	Sound Generator
00E0-00FF	00E0-00FF	Numerical Coprocessor
0100-01FF		Reserved
0200-020F	0200-0207	Joystick Interface
0210-02F7		Reserved
02F8-02FF	02F8-02FF	Serial Port Secondary (COM2)
0300-031F		Reserved
0320-032F		Hard Disk Controller (optional)
0330-036F		Reserved
0370-0377	0370-0377	Floppy Disk Controller 2 (optional)
0378-037F	0378-037F	Printer
0380-03CF		Reserved
03D0-03DF	03D0-03DF	System Video
03E0-03EF		Reserved
03F0-03F7	03F0-03F7	Floppy Disk Controller 1
03F8-03FF	03F8-03FF	Serial Port Primary (COM1)
0400-FFE7		Not Usable
FFE8-FFEF		System Programming Options

Address	Description
0000	DMA Controller IOW- = 0: Channel 0 Base and Current Address Internal Flip/Flop = 0: Write A0-A7 Internal Flip/Flop = 1: Write A8-A15 IOR- = 0: Channel 0 Current Address Internal Flip/Flop = 0: Read A0-A7 Internal Flip/Flop = 1: Read A8-A15
0001	DMA Controller IOW- = 0: Channel 0 Base and Current Word Count Internal Flip/Flop = 0: Write W0-W7 Internal Flip/Flop = 1: Write AW-W15 IOR- = 0: Channel 0 Current Word Count Internal Flip/Flop = 0: Read W0-W7 Internal Flip/Flop = 1: Read W8-W15
0002	DMA Controller IOW- = 0: Channel 1 Base and Current Address Internal Flip/Flop = 0: Write A0-A7 Internal Flip/Flop = 1: Write A8-A15 IOR- = 0: Channel 1 Current Address Internal Flip/Flop = 0: Read A0-A7 Internal Flip/Flop = 1: Read A8-A15
0003	DMA Controller IOW- = 0: Channel 1 Base and Current Word Count Internal Flip/Flop = 0: Write W0-W7 Internal Flip/Flop = 1: Write AW-W15 IOR- = 0: Channel 1 Current Word Count Internal Flip/Flop = 0: Read W0-W7 Internal Flip/Flop = 1: Read W8-W15

Address	Description
0004	DMA Controller
	IOW- = 0: Channel 2 Base and Current Address
	Internal Flip/Flop = 0: Write A0-A7 Internal Flip/Flop = 1: Write A8-A15
	IOR- = 0: Channel 2 Current Address
	Internal Flip/Flop = 0: Read A0-A7 Internal Flip/Flop = 1: Read A8-A15
0005	DMA Controller
	IOW- = 0: Channel 2 Base and Current Word Count
	Internal Flip/Flop = 0: Write W0-W7 Internal Flip/Flop = 1: Write AW-W15
	IOR- = 0: Channel 2 Current Word Count
	Internal Flip/Flop = 0: Read W0-W7 Internal Flip/Flop = 1: Read W8-W15
0006	DMA Controller
	IOW- = 0: Channel 3 Base and Current Address
	Internal Flip/Flop = 0: Write A0-A7 Internal Flip/Flop = 1: Write A8-A15
	IOR- = 0: Channel 3 Current Address
	Internal Flip/Flop = 0: Read A0-A7 Internal Flip/Flop = 1: Read A8-A15
0007	DMA Controller
	IOW- = 0: Channel 3 Base and Current Word Count
	Internal Flip/Flop = 0: Write W0-W7 Internal Flip/Flop = 1: Write AW-W15
	IOR- = 0: Channel 3 Current Word Count
	Internal Flip/Flop = 0: Read W0-W7 Internal Flip/Flop = 1: Read W8-W15

Address	Description
0008	DMA Controller

IOW- = 0, Write Command Register

Bit	Description
0	0 = Memory to Memory Disable 1 = Memory to Memory Enable
1	0 = Channel 0 Address Hold Disable 1 = Channel 0 Address Hold Enable X If Bit 0 = 0
2	0 = Controller Enable 1 = Controller Disable
3	0 = Normal Timing 1 = Compressed Timing X If Bit 0 = 1
4	0 = Fixed Priority 1 = Rotating Priority
5	0 = Late Write Selection 1 = Extended Write Selection X If Bit 3 = 1
6	0 = DREQ Sense Active High 1 = DREQ Sense Active Low
7	0 = DACK Sense Active Low 1 = DACK Sense Active High

IOR- = 0, Read Status Register

Bit	Description
0	1 = Channel 0 Has Reached DMATC
1	1 = Channel 1 Has Reached DMATC
2	1 = Channel 2 Has Reached DMATC
3	1 = Channel 3 Has Reached DMATC
4	1 = Channel 0 Request
5	1 = Channel 1 Request
6	1 = Channel 2 Request
7	1 = Channel 3 Request

Address	Description
0009	DMA Controller

IOW- = 0, Write Request Register

Bit Description

Bits 0-1

Bit 1	Bit 0	
0	0	Select Channel 0
0	1	Select Channel 1
1	0	Select Channel 2
1	1	Select Channel 3

Bit 2

0	Reset Request Bit
1	Set Request Bit

Bits 3-7 Don't Care

IOR- = 0, Illegal

000A DMA Controller

IOW- = 0, Write Single Mask Register

Bit Description

Bits 0-1

Bit 1	Bit 0	
0	0	Select Channel 0 Mask Bit
0	1	Select Channel 1 Mask Bit
1	0	Select Channel 2 Mask Bit
1	1	Select Channel 3 Mask Bit

Bit 2

0	Clear Mask Bit (Enable Channel)
1	Set Mask Bit (Disable Channel)

Bits 3-7 Don't Care

IOR- = 0, Illegal

Address	Description

000B DMA Controller

IOW- = 0, Write Mode Register

Bit Description

Bits 0-1

Bit 1	Bit 0	
0	0	Channel 0 Select
0	1	Channel 1 Select
1	0	Channel 2 Select
1	1	Channel 3 Select

Bits 2-3

Bits 3	Bit 2	
0	0	Verify Transfer
0	1	Write Transfer To Memory
1	0	Read Transfer To Memory
1	1	Illegal
X	If Bits 6 and 7 = 11	

Bit 4

0	Autoinitialization Enable
1	Autoinitialization Disable

Bit 5

0	Address Increment Select
1	Address Decrement Select

Bits 6-7

Bit 7	Bit 6	
0	0	Demand Mode Select
0	1	Single Mode Select
1	0	Block Mode Select
1	1	Cascade Mode Select

IOR- = 0, Illegal

000C DMA Controller

IOW- = 0, Clear Byte Pointer Flip/Flop
IOR- = 0, Illegal

Address	Description
000D	DMA Controller IOW- = 0, Master Clear IOR- = 0, Read Temporary Register
000E	DMA Controller IOW- = 0, Clear Mask Register IOR- = 0, Illegal
000F	DMA Controller IOW- = 0, Write All Mask Register Bits Bit Description 0 0 = Clear Channel 0 Mask Bit (Enable) 1 = Set Channel 0 Mask Bit (Disable 1 0 = Clear Channel 1 Mask Bit (Enable) 1 = Set Channel 1 Mask Bit (Disable 2 0 = Clear Channel 2 Mask Bit (Enable) 1 = Set Channel 2 Mask Bit (Disable 3 0 = Clear Channel 3 Mask Bit (Enable) 1 = Set Channel 3 Mask Bit (Disable 4-7 Don't Care IOR- = 0, Illegal
0010 - 001F	Same as 0000-000F

Address	Description
0020	8259A Interrupt Controller

Note: Initialization Words are set up by the operating system and are generally not to be changed. Writing an initialization word might cancel pending interrupts.

Bit 4 = 1 Initialization Command Word 1

Bit 0
- 0 ICW4 Needed
- 1 ICW4 Not Needed

Bit 1
- 0 Cascade Mode
- 1 Single Mode

Bit 2 Not Used

Bit 3
- 0 Edge Triggered Mode
- 1 Level Triggered Mode

Bits 5-7 Not Used

Bit 4 = 0 Operation Control Word 2

Bit 3 = 0 Bit0-2: Determine The Interrupt Level Acted On When the SL Bit Is Active

Interrupt Level = 0 1 2 3 4 5 6 7

Bit 0 (L0): 0 1 0 1 0 1 0 1
Bit 1 (L1): 0 0 1 1 0 0 1 1
Bit 2 (L2): 0 0 0 0 1 1 1 1

Bits 5-7: Control Rotate and End of Interrupt Modes

B7	B6	B5		
0	0	1	Non-Specific EOI Command	End Of Interrupt
0	1	1	Specific EOI Command	End Of Interrupt
1	0	1	Rotate On Non-Specific EOI	Auto Rotation
1	0	0	Rotate In Automatic EOI Mode	(Set) Auto Rotation
0	0	0	Rotate In Automatic EOI Mode	(Clear) Auto Rotation
1	1	1	*Rotate On Specific EOI Command	Specific Rotation
1	1	0	*Set Priority Command	Specific Rotation
0	1	0	No Operation	

(*L0 - L2 Are Used)

Address	Description
0020	8259A Interrupt Controller

Bit 4 = 0 & Bit 3 = 1 — Operation Control Word 3

Bit 0-1:

Bit 1	Bit 0	Read Register Command
0	0	No Action
0	1	No Action
1	0	Read IR Register On Next IOR- Pulse
1	1	Read IS Register On Next IOR- Pulse

Bit 2

0	No Poll Command
1	Poll Command

Bits 5-6

Bit 5	Bit 6	Special Mask Mode
0	0	No Action
0	1	No Action
1	0	Reset Special Mask
1	1	Set Special Mask

Bit 7 = 0

0021 8259A Interrupt Controller

Initialization Control Word 2

Bits 0-7: Not Used

Bits 3-7: T3-T7 of Interrupt Vector Address (8086/8088/80286 Mode)

Initialization Control Word 3 (Master Device)

Bits 0-7		
	1	Indicated IR Input Has a Slave
	0	Indicated IR Input Does Not Have a Slave

Address	Description
0021	8259A Interrupt Controller

Initialization Control Word 3 (Slave Device)

Bits 0-2 ID0-2

Bit 0	Bit 1	Bit 2	Slave ID #
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Bits 3-7 0 (Not Used)

Initialization Control Word 4

Bit 0 Type Of Processor

0	MCS-80/85 Mode
1	8086/8088/80286 Mode

Bit 1 Type of End of Interrupt

0	Normal EOI
1	Auto EOI

Bits 2-3 Buffering Mode

Bit 3	Bit 2	
0	X	Non-Buffered Mode
1	0	Buffered Mode/Slave
1	1	Buffered Mode/Master

Bit 4 Nesting Mode

0	Not Special Fully Nested Mode
1	Special Fully Nested Mode

Bit5-7 0 (Not Used)

Address	Description
0021	8259A Interrupt Controller
	Operation Control Word 1 (IOR-
	Bits 0-7 Interrupt Mask For IRQ0-IRQ7
	0 Mask Reset (Enable)
	1 Mask Set (Disable)

Note: Peripherals requesting an interrupt service must generate a low to high edge and then remain at a logic high level until service is acknowledged. Failure to do so results in a Default Service for IRQ7.

0022-0027 Same as 0020-0021

0028-003F Not Used

0040/0044 8254-2 Timer

IOW- = 0: Load Counter No. 0
IOR- = 0: Read Counter No. 0

0041/0045 8254-2 Timer

IOW- = 0: Load Counter No. 1
IOR- = 0: Read Counter No. 1

0042/0046 8254-2 Timer

IOW- = 0: Load Counter No. 2
IOR- = 0: Read Counter No. 2

Address	Description

0043/0047 8254-2 Timer

IOW- = 0: Write Mode Word

Control Word Format

Bit 0 BCD

0	BCD Counter (4 Decades)
1	Binary Counter 16 Bits

Bits 1-3 Mode Selection

Bit 3	Bit 2	Bit 1	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

0043/0047 8254-2 Timer

Bits 4-5: Read/Load

Bit 5	Bit 4	
0	0	Counter Latching Operation
0	1	Read/Load LSB Only
1	0	Read/Load MSB Only
1	1	Read/Load LSB First, Then MSB

Bits 6-7 Select Counter

Bit 7	Bit 6	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

IOR- = 0: No-Operation 3-State

0048-005F Not Used

Address	Description
0060	Port A / Keyboard Interface Control Ports (Read Only)

Bit	Description
0	Keyboard Bit 0-LSB
1	Keyboard Bit 1
2	Keyboard Bit 2
3	Keyboard Bit 3
4	Keyboard Bit 4
5	Keyboard Bit 5
6	Keyboard Bit 6
7	Keyboard Bit 7-MSB

0061 Port B Read or Write

Bit	Description
0	1 = 8253 Gate 2 Enable
1	1 = Speaker Data Out Enable
2	Not Used
3	Not Used
4	1 = Disable Internal Speaker (Sound Control2)
5	Not Used
6	0 = HOLOCK (If IBM PC Keyboard Mode)
7	1 = Keyboard Clear

Address	Description

0062 Port C Read/Write: Bits 0-3; Read Only: Bits 4-7

Bit	Description
0	Read/Write - Not Used
1	Read/Write - Not Used
2	Read/Write - Not Used
3	(Output) CPU Clock Rate 0 = 4.00 MHz (PC Compatible Rate) 1 = 8.00 MHz (Default By Boot ROM)
4	Video RAM Size 0 = 128K Video 1 = 256K Video
5	8253 Out #2
6	Monochrome Mode 0 = Color Monitor 1 = 350 Line Monitor, Mono
7	Reserved

0063-0064 Reserved

0065 Planar Control Register

Bit	Description
0	Hard Disk Port Select
1	Parallel Port Select
2	Video Port Select
3	Floppy Disk Port Select
4	Serial Port Select
5	Not Used
6	Not Used
7	Parallel Port Output Enable

0066 Reserved

0067 Port H Reserved

0068-007F Reserved

0080 DMA Page Register (Reserved for Diagnostics)
Write Only

0081 DMA Channel 2 Page Register -Write Only

Address	Description
Bit 0	Address A16
Bit 1	Address A17
Bit 2	Address A18
Bit 3	Address A19

Address	Description
0082	DMA Channel 3 Page Register -Write Only

Address	Description
Bit 0	Address A16
Bit 1	Address A17
Bit 2	Address A18
Bit 3	Address A19

0083 DMA Channel 0-1 Page Register -Write Only

Address	Description
Bit 0	Address A16
Bit 1	Address A17
Bit 2	Address A18
Bit 3	Address A19

0084-008F Same as 0080-0083

00A0 NMI- Mask Register, Write Only

Bit		Description
0-6		Not Used
7	1	NMI- Enabled
	0	NMI- Disabled

00A1-00A7 Reserved

00A8-00AF Not Used

Address	Description							
00C0-00C3	Sound SN76496							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
1	0	0	0	F6	F7	F8	F9	Update Tone Frequency 1
0	X	F0	F1	F2	F3	F4	F5	Additional Frequency Data
1	0	0	1	A0	A1	A2	A3	Update Tone Attenuation 1
1	0	1	0	F6	F7	F8	F9	Update Tone Frequency 2
0	X	F0	F1	F2	F3	F4	F5	Additional Frequency Data
1	0	1	1	A0	A1	A2	A3	Update Tone Attenuation 2
1	1	0	0	F6	F7	F8	F9	Update Tone Frequency 3
0	X	F0	F1	F2	F3	F4	F5	Additional Frequency Data
1	1	0	1	A0	A1	A2	A3	Update Tone Attenuation 3
1	1	1	0	X	FB	NF0	NF1	Update Noise Control
1	1	1	1	A0	A1	A2	A3	Update Noise Attenuation

Address	Description
00C4-00C7	DAC Functions
00C4	Write

Bits 0-1

Bit 0	Bit 1	DAC Function Selected
0	0	Joystick
0	1	Successive Approximation
1	0	Sound Channel
1	1	Direct Write to DAC

Bit 2 DMA Enable (for SA, Direct R/W)

0	DMA Disabled
1	DMA Enabled for SA, DA

Bit 3 DMA Interrupt Clear

0	DMA Interrupt Held Clear
1	DMA Interrupt Allowed

Bit 4 DMA Interrupt Enable

0	DMA EOP Interrupt Disabled
1	DMA EOP Interrupt Enabled

Bit 5 Sound Divider Sync Enable

0	Synchronization Disabled
1	Sync Enabled (Write to 00C6 or 00C7 reloads all dividers)

Bit 6 Sound Chip Extra Divide Enable

0	Extra Divide Disabled
1	Extra Divide Enabled

Bit 7 Reserved

00C4 Read

Bit 3 DMA Interrupt Flag. A DMA Interrupt has occurred. To clear the interrupt flag, Bit 3 must be brought low and then high again.

Bit 7 Successive Approximation Done. Useful when polling instead of using DMA.

Address	Description

00C5 Write

Bits 0-2

Bit 0	Bit 1	Bit 2	Duty Cycle
0	0	0	6.25%
0	0	1	12.5%
0	1	0	18.75%
0	1	1	25.0%
1	0	0	31.25%
1	0	1	37.5%
1	1	0	43.75%
1	1	1	50.0%

Bit 3 Reserved

Bit 4 Reserved

Bit 5 Reserved

Bits 6-7 Waveshape Select

Bit 7	Bit 6	Waveshape Selected
0	0	Pulse
0	1	Ramp
1	0	Triangle
1	1	Reserved

00C5 Read

Direct Read of DAC when 00C4 Bits 0-1 = 1X
Direct Read of Control Register when 00C4 Bits 0-1 = 01

00C6 R/W Frequency lsb for DAC sound channel

Bit 0	F0
Bit 1	F1
Bit 2	F2
Bit 3	F3
Bit 4	F4
Bit 5	F5
Bit 6	F6
Bit 7	F7

Address	Description
00C7	R/W Amplitude/frequency msb for DAC sound channel

Bit 0	F8
Bit 1	F9
Bit 2	F10
Bit 3	F11
Bit 4	Reserved
Bit 5	AMP 1
Bit 6	AMP 2
Bit 7	AMP 3

00C8-00CF Reserved

0100-01FF Reserved

0200-0207 Joystick

Write Clear (Resets Ramp Generator To 0)

0201 Read R = Right Joystick, L = Left Joystick

Bit	Description
0	R - X Horizontal Position
1	R - Y Vertical Position
2	L - X Horizontal Position
3	L - Y Vertical Position
4	R Button #1 (Logic 0 = Button Pressed)
5	R Button #2 (Logic 0 = Button Pressed)
6	L Button #1 (Logic 0 = Button Pressed)
7	L Button #2 (Logic 0 = Button Pressed)

0208-020F Not Used

0210-02F7 Reserved

2F8-2FF Serial Port Secondary (COM2 Optional)

02F8 Write Transmitter Holding Register (Character to send)

Bit	Description
0	Bit 0 - LSB (First Bit Sent Serially)
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7 - MSB

Address	Description

02F8 Read Receiver Buffer Register (Character Received)

Bit	Description
0	Bit 0 - LSB (First Bit Received Serially)
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7 - MSB

02F8 Divisor Latch LSB (Divisor Latch Access Bit DLAB ="1")

Bit	Description
0	Bit 0
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7

02F9 Divisor Latch MSB (Divisor Latch Access Bit DLAB ="1")

Bit	Description
0	Bit 0
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7

02F9 Interrupt Enable Register

Bit	Description
0	"1" = Enables the Received Data Available Interrupt
1	"1" = Enables the Transmitter Holding Register Int
2	"1" = Enables Receive Line Status Interrupt
3	"1" = Enables the Modem Status Interrupt
4-7	Always Logical "0"

Address	Description
02FA	Interrupt Identification Register

Bit	Description
0	"0" = Interrupt Pending
1-2	Bit 2 / Bit 1 "0" / "0" Fourth Level Priority "0" / "1" Third Level Priority "1" / "0" Second Level Priority "1" / "1" Highest Level Priority
3-7	Always Logical "0"

02FB Line Control Register

Bit	Description
0-1	Bit 1 / Bit 0 "0" / "0" Five Bit Word Length "0" / "1" Six Bit Word Length "1" / "0" Seven Bit Word Length "1" / "1" Eight Bit Word Length
2	"0" = One Stop Bit "1" = 1½ Stop Bits When Five Bit Length Selected Two Stop Bits With Six, Seven, or Eight Bit
3	"1" = Parity Enable
4	"0" = Odd Parity Select "1" = Even Parity Select
5	Stick Parity Bit
6	"1" = Set Break Enable
7	"1" = Divisor Latch Access Bit Enable

02FC

Bit	Description
0	"1" = Data Terminal Ready Set (DTR) "0" = Data Terminal Ready Reset (DTR)
1	Request To Send (RTS)
2	Out 1
3	Out 2
4	Loop
5-7	Always Logical "0"

Address	Description
02FD	Line Status Register

Bit	Description
0	Data Ready (DR)
1	Overrun Error (OR)
2	"1" = Detect Parity Error (PE)
3	"1" = Detect Framing Error (FE)
4	"1" = Break Interrupt (BI)
5	Transmitter Holding Register "1" = Character Transferred From Holding To Shift Register "0" = Loading Transmitter Holding Register
6	Transmitter Shift Register Empty "1" = Shift Register Idle "0" = Data Transfer From Holding Register
7	Always Logical "0"

02FE Modem Status Register

Bit	Description
0	Delta Clear To Send (DCTS)
1	Delta Data Set Ready (DDSR)
2	Trailing Edge Ring Indicator "1" = On "0" = Off
3	Delta Received Line Signal Detect (If Bit 0, 1, 2, or 3 is set to a "1", modem status interrupt is generated)
4	"0" = Clear To Send (CTS)
5	"0" = Data Set Ready (DSR)
6	"0" = Ring Indicator (RI)
7	"0" = Received Line Signal Detect (RLSD)

02FF Reserved

0300-036F Reserved

0370-0377 Floppy Disk Controller 2 (optional)

Address	Description
0378	Printer - Data Latch

Bit	Description
0	Bit 0 - LSB
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7 - MSB

0379 Printer - Read Status

Bit	Description
0	Not Used
1	Not Used
2	Not Used
3	"0" = Error
4	"1" = Printer Select
5	"0" = Out of Paper
6	"0" = Acknowledge
7	"0" = Busy

037A (037E) Printer - Control Latch

Bit	Description
0	"0" = Strobe
1	"0" = Auto FD XT
2	"0" = Initialize
3	"0" = Select Printer
4	"1" = Enable Interrupt
5	"0" = Enable Output Data
6	Not Used
7	Not Used

037B Not Used

037C Printer - Data Latch

037D Printer - Read Status

037F-03CF Not Used

03D0-03D3 Not Used

03D4 6845 Address Register

Address	Description
03D5	6845 Data Register
03D6	Not Used
03D7	Not Used
03D8	Mode Select Register

Bit 0 High Resolution Clock
= 0 Selects 40 By 25 Alphanumeric Mode
= 1 Selects 80 By 25 Alphanumeric Mode
Bit 1 Graphics Select
= 0 Selects Alphanumeric Mode
= 1 Selects 320 By 200 Graphics Mode
Bit 2 Black And White
= 0 Selects Color Mode
= 1 Selects Black And White Mode
Bit 3 Video Enable
= 0 Disables Video Signal
= 1 Enables Video Signal
Bit 4 640 Dot Graphics
= 0 Disables 640 By 200 B&W Graphics Mode
= 1 Enables 640 By 200 B&W Graphics Mode
Bit 5 Blink Enable
= 0 Disables Blinking
= 1 Enables Blinking

03D9 Color Select Register

Bit 0 Background Blue
Bit 1 Background Green
Bit 2 Background Red
Bit 3 Background Intensity
Bit 4 Foreground Intensity
Bit 5 Color Select

Address	Description

03DA-03DE Write Video Array Address and Read Status (03DA)
Write Video Array Data (03DE)

Read (03DA)		Write (03DE)
00 Bit 0	Display Inactive	Not Used
00 Bit 1	Light Pen Set	Not Used
00 Bit 2	Light Switch Status	Not Used
00 Bit 3	Vertical Retrace	Not Used
00 Bit 4	Not Used	Not Used
01 Bit 0		Palette Mask 0
01 Bit 1		Palette Mask 1
01 Bit 2		Palette Mask 2
01 Bit 3		Palette Mask 3
02 Bit 0		Border Blue
02 Bit 1		Border Green
02 Bit 2		Border Red
02 Bit 3		Border Intensity
02 Bit 5		Reserved = 0
03 Bit 0		Mono Enable = 1
03 Bit 1		Reserved = 0
03 Bit 2		Border Enable
03 Bit 3		4-Color High Resolution
03 Bit 4		16-Color Mode
03 Bit 5		Extra Video Mode

03DB Clear Light Pen Latch

03DC Preset Light Pen Latch

03DD Extended RAM Page Register - CPU Relative

Bit	Description
0	Extended Addressing Modes
1	Not Used
2	Not Used
3	CRT Video Page Address "17"
4	CRT Video Page Address "18"
5	CPU Page Address "17"
6	CPU Page Address "18"
7	Select 64K Or 256K RAM

Address	Description

03DF CRT Processor Page Register - Video Memory Relative

Bit 0	A14	CRT Page 0
Bit 1	A15	CRT Page 1
Bit 2	A16	CRT Page 2
Bit 3	A14	Processor Page 0
Bit 4	A15	Processor Page 1
Bit 5	A16	Processor Page 2
Bit 6	Video Address Mode 0	
Bit 7	Video Address Mode 1	

Video Descriptions	D0 3DDH	D7 3DFH	D6 3DFH
8p 1 - 16K	0	0	0
8p 2 - 8K	0	0	1
4p 2 - 16K	0	1	0
4p 4 - 8K	0	1	1
4p 1 - 32K	1	0	0
2p 2 - 32K	1	0	1

03E0-03EF Reserved

03F0 Not Used

03F1 Drive Select Switch

Bit 0	Not Used
Bit 1	"1" DS0 = DS0
	"0" DS0 = DS1
Bit 2	Not Used
Bit 3	Mux FDCDMATC (Write Only)
	"0" FDCDMATC Out
	"1" Input
Bit 4	Not Used
Bit 5	Not Used
Bit 6	Not Used
Bit 7	Not Used

03F2 DOR Register (Write Only)

Bits 0-1	Drive Select
Bit 1	Bit 0
0	0 Drive Select A*
0	1 Drive Select B*
Bit 2	0 = FDC Reset
Bit 3	1 = Enable DMA Request/Interrupt
Bit 4	1 = Drive A Motor On
Bit 5	1 = Drive B Motor On
Bit 6	1 = FDC Terminal Count
Bit 7	Not Used

Address	Description
03F3	Not Used
03F4	FDC - Status (Read Only) See FDC Specification
03F5	FDC - Data (R/W) See FDC Specification
03F6-03F7	Reserved
03F8-03FF	Serial Port Primary (COM1)
03F8	Write Transmitter Holding Register (Character to send)

Bit	Description
0	Bit 0 - LSB (First Bit Sent Serially)
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7 - MSB

03F8 Read Receiver Buffer Register (Character Received)

Bit	Description
0	Bit 0 - LSB (First Bit Received Serially)
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7 - MSB

03F8 Divisor Latch LSB (Divisor Latch Access Bit DLAB = "1")

Bit	Description
0	Bit 0
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7

Address	Description

03F9 Divisor Latch MSB (Divisor Latch Access Bit DLAB = "1")

Bit	Description
0	Bit 0
1	Bit 1
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7

03F9 Interrupt Enable Register

Bit	Description
0	"1" = Enables the Received Data Available Interrupt
1	"1" = Enables the Transmitter Holding Register Int
2	"1" = Enables Receive Line Status Interrupt
3	"1" = Enables the Modem Status Interrupt
4-7	Always Logical "0"

03FA Interrupt Identification Register

Bit	Description		
0	"0" = Interrupt Pending		
1-2	Bit 2	Bit 1	
	"0"	"0"	Fourth Level Priority
	"0"	"1"	Third Level Priority
	"1"	"0"	Second Level Priority
	"1"	"1"	Highest Level Priority
3-7	Always Logical "0"		

Address	Description
03FB	Line Control Register

Bit	Description
0-1	Bit 1 Bit 0 "0" "0" Five Bit Word Length "0" "1" Six Bit Word Length "1" "0" Seven Bit Word Length "1" "1" Eight Bit Word Length
2	"0" = One Stop Bit "1" = 1½ Stop Bits When Five Bit Length Selected Two Stop Bits With Six, Seven, or Eight Bit
3	"1" = Parity Enable
4	"0" = Odd Parity Select "1" = Even Parity Select
5	Stick Parity Bit
6	"1" = Set Break Enable
7	"1" = Divisor Latch Access Bit Enable

03FC

Bit	Description
0	"1" = Data Terminal Ready Set (DTR) "0" = Data Terminal Ready Reset (DTR)
1	Request To Send (RTS)
2	Out 1
3	Out 2
4	Loop
5-7	Always Logical "0"

03FD Line Status Register

Bit	Description
0	Data Ready (DR)
1	Overrun Error (OR)
2	"1" = Detect Parity Error (PE)
3	"1" = Detect Framing Error (FE)
4	"1" = Break Interrupt (BI)
5	Transmitter Holding Register "1" = Character Transferred From Holding To Shift Register "0" = Loading Transmitter Holding Register
6	Transmitter Shift Register Empty "1" = Shift Register Idle "0" = Data Transfer From Holding Register
7	Always Logical "0"

Address	Description
03FE	Modem Status Register

Bit	Description
0	Delta Clear To Send (DCTS)
1	Delta Data Set Ready (DDSR)
2	Trailing Edge Ring Indicator "1" = On "0" = Off
3	Delta Received Line Signal Detect (If Bit 0, 1, 2, or 3 is set to a "1", modem status interrupt is generated)
4	"0" = Clear To Send (CTS)
5	"0" = Data Set Ready (DSR)
6	"0" = Ring Indicator (RI)
7	"0" = Received Line Signal Detect (RLSD)

03FF	Reserved

Address	Description
FFE8-FFEB	System Control Registers
FFE8	Video Configuration Register

Bit Description

0 Reserved

Bit 1-4 Video Memory Configuration

Bit 4 256K Enable	Bit 3 A19	Bit 2 A18	Bit 1 A17	Memory Start	Memory Length	Memory Range
0	0	0	0	0 0000	128K	0 0000-1 FFFF
0	0	0	1	2 0000	128K	2 0000-3 FFFF
0	0	1	0	4 0000	128K	4 0000-5 FFFF
0	0	1	1	6 0000	128K	6 0000-7 FFFF
0	1	0	0	8 0000	128K	8 0000-9 FFFF
0	1	1	1	B 0000	128K	B 0000-B FFFF (4 Page)
1	0	0	1	0 0000	256K	0 0000-3 FFFF
1	0	1	0	2 0000	256K	2 0000-5 FFFF
1	0	1	1	4 0000	256K	4 0000-7 FFFF
1	1	0	0	6 0000	256K	6 0000-9 FFFF
1	1	1	1	B 8000	256K	B 0000-B FFFF (8 Page)

NOTE: To turn off on-board Video, be sure Port A0H, Data Bit 0 is a "1" and Video Array Register 3.

5 16 Bit CPU Memory = 1
6 Reserved
7 Reserved

Address	Description

FFE9 Programmable Wait State Port

Bit(s)	Description
0	Internal Memory Wait States 0 = 0 wait states 1 = 1 wait states
1,2	External Memory Wait States 00 = 0 wait states 01 = 1 wait states 10 = 2 wait states 11 = 3 wait states
3,4	I/O Cycle Wait States 00 = 0 wait states 01 = 1 wait states 10 = 2 wait states 11 = 3 wait states
5	DMA Early Write Disable 0 = DMA waits for IOCHRDY = 1 to start Write Strobe 1 = Normal 8237A-5 Write Strobe Generation
6	Internal Video Wait States 0 = 0 wait states 1 = 1 wait states
7	OSCIN Select 0 = 28.63636 MHz 1 = 24 MHz

FFEA WRITE/READ

Bit 0: ROM PAGING 0
Bit 1: ROM PAGING 1
Bit 2: ROM PAGING 2
Bit 3: ROM PAGING 3
Bit 4: ROM PAGING 4
Bit 5: 0 = Internal and Bus Refresh
1 = Internal Refresh only

Bit 6-7	Bit 7	Bit 6	
	0	0	Two Banks of 128K memory
	0	1	Four Banks of 128K memory
	1	0	One Bank of 512K memory
	1	1	One Bank of 512K memory, One Bank of 128K memory

NOTE: When reading Port FFEA, Bit 4 will be inverted from what was written, (i.e. when a 0 is written, a 1 will be read; when a 1 is written, a 0 will be read.)

ROM Paging Definition:

Two 2 Meg ROMs (Two 1 Meg ROMs)	ADDRESS 19	18	17	16	ROM PAGES 4	3	2	1	0	ROMCS #0	#1	SELECT 2	1	0	64K Page ROM 0	ROM 1
F0000-FFFFF	1	1	1	1	x	x	x	x	x	0	1	x	1	1	1	
E0000-EFFFF	1	1	1	0	1	x	1	1	1	1	1	x	x	x		
E0000-EFFFF	1	1	1	0	1	x	1	1	0	0	1	x	1	0	2	
E0000-EFFFF	1	1	1	0	1	x	1	0	1	0	1	x	x	1	3	
E0000-EFFFF	1	1	1	0	1	x	1	0	0	0	1	x	0	0	4	
E0000-EFFFF	1	1	1	0	1	x	0	1	1	1	0	x	1	1		1
E0000-EFFFF	1	1	1	0	1	x	0	1	0	1	0	x	1	0		2
E0000-EFFFF	1	1	1	0	1	x	0	0	1	1	0	x	0	1		3
E0000-EFFFF	1	1	1	0	1	x	0	0	0	1	0	x	0	0		4

Two 4 Meg ROMs	19	18	17	16	4	3	2	1	0	#0	#1	2	1	0	ROM 0	ROM 1
F0000-FFFFF	1	1	1	1	x	x	x	x	x	0	1	1	1	1	1	
E0000-EFFFF	1	1	1	0	0	1	1	1	1	1	1	x	x	x		
E0000-EFFFF	1	1	1	0	0	1	1	1	0	0	1	1	1	0	2	
E0000-EFFFF	1	1	1	0	0	1	1	0	1	0	1	1	0	1	3	
E0000-EFFFF	1	1	1	0	0	1	1	0	0	0	1	1	0	0	4	
E0000-EFFFF	1	1	1	0	0	1	0	1	1	0	1	0	1	1	5	
E0000-EFFFF	1	1	1	0	0	1	0	1	0	0	1	0	1	0	6	
E0000-EFFFF	1	1	1	0	0	1	0	0	1	0	1	0	0	1	7	
E0000-EFFFF	1	1	1	0	0	1	0	0	0	0	1	0	0	0	8	
E0000-EFFFF	1	1	1	0	0	0	1	1	1	1	0	1	1	1		1
E0000-EFFFF	1	1	1	0	0	0	1	1	0	1	0	1	1	0		2
E0000-EFFFF	1	1	1	0	0	0	1	0	1	1	0	1	0	1		3
E0000-EFFFF	1	1	1	0	0	0	1	0	0	1	0	1	0	0		4
E0000-EFFFF	1	1	1	0	0	0	0	1	1	1	0	0	1	1		5
E0000-EFFFF	1	1	1	0	0	0	0	1	0	1	0	0	1	0		6
E0000-EFFFF	1	1	1	0	0	0	0	0	1	1	0	0	0	1		7
E0000-EFFFF	1	1	1	0	0	0	0	0	0	1	0	0	0	0		8

FFEB UART Clock, Joystick, and Sound Enable

Bit	Description
0	0 = Clock divided by 13 1 = Clock Divided by 1
1	0 = Disable Joystick 1 = Enable Joystick
2	0 = Disable Sound Chip 1 = Enable Sound Chip

ELECTRICAL BILL OF MATERIAL - TANDY 1000 SL

MAIN LOGIC ASSY. TANDY 1000 SL

QTY.	DESCRIPTION	DESIGNATOR	VENDOR	PART NUMBER
1	TANDY 1000 SL MAIN LOGIC PCB REV. B			8709843
4	STAKE PIN	E2-4	AMP#1-87022-0	8529014
1	SOCKET, 8-PIN DIP	U17	AMP#640463-1	8509011
20	SOCKET, 18 PIN DIP	U6-11,15,16, 19,20,23,24 27,28,31,32, 34,35,36,37	AMP#2-383060-3	8509037
1	SOCKET, 20 PIN DIP	U13B		8509009
1	SOCKET, 24 PIN .300	U18	AMP#640962-3	8509029
2	SOCKET, 28 PIN DIP	U13,25	AMP#2-641605-3	8509007
2	SOCKET, 32 PIN	HU1,HU2 OR SU3,SU4		8509048
3	SOCKET, 40 PIN DIP	U12,21,29	AMP#2-641606-3	8509002
2	SOCKET, 68 PIN PLCC	U30,40		8509020
1	CONNECTOR, 9-PIN	J3 (POWER)	MOLEX#26-48-1095	8519191
1	CONNECTOR, 34 PIN	J2 (FLOPPY)	MOLEX#70246-3402	8519324
5	CONNECTOR, 62 PIN	J5-9		8519236
1	CONNECTOR, DB9	J10 (SERIAL)	AMP#747840-3	8519269
1	CONNECTOR, DB9	J11 (VIDEO)	AMP#7459883 HOLMBERG#4509RA28CM42 MOLEX#82009-2052	8519279
1	CONNECTOR, 8 PIN	J1	AMP#5-102074-8 BERG#65001-208 MOLEX#90148-1108	8519365
1	CONNECTOR, 20 PIN	J4 (JOYSTK)	AMP#5-102083-6 MOLEX#15-38-2020 BERG#65000-210	8519366
6	RESISTOR, 10 OHM 1/8W 5% SMD R1206	R11,14,16,22, 24,27		X20301030
7	RESISTOR, 33 OHM 1/8W 5% SMD R1206	R2,3,18,34, 35,36,37		X20303330
1	RESISTOR, 510 OHM 1/8W 5% SMD R1206	R41		X20315130
6	RESISTOR, 1K OHM 1/8W 5% SMD R1206	R1A,20,21,23, 25,39		X20321030
1	RESISTOR, 1.2K OHM 1/8W 5% SMD R1206	R42		X20321230
1	RESISTOR, 2.2K OHM 18W 5% SMD R1206	R29		X20322230
1	RESISTOR, 3.3K OHM 18W 5% SMD R1206	R28		X20323330

ELECTRICAL BILL OF MATERIAL - TANDY 1000 SL

MAIN LOGIC ASSY. TANDY 1000 SL

QTY.	DESCRIPTION	DESIGNATOR	VENDOR	PART NUMBER
5	RESISTOR, 4.7K OHM 1/8W 5% SMD R1206	R1,4,5,17,33		X20324730
10	RESISTOR, 10K OHM 1/8W 5% SMD R1206	R6,7,8,9, 10,12,13,15, 18A,19		X20331030
5	RESISTOR, 27K OHM 1/8W 5% SMD R1206	R26,31,38,40,46		X20332730
2	RESISTOR, 47K OHM 1/8W 5% SMD R1206	R30,45		X20334730
2	RESISTOR, 100K OHM 1/8W 5% SMD R1206	R43,44		X20341030
1	RES PAK, 1K,	RP3		8290210
1	RES PAK, 4.7K	RP8		8294247
1	RES PAK, 10K	RP4		8290032
1	RES PAK, 10K	RP7		8292310
7	RES PAK, 33 OHM,	RP1,2,5,6, 9-11		8290044
36	CAP 0.1uf 50V 20% SMD C0805	C2-4,6,9, 10,10A,15A, 18,19,21,22, 28,31,35-37, 39,47,69, 70-72,74-79, 82,84,87,91, 102,111,126		X30410345
20	CAP 0.33 uf 50V 20% Z5U SMD C1210	C7,8,11,12, 13,14,16,17, 20,23,25,26, 29,30,32,33, 40,41,51,52		X30433343
4	CAP 10 uf 25V TANT RAD. 20%	C5,15,27,68		8336106
2	CAP 10 uf 16V ELECT.RAD. 20%	C81,86		8326106
6	CAP 22 uf 16V ELECT.RAD. 20%	C1,44-46,83,127		8326221
2	CAP 22 UF 25V ELECT.RAD. 20%	C42,43		8326224
1	CAP 47 uf 16V ELECT.RAD. 20%	C101		8326474
6	CAP 33 pf 10% 50V SMD C0805	C24,34,38,50, 73,80		X30033240

ELECTRICAL BILL OF MATERIAL - TANDY 1000 SL

MAIN LOGIC ASSY. TANDY 1000 SL

QTY.	DESCRIPTION	DESIGNATOR	VENDOR	PART NUMBER
49	CAP 220 pf 10% 50V SMD C0805	C48,49,53-67, 85,88-90, 92-99,100 103,105,106, 109,110, 112-125		X30122243
3	CAP 330 pf SMD C0805	C104,107,108		X30133244
1	OSCILLATOR, DUAL 28/32 MHZ	Y1	DIAWA, MF	8409076
1	OSCILLATOR, DUAL 16/24 MHZ	Y2	DIAWA, MF	8409075
2	IC, 74HCT14*	U33	GENERIC	8026014
1	IC, 74HCT273	U14	"	8026273
1	IC, 74LS00	U5	"	8020000
1	IC, 74LS32	U22	"	8020032
1	IC, 74LS175	U13A	"	8020175
1	IC, 74LS244	U45	MOTOROLA	8020244
1	IC, 74LS373	U38	GENERIC	8020373
1	IC, MC1458S	U44	"	8052458
1	IC, MC1488	U39	"	8050188
2	IC, MC1489	U42,43	"	8050189
1	IC, VIDEO II	U26		8079020
1	IC, BUFFER BLUE	U41		8079024
10	FERRITE BEAD	FB1-10	FAIRRITE#2743002121	8419013
1	VOLT.REG. 78L05	VR1	MOTOROLA MC78L05, FAIRCHILD UA78L05 TEXAS INST. UA78L05C	8052805
1	VOLT.REG. 79M05CT	VR2	MOTOROLA MC79M05CT, FAIRCHILD UA7905 TEXAS INST. UA79M05CKC	8190005
5	EMI FILTER, .22 uf W/FER. BEAD	CF1-5	MURATA#DTS310 55D-2235	8418013
1	1N4148 DIODE	CR1		8150148

* (CAN SUB LS FOR ALL HCT PARTS)
NOTE: DO NOT STUFF R32,E5,E6,E7,R1B.

TANDY 1000 SL FINAL ASSEMBLY

QTY.	DESCRIPTION	DESIGNATOR	VENDOR	PART NUMBER
1	TANDY 1000 SL SUBASSEMBLY REV. B			8859024
1	JUMPER PLUG	E2-E3	GENERIC	8519098
1	IC, EEPROM, 1K SERIAL	U17	NAT. SEMI CONDUCTOR, HYUNDAI, AMI	8040346
1	IC, 16K X 8 ROM (CHAR GEN) 200NS	U25	HITACHI, SHARP, NCR	8079027
4	IC, 64K X 4 DRAM 120 ns	U6,7,8,9	FUJITSU, HITACHI, NEC, TI, SAMSUNG, MICRON	8045164
8	IC, 64K X 4 DRAM 150 ns	U10,15,19,23, 27,31,34,36,	GENERIC	8040464
1	IC, VIDEO II	U26		8079020
1	IC, CPU 8086-2	U29	AMD	8041086
1	IC, BUFFER BLUE	U41		8079024
1	IC, PSSJ (68 PLCC)	U40		8079021
1	IC, FDSL	U18		8041401
1	IC, KFIT (68 PLCC)	U30		8079019
1	IC, UPD 765A	U12	INTEL, ROCKWELL, ZILOG, NEC	8040272
1	IC, 256K X 8 (2MEG BIT ROM) EVEN (200NS) *	HU1	HITACHI	8076312
1	IC, 256K X 8 (2MEG BIT ROM) ODD (200NS) *	HU2	HITACHI	8075312
1	IC, 256K X 8 (2MEG BIT ROM) EVEN (200NS) *	SU3	SHARP	8076323
1	IC, 256K X 8 (2MEG BIT ROM) ODD (200NS) *	SU4	SHARP	8075323
1	IC, PAL 16R4A	U13B	AMD, NAT. SEMI CONDUCTOR	8042164

* NOTE: USE EITHER HITACHI ROMS (HU1,HU2) OR SHARP ROMS (SU3,SU4), BUT NOT BOTH SETS.

ELECTRICAL BILL OF MATERIAL - TANDY 1000 SL

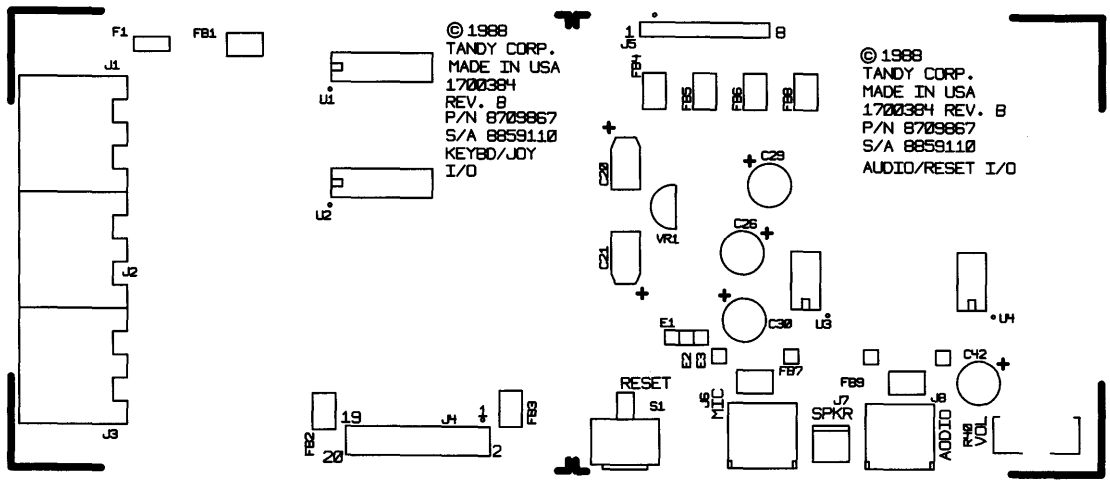
TANDY 1000 SL SUBASSEMBLY 8859110

QTY.	DESCRIPTION	DESIGNATOR	VENDOR	PART NUMBER
1	TANDY 1000 SL SATELLITE PCB REV. B			8709867
3	STAKING PIN	E1-3	AMP#1-87022-0	8529014
1	JUMPER PLUG	E2-E3		8519098
1	CONNECTOR	J7 (SPEAKER)	MOLEX#22-29-2021	8519193
1	CONNECTOR	J1 (KEYBOARD)	HOSIDEN#TCS5040-17-4071	8519358
2	CONNECTOR	J2,3 (JOYSTICK)	HOSIDEN#TCS5040-16-1911	8519318
1	CONNECTOR	J5	AMP#103323-8 MOLEX#22-59-1108 BERG#68015-408	8519367
1	CONNECTOR	J4	AMP#1-103324-0 MOLEX#10-88-1206 BERG#6805-420	8519368
1	RESISTOR, 47 OHM 1/8W 5% SMD R1206	R26		X20304730
1	RESISTOR, 10 OHM 1/8W 5% SMD R1206	R39		X20301030
9	RESISTOR, 33 OHM 1/8W 5% SMD R1206	R1-9		X20303330
4	RESISTOR, 1K OHM 1/8W 5% SMD R1206	R14,17,21,23,		X20321030
3	RESISTOR, 1.2K OHM 1/8W 5% SMD R1206	R29,32,34		X20321230
1	RESISTOR, 1.3K OHM 1/8W 5% SMD R1206	R30		X20321330
1	RESISTOR, 2.4K OHM 1/8W 5% SMD R1206	R27		X20322430
1	RESISTOR, 2.7K OHM 1/8W 5% SMD R1206	R36		X20322730
1	RESISTOR, 4.7K OHM 1/8W 5% SMD R1206	R33		X20324730
8	RESISTOR, 10K OHM 1/8W 5% SMD R1206	R10,13,18,19, 20,22,24,25		X20331030
2	RESISTOR, 13K OHM 1/8W 5% SMD R1206	R28,R35		X20331330
1	RESISTOR, 91K OHM 1/8W 5% SMD R1206	R31		X20339130
1	RESISTOR, 300 OHM 1/8W 5% SMD R1206	R37,38		X20313030
4	RESISTOR, 1 MEG 1/8W 5% SMD R1206	R11,12,15,16		X20361030
7	CAP 0.1 uf 50V 20% SMD C0805	C23,33,36,38-41		X37410341
3	CAP .33 uF	C35,43,44		X30433343
1	CAP .047 uF C1206P 20% 50V Z5U	C24		X30347343
3	CAP 3.3 uF	C26,29,30		X3335332

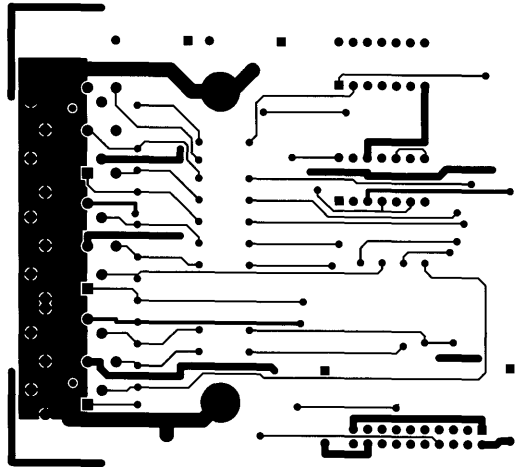
ELECTRICAL BILL OF MATERIAL - TANDY 1000 SL

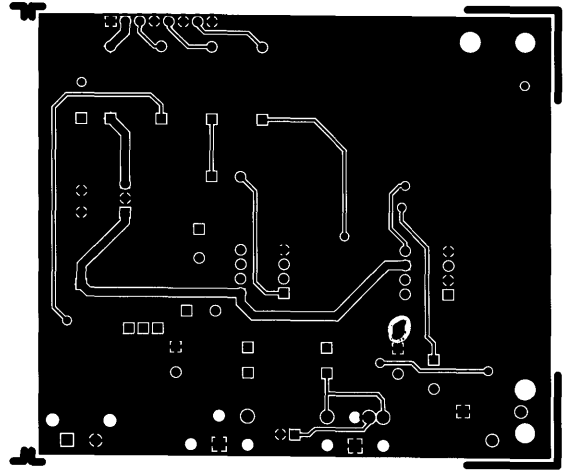
TANDY 1000 SL SUBASSEMBLY 8859110

QTY.	DESCRIPTION	DESIGNATOR	VENDOR	PART NUMBER
2	CAP 10 uf 20V 10% TANT. AX.	C20,21		8336103
1	CAP 100 uf ELECT.RAD. 20%	C42		8327108BAA
2	CAP 1000 pf 10% 50V XR7 SMD C0805	C27,34		X30210343
25	CAP 220 pf 50V 20% SMD C0805	C1-19,28,31, 22,25,32,37		X30122243
1	IC, 7416	U1	GENERIC	8000016
1	IC, MC1458	U3		8051458
1	IC, LM339	U2		8050339
1	IC, LM386	U4		8050386
9	FERRITE BEAD	FB1-9	FAIRRITE#2743002121	8419013
1	VOLT.REG. 78L05	VR1	MOTOROLA MC78L05, FAIRCHILD UA78L05 TEXAS INST. UA78L05C	8052805
1	RESET BUTTON	S1	ALPS#KHC15901	8489065
1	MINI PHONE JACK	J6	HSJ0862-01-1060	8519355
1	PHONO JACK	J8	HSJ0842-01-1020	8519322
1	POT. 10K	R40	PT15N#510KA	8270510

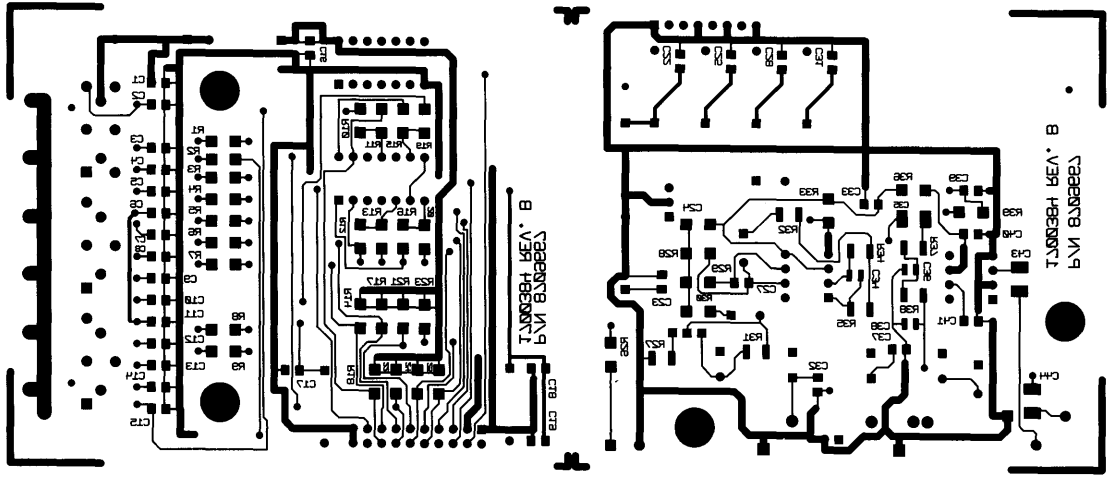


1700384 REV. B
7/22/88
LAYER SILKSCREEN



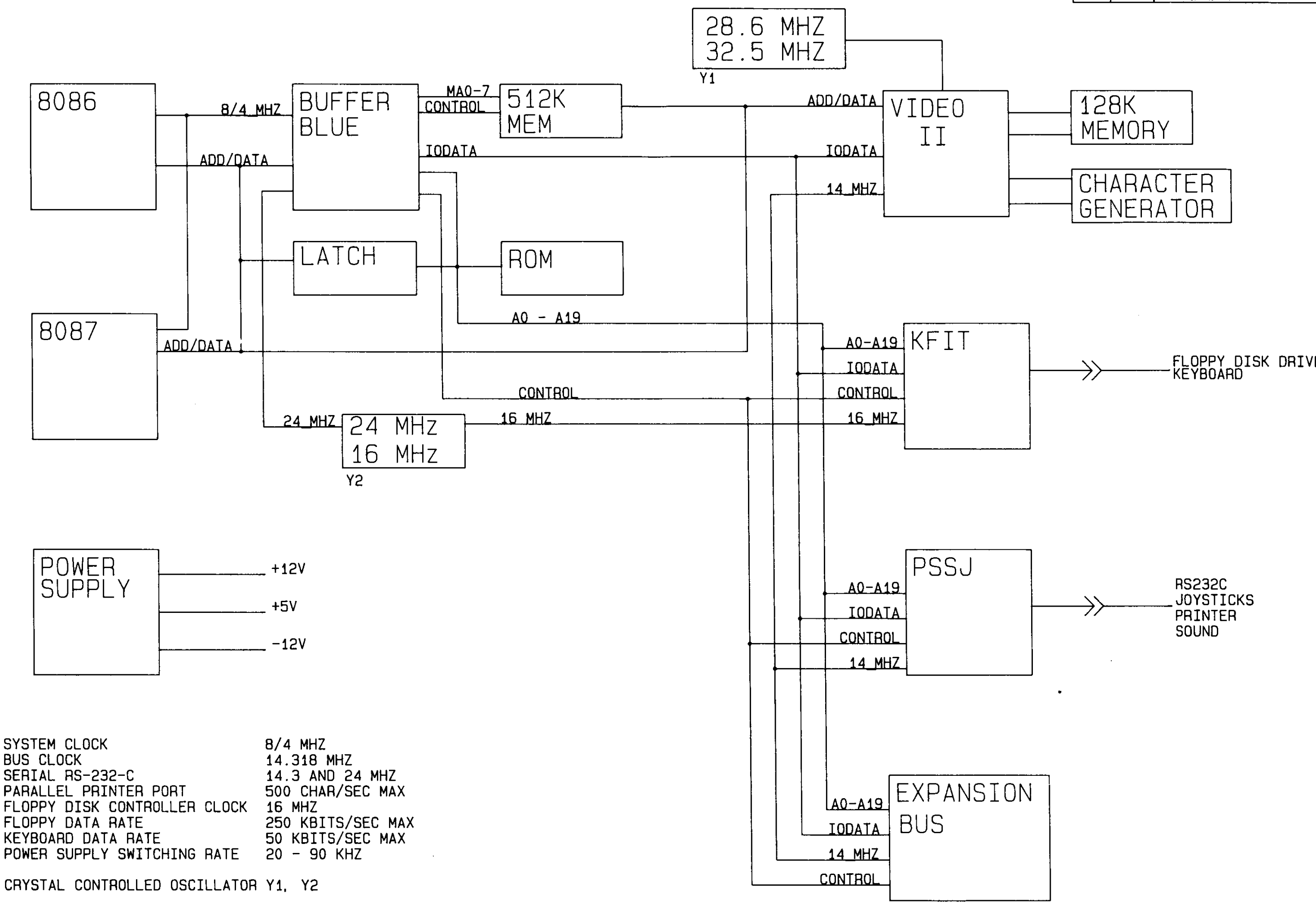


1700384 REV. B
7/22/88
LAYER 1 TOP SIDE



1700384 REV. B
7/22/88
LAYER 2 BOTTOM SIDE

ZONE	LETTER	DESCRIPTION	DATE	APPROVED
-	A	RELEASED_FOR_PRODUCTION	07/25/88	
-	B	CHANGED_PER_TCO_#13654	08/04/88	



SYSTEM CLOCK	8/4 MHZ
BUS CLOCK	14.318 MHZ
SERIAL RS-232-C	14.3 AND 24 MHZ
PARALLEL PRINTER PORT	500 CHAR/SEC MAX
FLOPPY DISK CONTROLLER CLOCK	16 MHZ
FLOPPY DATA RATE	250 KBITS/SEC MAX
KEYBOARD DATA RATE	50 KBITS/SEC MAX
POWER SUPPLY SWITCHING RATE	20 - 90 KHZ

CRYSTAL CONTROLLED OSCILLATOR Y1, Y2

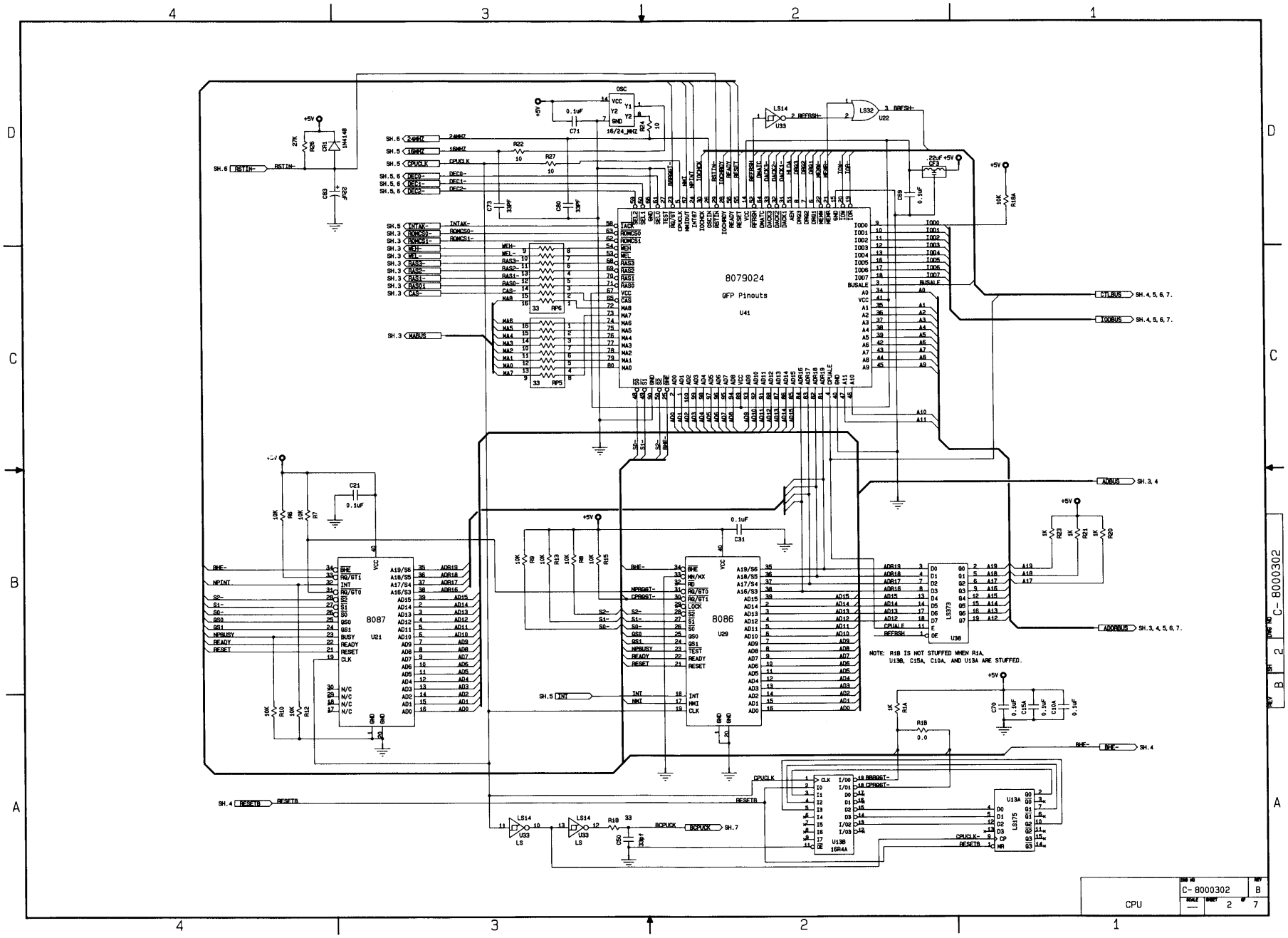
SCHEMATIC-
MAIN_LOGIC_BOARD

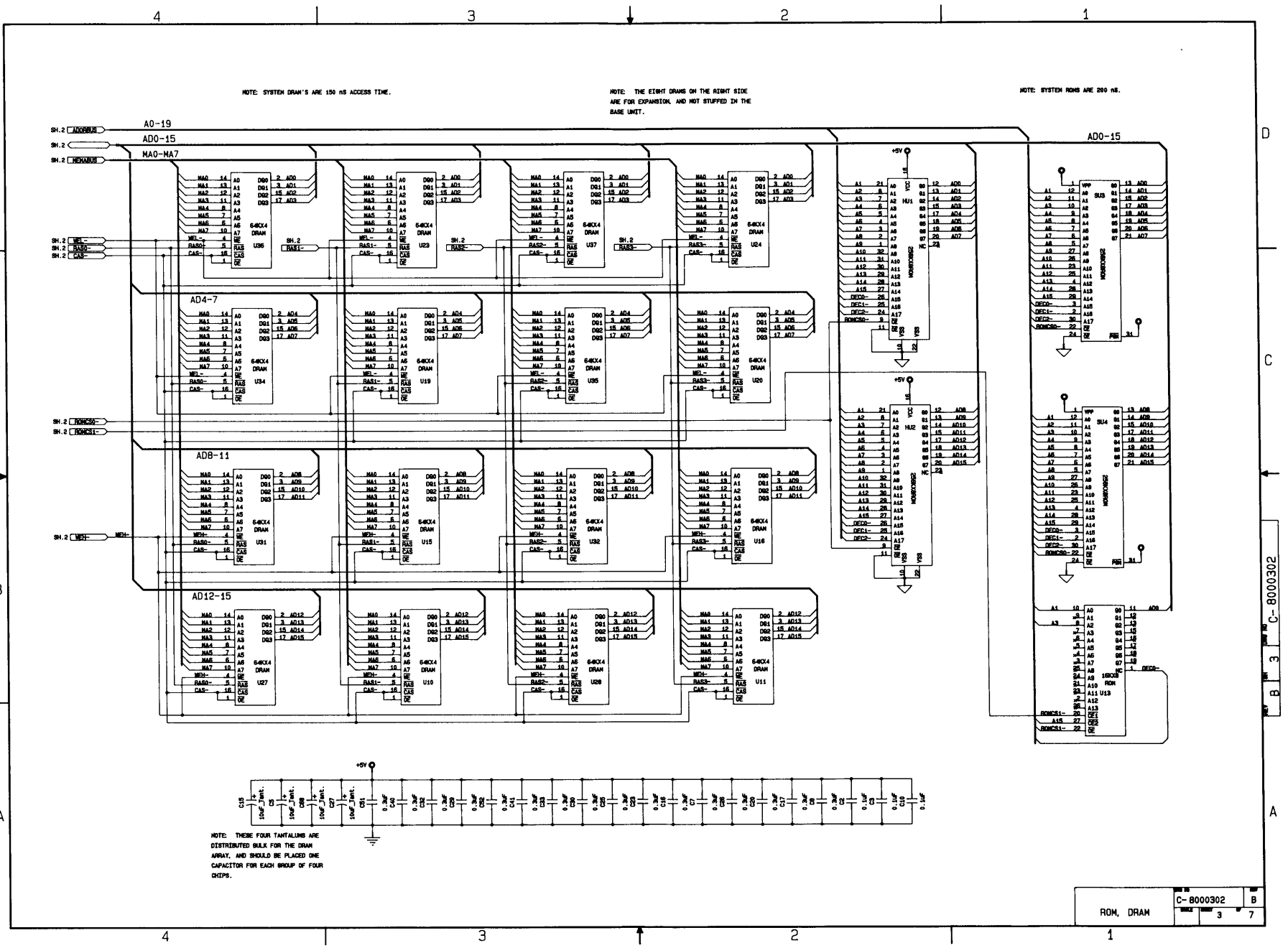
TANDY

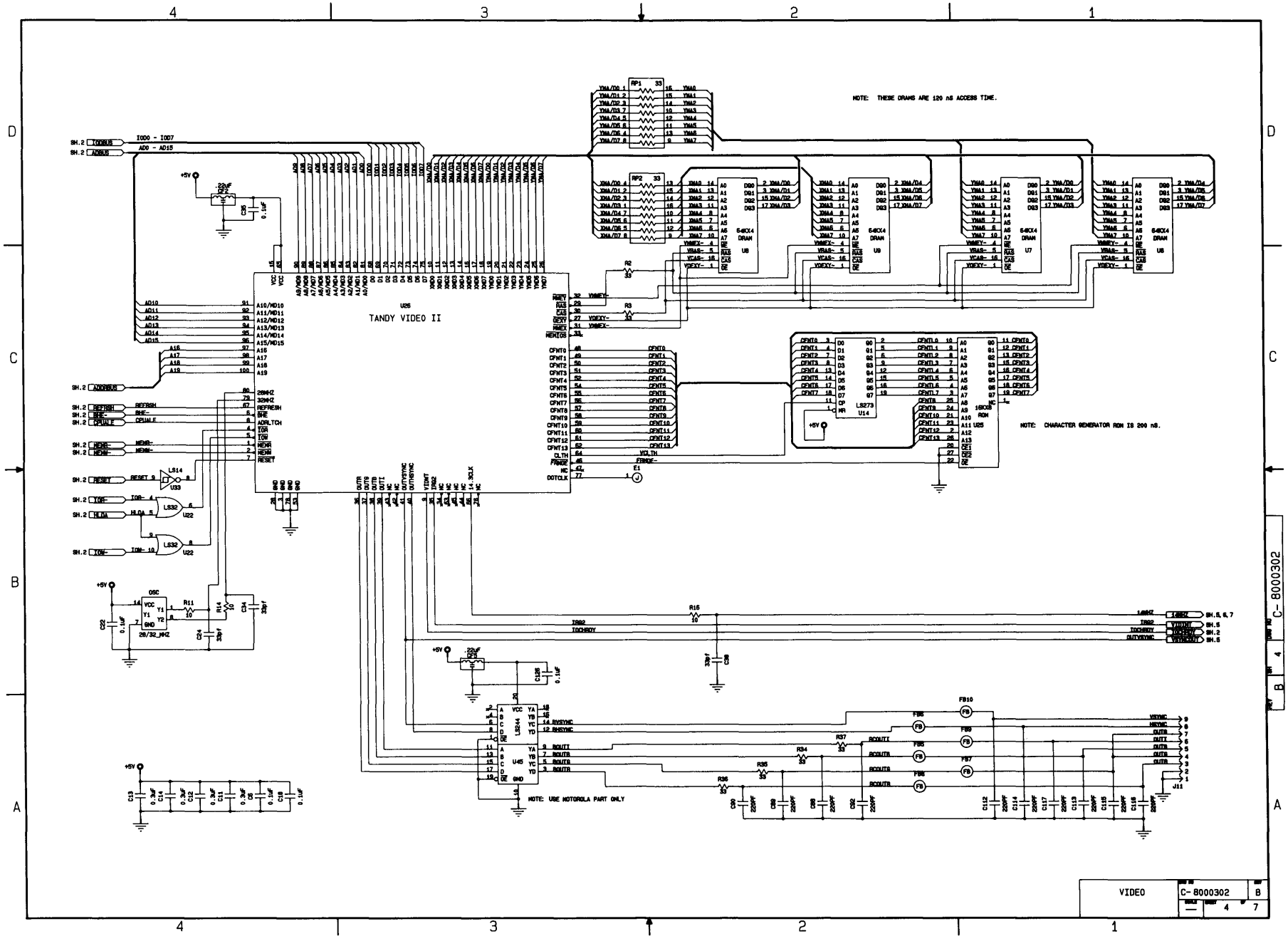
DWG NO C- 8000302 REV B

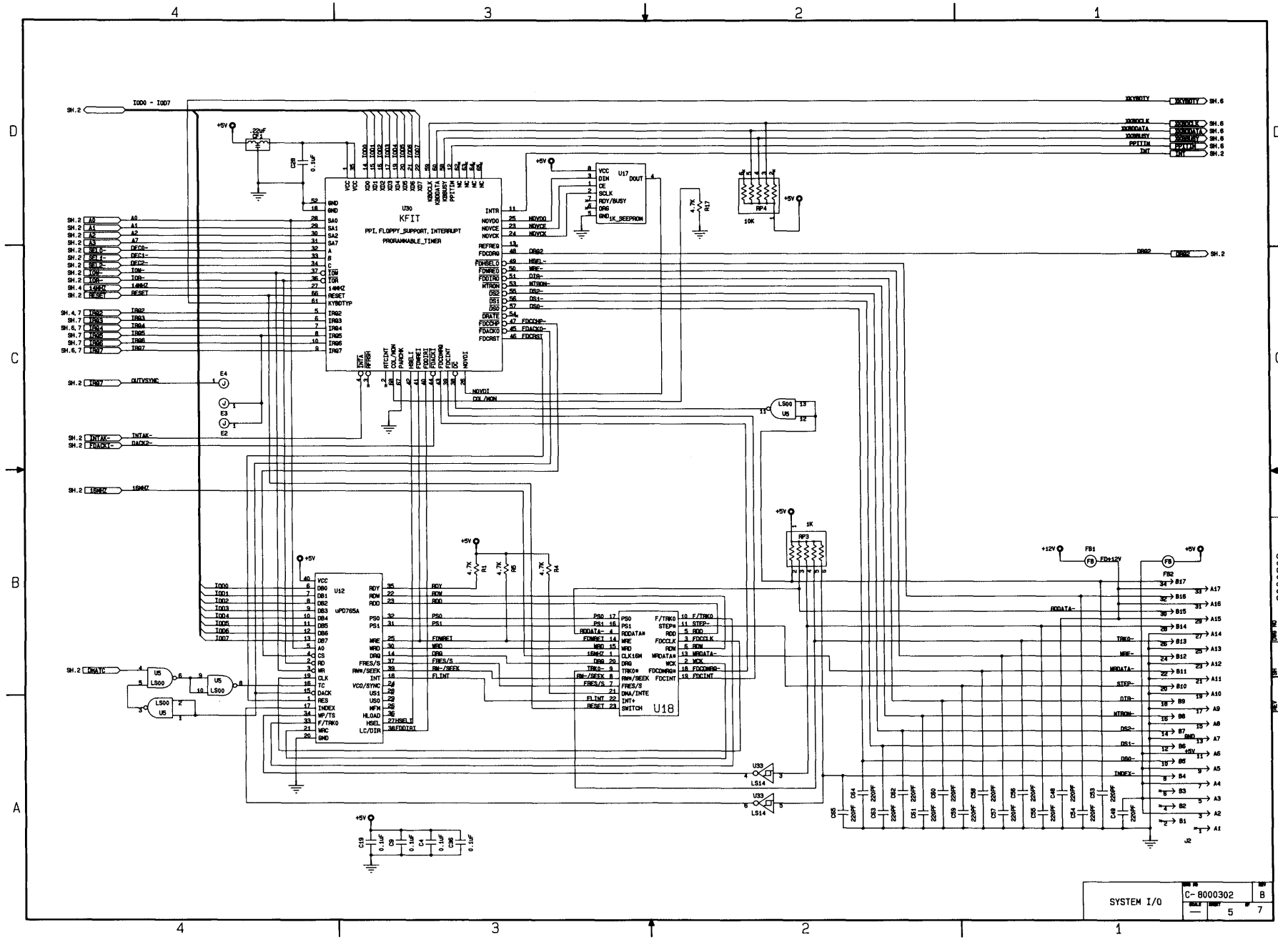
SHEET 1 OF 7

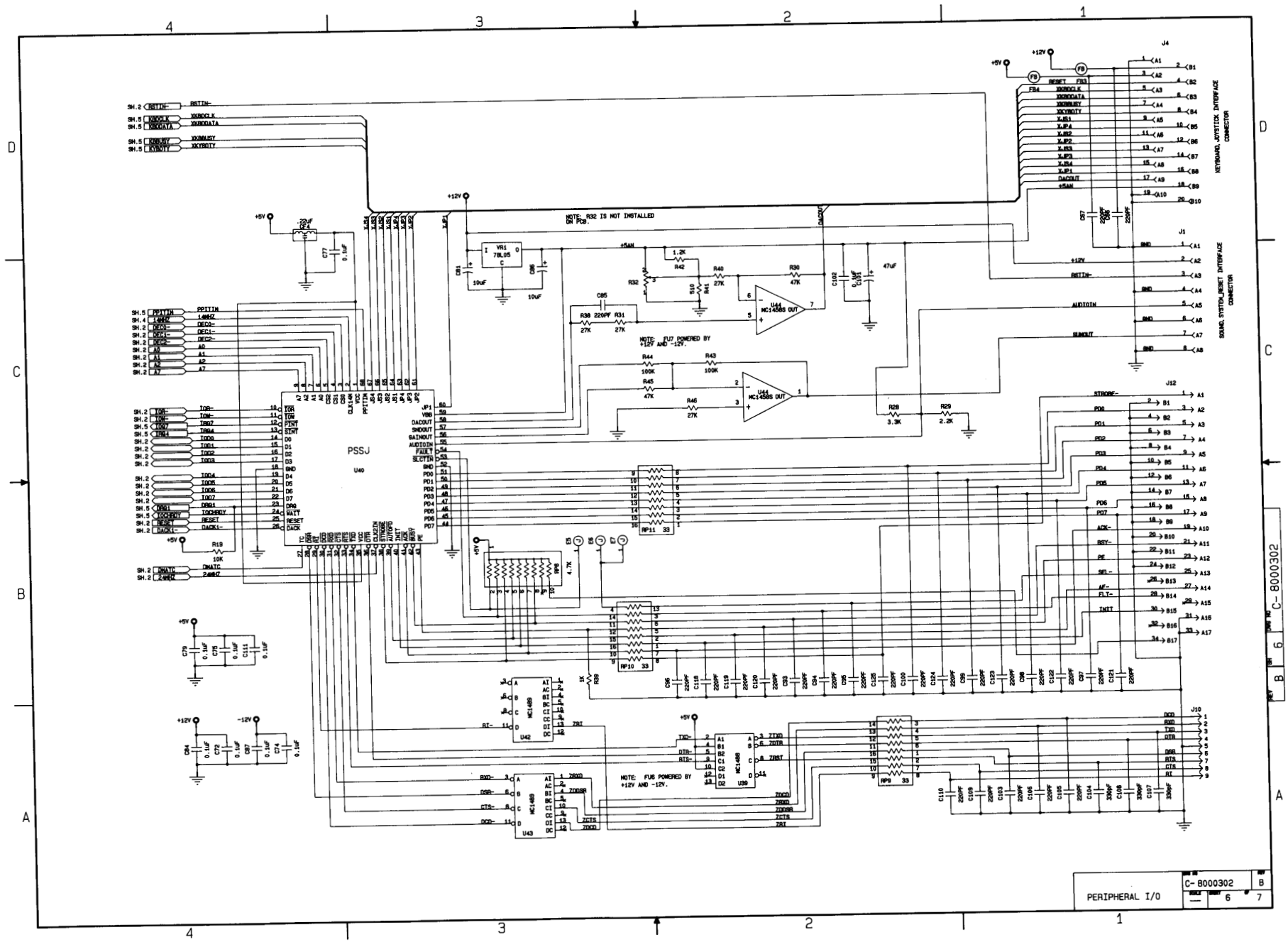
886

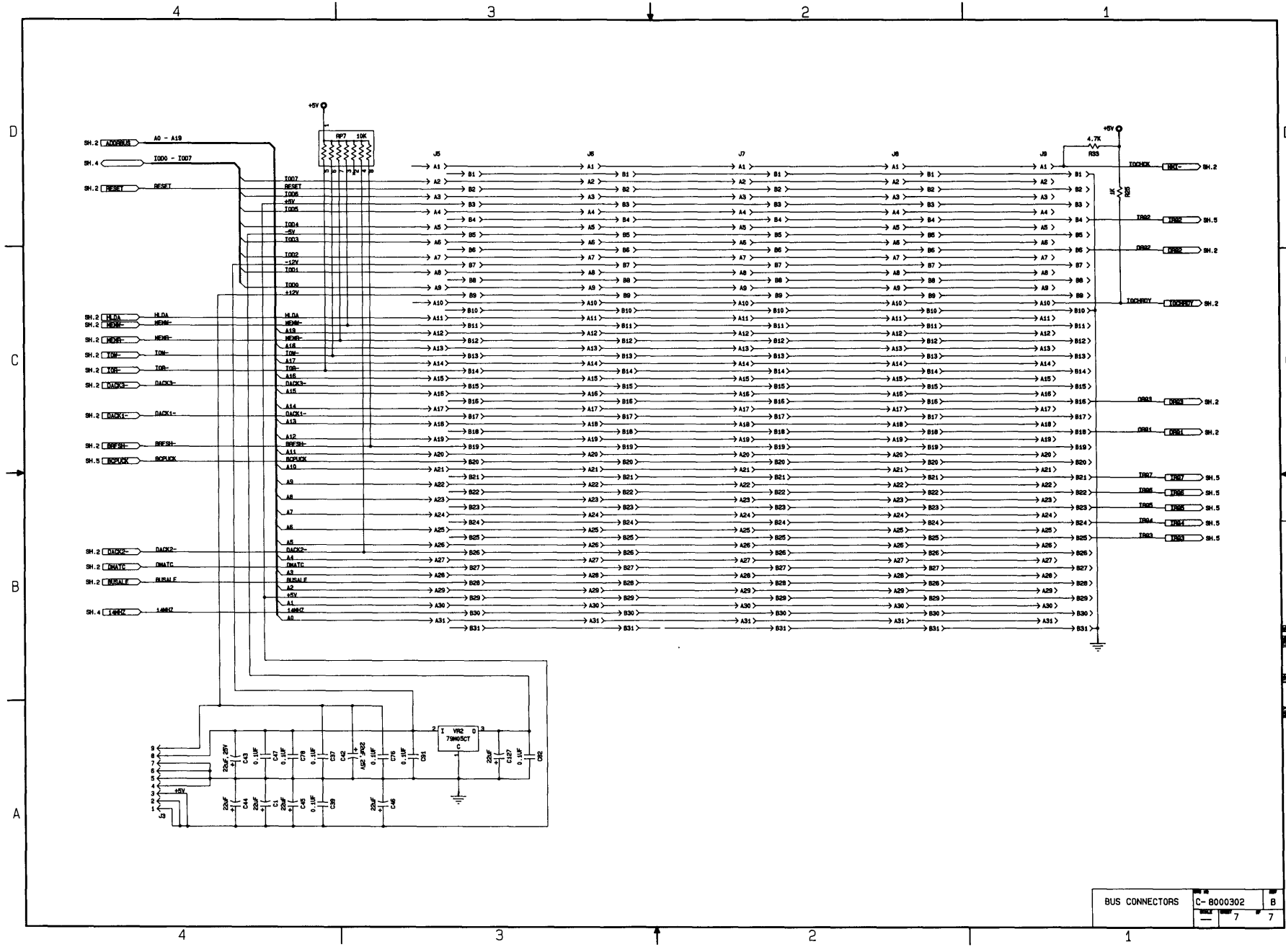

8079024
QFP Pinouts
U41
8087
U21
8086
U29
NOTE: R18 IS NOT STUFFED WHEN R1A,
U13B, C15A, C10A, AND U13A ARE STUFFED.
CPU
C- 8000302
B
2
7

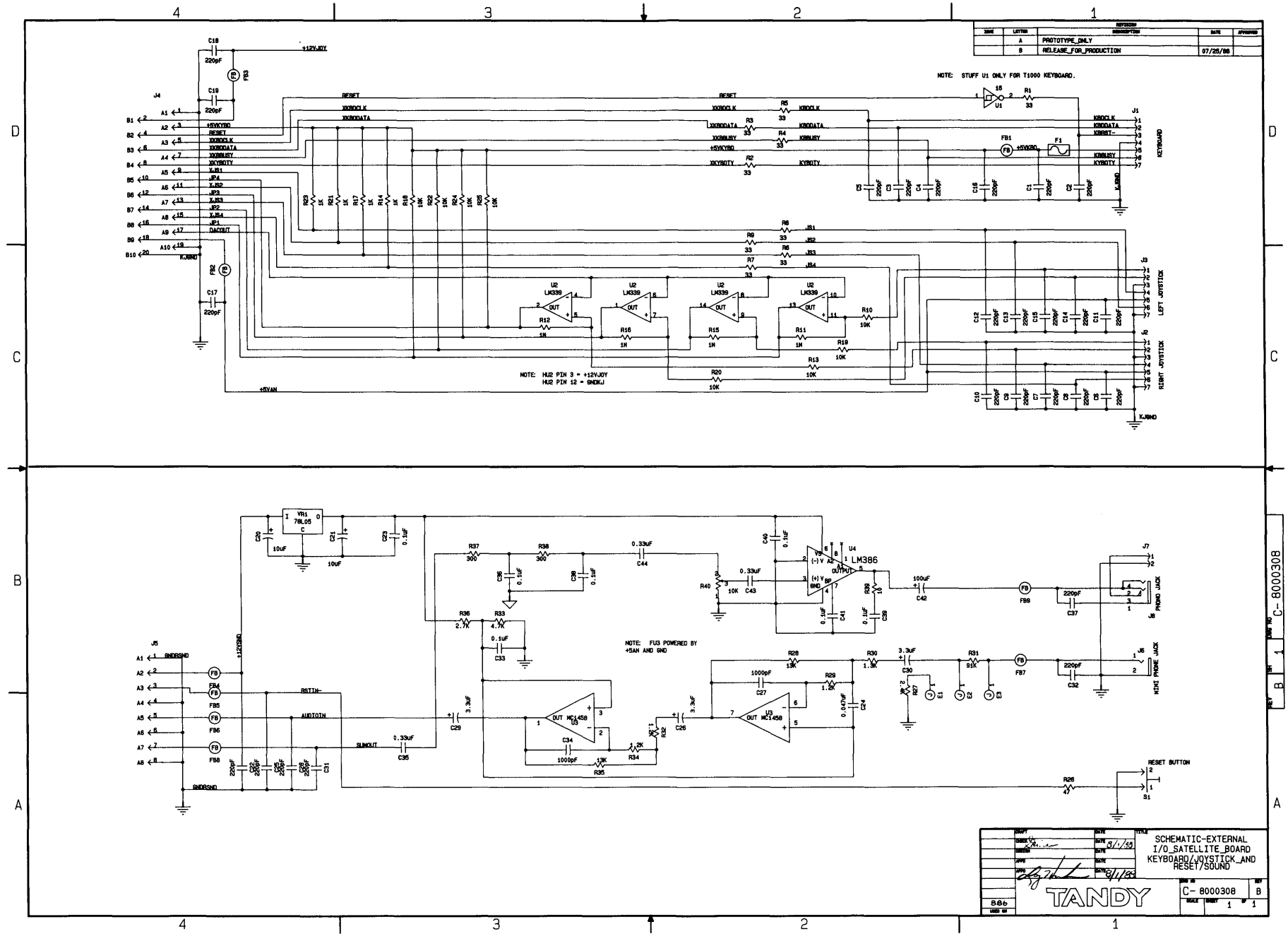

NOTE: SYSTEM DRAM'S ARE 150 nS ACCESS TIME.
NOTE: THE EIGHT DRAMS ON THE RIGHT SIDE ARE FOR EXPANSION, AND NOT STUFFED IN THE BASE UNIT.
NOTE: SYSTEM ROMS ARE 200 nS.
A0-19
AD0-15
MA0-MA7
AD4-7
AD8-11
AD12-15
ROMCS0-
ROMCS1-
MEM-
RAS0-
RAS1-
RAS2-
RAS3-
CAS-
+5V
NOTE: THESE FOUR TANTALUMS ARE DISTRIBUTED BULK FOR THE DRAM ARRAY, AND SHOULD BE PLACED ONE CAPACITOR FOR EACH GROUP OF FOUR CHIPS.
ROM, DRAM
C-8000302
B
3
7

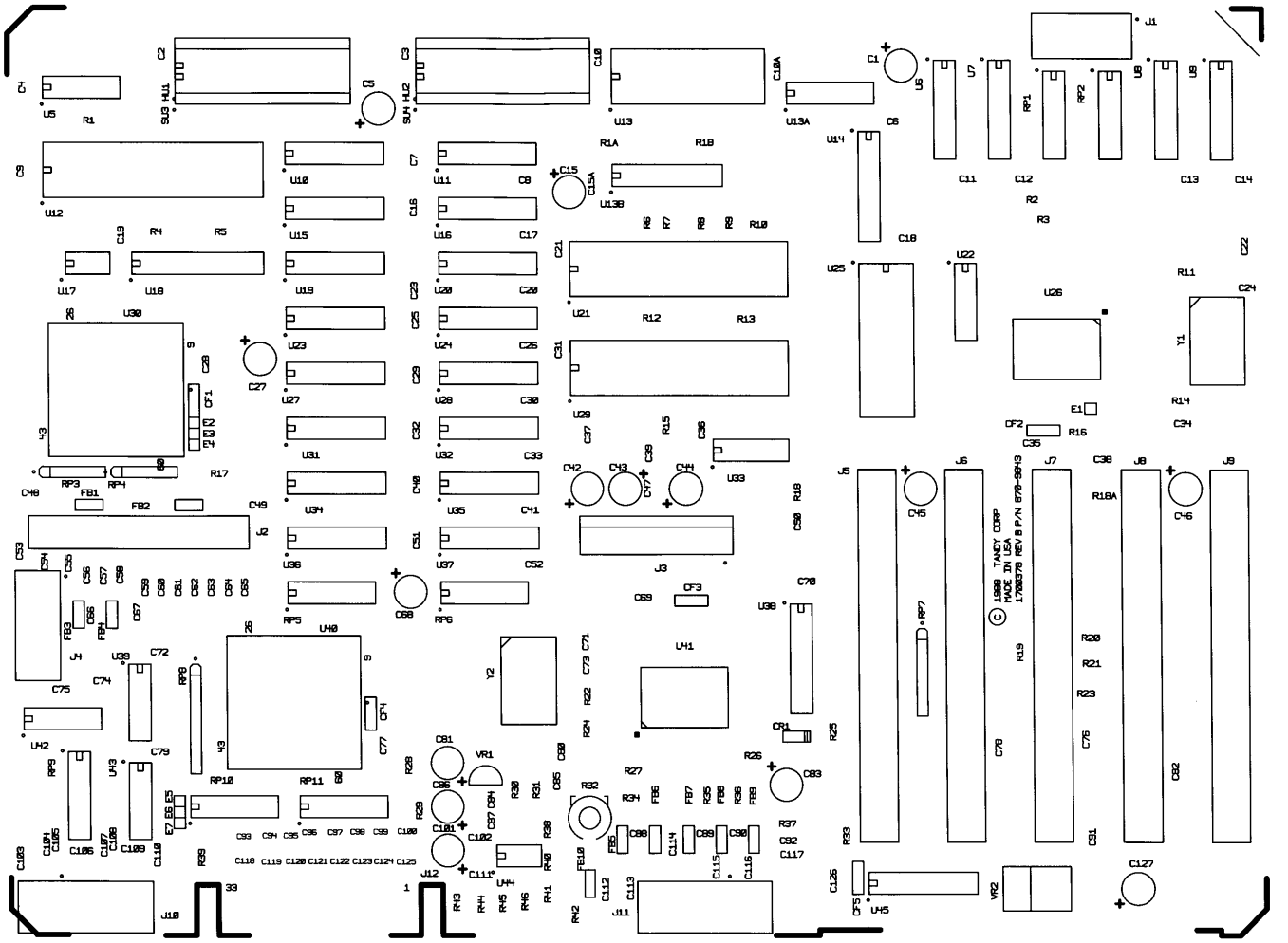

NOTE: THESE DRAMS ARE 120 nS ACCESS TIME.
TANDY VIDEO II
NOTE: CHARACTER GENERATOR ROM IS 200 nS.
NOTE: USE MOTOROLA PART ONLY
VIDEO
C- 8000302
B
4
7


U30
KFIT
PPI, FLOPPY_SUPPORT, INTERRUPT
PROGRAMMABLE_TIMER
U12
uPD765A
U18
SWITCH
U17
1K_SEEPROM
RP4
10K
RP3
1K
SYSTEM I/O
C-8000302
B
SHEET 5 OF 7


PSSJ
U40
MC1488
MC1489
MC14558S OUT
VR1 78L05
J4
KEYBOARD, JOYSTICK INTERFACE CONNECTOR
J1
SOUND, SYSTEM_RESET INTERFACE CONNECTOR
J12
J10
NOTE: R32 IS NOT INSTALLED ON PCB.
NOTE: FU7 POWERED BY +12V AND -12V.
NOTE: FU8 POWERED BY +12V AND -12V.
PERIPHERAL I/O
C-8000302
B
6
7


BUS CONNECTORS
C-8000302
B
7
7


REVISIONS
LTR | LETTER | DESCRIPTION | DATE | APPROVED
A | PROTOTYPE_ONLY
B | RELEASE_FOR_PRODUCTION | 07/25/88
NOTE: STUFF U1 ONLY FOR T1000 KEYBOARD.
NOTE: HU2 PIN 3 = +12VJOY
HU2 PIN 12 = GNDKJ
NOTE: FU3 POWERED BY +5AN AND GND
RESET BUTTON
KEYBOARD
LEFT JOYSTICK
RIGHT JOYSTICK
PHONO JACK
MINI PHONE JACK
SCHEMATIC-EXTERNAL I/O_SATELLITE_BOARD KEYBOARD/JOYSTICK_AND RESET/SOUND
TANDY
C- 8000308
B
DRAWN
CHECKED
ENGR
APPR
DATE
SIZE
SHEET 1 OF 1
886

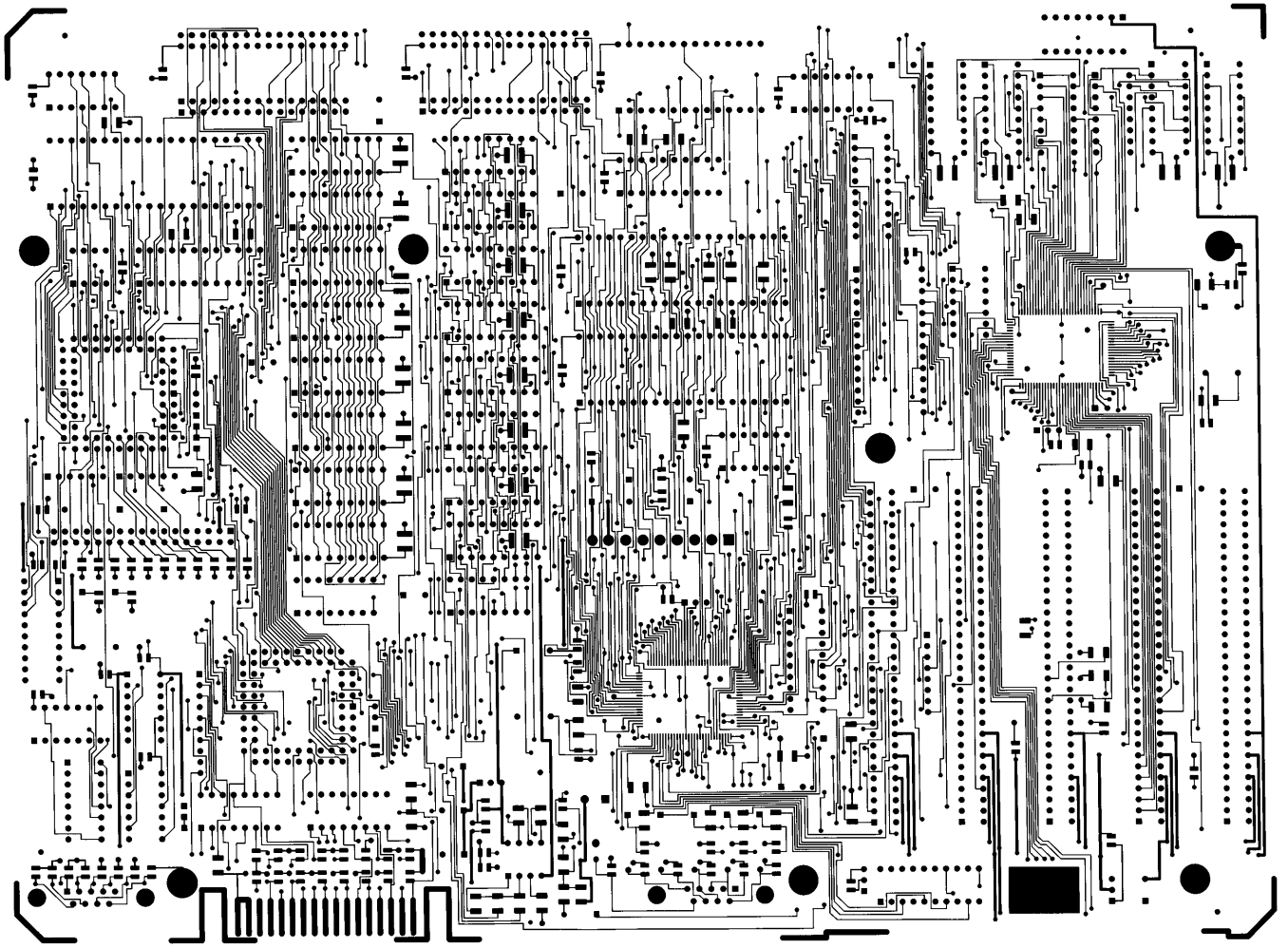


DWG NO. 1700378 REV. B

LAYER NAME SILKSCREEN

LAYER NO.

DATE 8/1/88

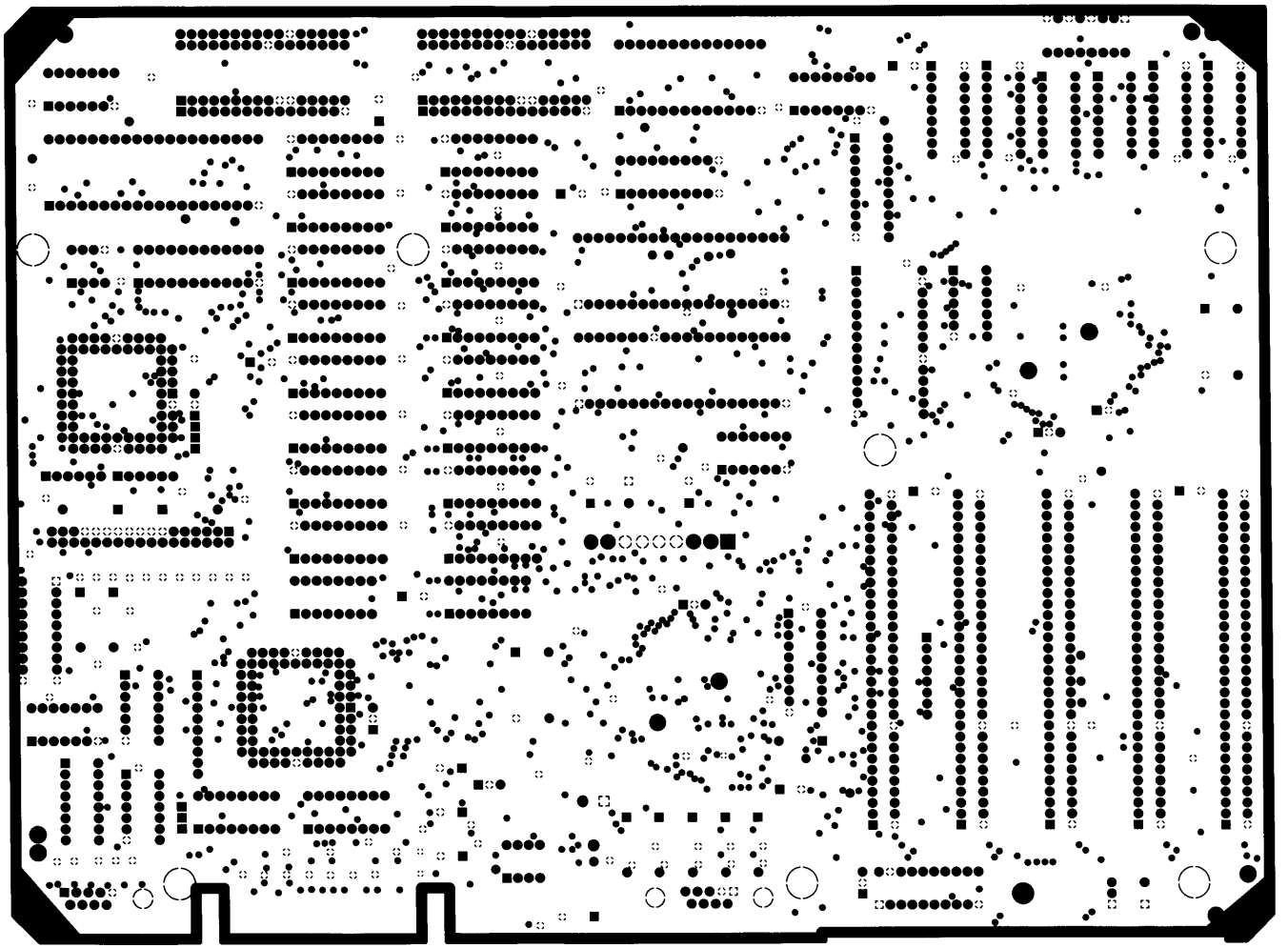


DWG NO. 1700370 REV. B

LAYER NAME COMPONENT SIDE

LAYER NO. 1

DATE 8/1/88

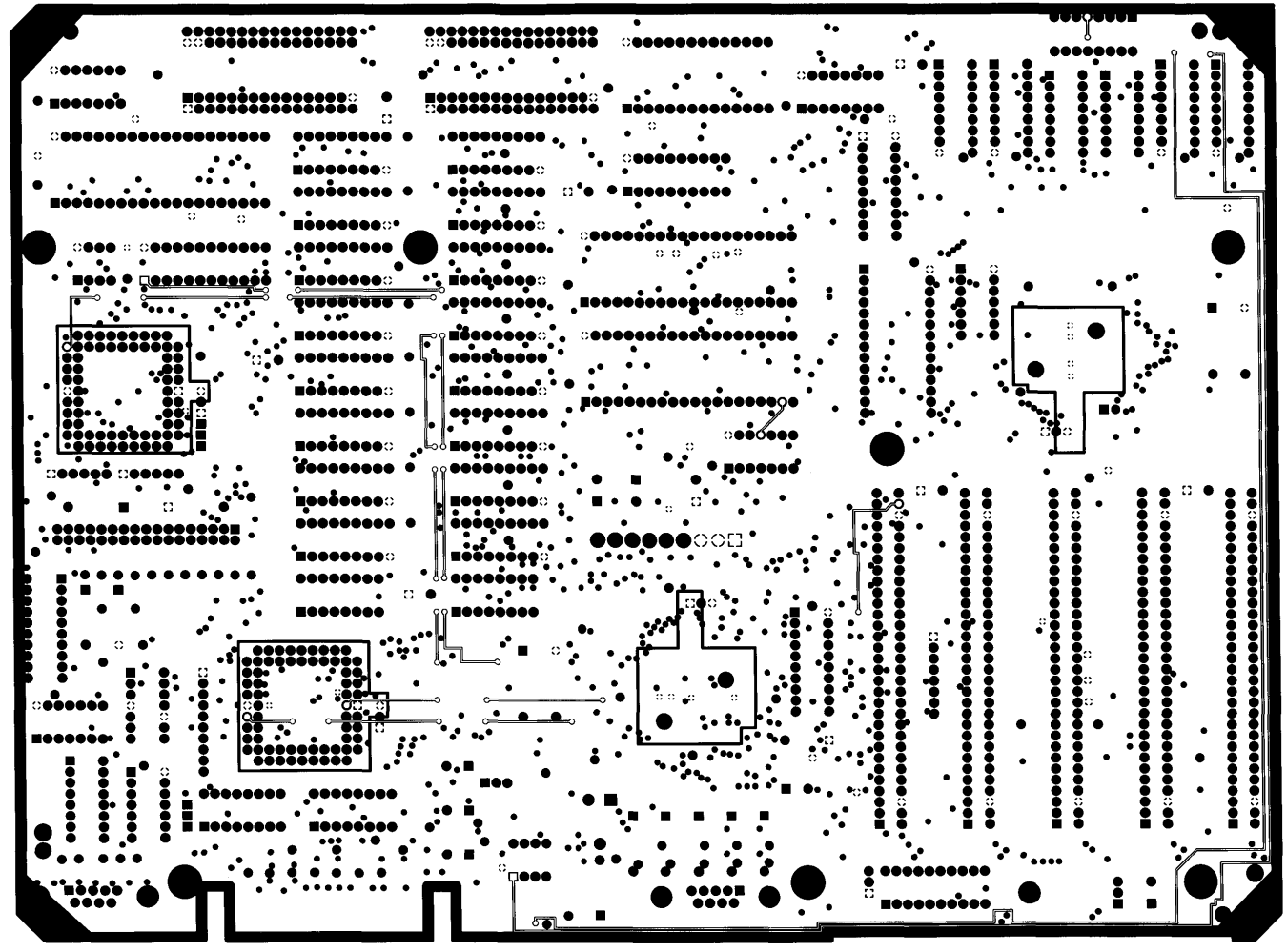


DWG NO. 1700378 REV. B

LAYER NAME GND PLANE

LAYER NO. 2

DATE 8/1/88

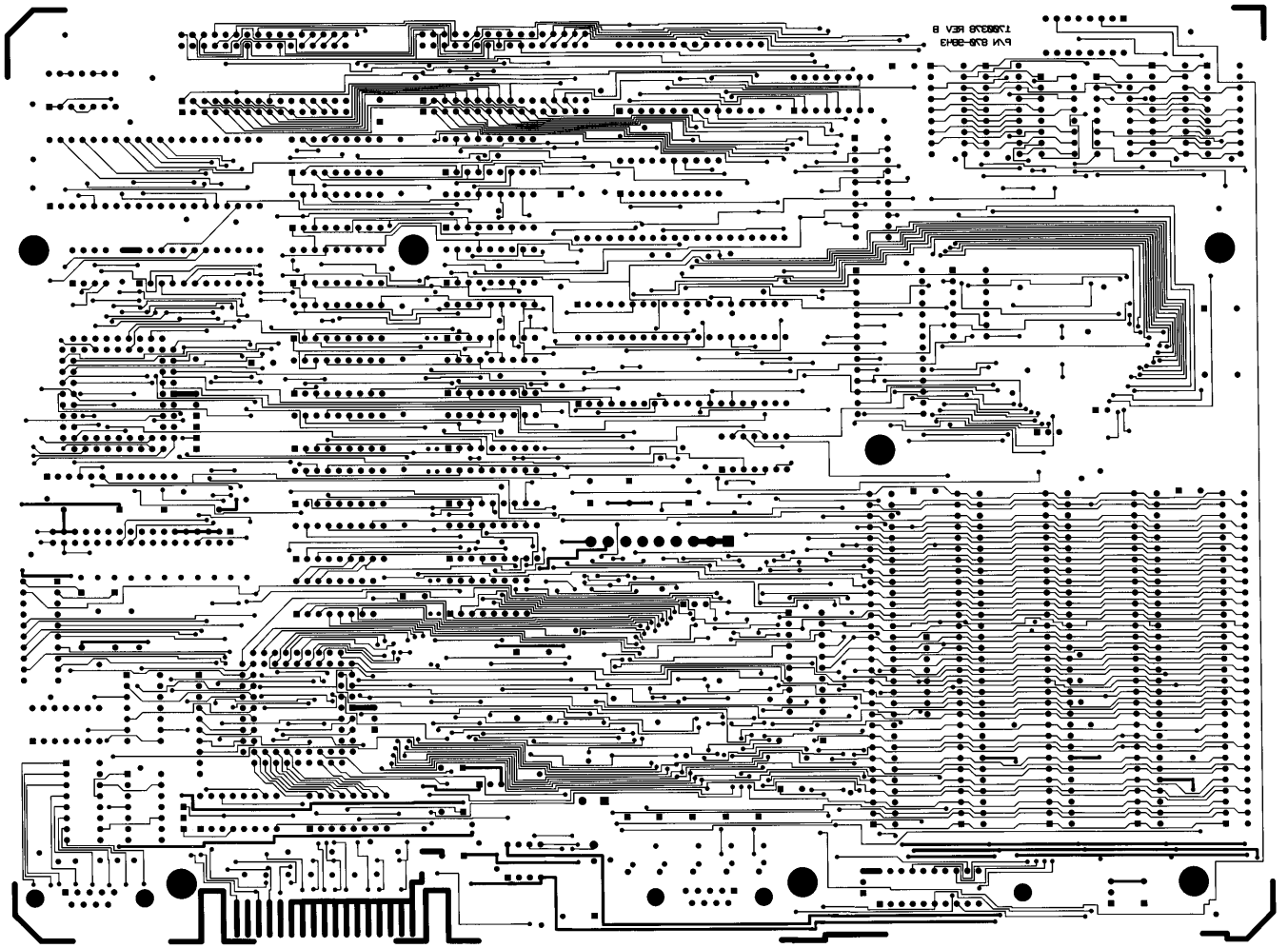


DWG NO. 1700378 REV. B

LAYER NAME +5V PLANE

LAYER NO. 3

DATE 8/1/88



DWG NO. 1700378 REV. B

LAYER NAME SOLDER SIDE

LAYER NO. 4

DATE 8/1/88

Devices

TANDY BUFFER BLUE CUSTOM IC

PART # 8079024

Table Of Contents

BUFFER BLUE PRELIMINARY SPECIFICATION

1.0 GENERAL

1.1 Functional Description

The Buffer Blue Custom IC is a VLSI ASIC for use in a PC/XT typearchitecture using an 8086 microprocessor. It comprises the following elements:

- 8237 Equivqlent.
- DRAM control.
- Address buffering and decoding.
- Data Conversion and Buffering.

It is contained in a 100 pin flat package suitable for surface mounting.

2.0 PIN LIST

PIN NAME	QTY.	I/O	DESCRIPTION
VCC	4		Power inputs
GND	4		Grounds
AD0 - AD15	16	Bidir.	Multiplexed address and data signals for connection to 8086 CPU, ROM data, and 16 bit RAM data.
ADR16 - ADR19	4	Bidir.	Address inputs from CPU, Address outputs from DMA.
S0 - S2	3	Inputs	Status inputs from CPU.
BHEB	1	Input	Bus High Enable from CPU or DMA.
RQ/GTB	1	Bidir.	Bus control handshaking with CPU.
READY	1	Output	CPU ready signal, active high. This signal is synchronized with Clock.
RESET	1	Output	CPU Reset signal, active high. This signal is synchronized with Clock.

PIN NAME	QTY.	I/O	DESCRIPTION
CPUCLK	1	Output	CPU clock signal, 12 MHz 50 % duty cycle, or 8 or 4 MHz 33 % duty cycle, internally switchable.
A0 - A11	12	Outputs	Buffered bus address outputs, intended to drive 5 XT type I/O slots, as well as a few on board peripherals.
IOD0 - IOD7	8	Bidir.	Eight bit peripheral data bus, intended to drive 5 XT type I/O slots, as well as all on board peripherals.
IORB	1	Output	CPU/DMA I/O Read signal, active low. System control line.
IOWB	1	Output	CPU/DMA I/O Write signal, active low. System control line.
MEMRB	1	Output	CPU/DMA Memory Read signal, active low. System control line.
MEMWB	1	Output	CPU/DMA Memory Write signal, active low. System control line.
RSTINB	1	Input	Master reset input, synchonized.
RDYIN	1	Input	Unsynchronized ready input.
CPUALE	1	Output	CPU Address Latch Enable. Decoded from CPU S0 - S2 when used with CPU accesses. Used to latch addresses on the multiplexed address/data bus.
BUSALE	1	Output	DMA Address Latch Enable. Generated by internal timing when used with DMA accesses. Used to latch addresses on the I/O bus.

PIN NAME	QTY.	I/O	DESCRIPTION
HLDA	1	Output	Indicates DMA cycle in progress.
INTAB	1	Output	Decode of S2 - S0 to indicate an interrupt acknowledge cycle in progress.
OSCIN	1	Input	Clock input, 30 MHz max, 50 % duty cycle.
MA0 - MA8	9	Outputs	Multiplexed Memory Addresses. Intended to drive 20 MOS memory devices.
WEHB, WELB	2	Outputs	Memory write enable signal, active low. Intended to drive 10 MOS memory devices.
RAS0B,RAS1B RAS2B,RAS3B	4	Outputs	Memory Row Address Strobes, active low. Intended to drive 16 MOS memory devices. All others intended to drive 4 MOS memory devices each.
CASB	1	Output	Memory Column Address Strobes, active low. Each intended to drive 20 MOS memory devices.
DRQ1, DRQ3 FDDMARQ	3	Inputs	DMA channel requests.
DACK1, DACK3 FDDMACKB	3	Outputs	DMA acknowledge signals.
DMATC	1	Output	DMA end of process signal.
ROMCS0B ROMCS1B	2	Output	Active Low ROM Chip select valid during a MEMR with A17, A18, and A19 active.

PIN NAME	QTY.	I/O	DESCRIPTION
SEL0 - SEL2	3	Outputs	I/O or Rom paging decodes, depending upon whether a memory or I/O cycle is in progress.
IOCHCK	1	Input	NMI from I/O Bus.
COPRNMI	1	Input	NMI from 8087 Coprocessor.
NMIOUT	1	Output	NMI to CPU.
REFRESH	1	Output	Refresh request to the I/O Bus.
TRESET	1	Input	Test pin. Must be tied Low.

3.0 ABSOLUTE MAXIMUM RATINGS

	Min	Typ	Max	Units
Storage Temperature:	-65		150	degrees C
Operating Temperature:	0	25	70	degrees C
All output pins	-0.5		7.0	volts DC
All input pins	-0.5		7.0	volts DC
Power Supply (Vcc)	-0.5		7.0	volts DC
Power dissipation			750	milliwatts

4.0 D. C. ELECTRICAL CHARACTERISTICS

4.1 Inputs

	Min	Typ	Max	Units
Leakage current			+/-10	uA
Vih	2.0		Vcc+.5	volts DC
Vil	-0.5		0.8	volts DC
Input capacitance			10	pF

4.2 RQ/GT, READY, CLOCK, INTAK, ROMCS0B, ROMCS0B, DACK1-DACK3, EOP, SEL0-SEL2, NMIOUT, CPUALE

	Min	Typ	Max	Units
Iol	2			mA
Vol			0.4	volts DC
Ioh	1			mA
Voh	2.4			volts DC
Capacitive load	40			pF

4.3 AD0 - AD15

	Min	Typ	Max	Units
Iol	2			mA
Vol			0.4	volts DC
Ioh	1			mA
Voh	2.4			volts DC
Capacitive load	80			pF

4.4 RAS1B, RAS2B, RAS3B

	Min	Typ	Max	Units
Iol	2			mA
Vol			0.4	volts DC
Ioh	1			mA
Voh	2.4			volts DC
Capacitive load	160			pF

4.5 MA0-MA8, RAS0B, CASB

with Slew Rate Control

	Min	Typ	Max	Units
Iol	8			mA
Vol			0.4	volts DC
Ioh	1			mA
Voh	2.4			volts DC
Capacitive load	160			pF

4.6 MEMRB, MEMWB, IORB, IOWB, BUSALE, HLDA, BHE, A0-A19, IOD0-IOD7, REFRESH, RESET, WEHB, WELB

with Slew Rate Control

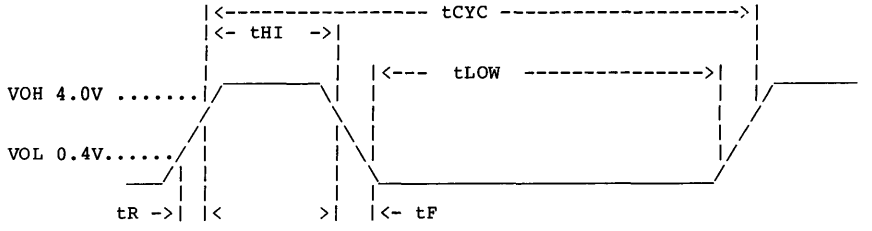
	Min	Typ	Max	Units
Iol	6			mA
Vol			0.4	volts DC
Ioh	2			mA
Voh	2.4			volts DC
Capacitive load	80			pF

5.0 AC CHARACTERISTICS

NOTE: All pins loaded with 85pf except Memory Address (MA0-8), RAS0, and CAS, which are loaded at 140pf.

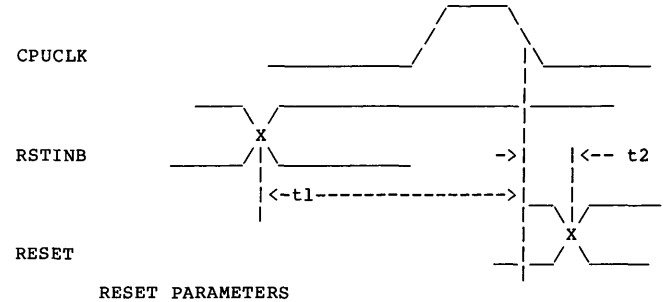
TIMING DIAGRAMS

FIGURE 1. CPUCLK



CLOCK PARAMETER	8.00 MHZ			4.00 MHZ			
	min	typ	max	min	typ	max	
tHI Level at least 4.0v	44			69			ns
tLOW Level not greater than 0.4v	68			118			ns
tR Rise time , 0.4 to 4.0v			10			10	ns
tF fall time , 4.0 to 0.4v			10			10	ns
tCYC		125			250		ns

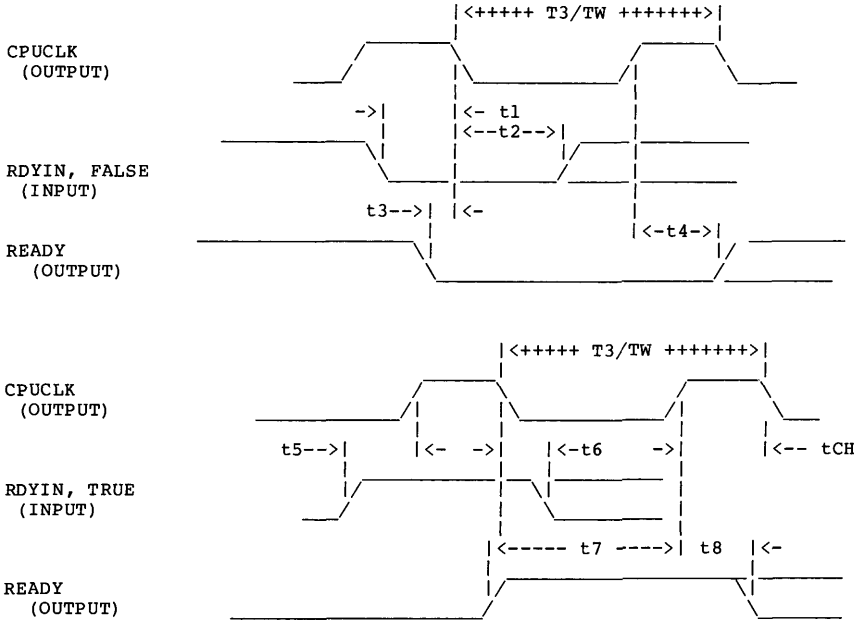
FIGURE 2. RESET



RESET PARAMETERS

t1	RSTIN Setup to CPUCLK low	Asynchronous input
t2	RESET Delay from CPUCLK low	6 min 24 ns max

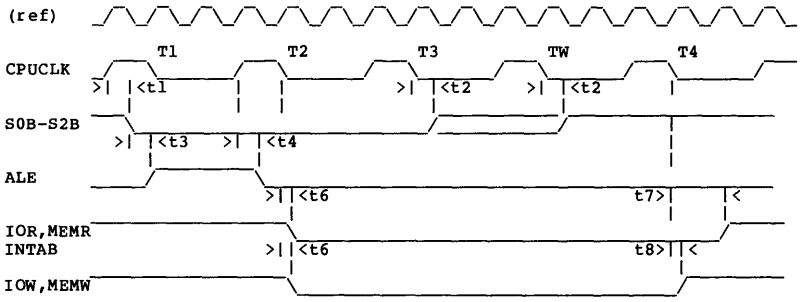
FIGURE 3. READY



READY PARAMETER

	min	max		
t1 RDYIN False Setup to CPUCLK low	30		ns	
t2 RDYIN False Hold after CPUCLK low	10		ns	
t3 READY False before CPUCLK low	0		ns	
t4 READY False Hold after CPUCLK hi	20		ns	
t5 RDYIN True Setup to CPUCLK hi	35		ns	
t6 RDYIN True Hold after CPUCLK low	10		ns	
t7 READY True before CPUCLK hi	66		ns	tRYHCH 8086
t8 READY True Hold after CPUCLK hi		20	ns	tCHRYX 8086

FIGURE 4. CONTROL GENERATOR



CONTROL GENERATOR

	min	max		
t1 STATUS Active Delay from CLK hi	10	60	ns	tCHSV 8086
t2 STATUS Inactive Delay from CLK low	10	70	ns	tCLSH 8086
t3 ALE True Delay from Status Active	0	22	ns	
t4 ALE False Delay from CLK hi	0	31	ns	
t6 STROBE True Delay from CLK low	0	31	ns	
t7 STROBE False Delay from CLK low	36	52	ns	
t8 STROBE False Delay from CLK hi	0	19	ns	

FIGURE 5A. ARBITTER/REQUEST

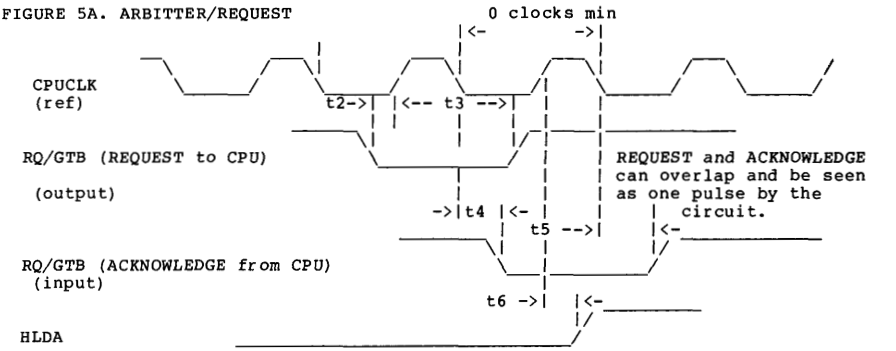
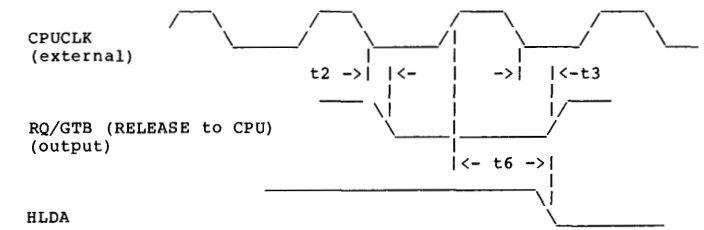


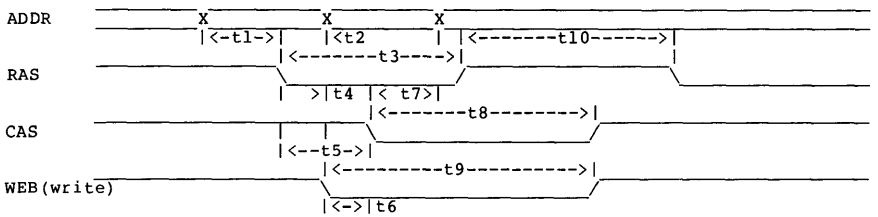
FIGURE 5B. ARBITTER/RELEASE



ARBITTER PARAMETER

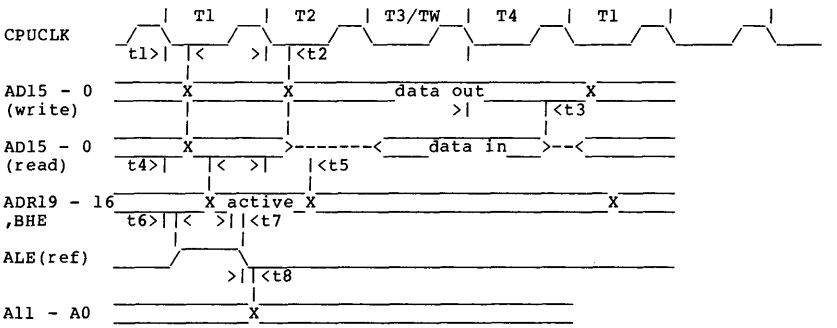
	min	max		
t2 CPUCLK low to RQ/GTB active (REQ/REL pulse)	20		ns	tGVCH 8086
t3 CPUCLK low to RQ/GTB inactive (REQ/REL pulse)	20		ns	tCHGX 8086
t4 RQ/GTB (True) setup to CPUCLK hi (ACK pulse)		50	ns	tCLGL 8086
t5 RQ/GTB (False) hold from CPUCLK low (ACK pulse)		50	ns	tCLGH 8086
t6 CPUCLK hi to HLDA Delay		30	ns	

MEMORY ACCESS TIMING (NO REFRESH)



		min	
t1	ADDRESS SETUP TO RAS	25	ns
t2	ROW ADDRESS HOLD TIME	17	ns
t3	RAS- WIDTH	150	ns
t4	COLUMN ADDRESS SETUP TIME	29	ns
t5	RAS- TO CAS- TIME	73	ns
t6	WE- TO CAS- SETUP TIME	29	ns
t7	COLUMN ADDRESS HOLD TIME	40	ns
t8	CAS- WIDTH	230	ns
t9	WE- WIDTH	220	ns
t10	RAS- PRECHARGE	109	ns

ADDRESS AND DATA BUS



PACKAGE PINOUT - QUAD FLAT PACK (PRODUCTION)
PACKAGE: PB30, DIE SIZE: 5.510MM x 5.500MM

PIN 1	AD1	PIN 26	OSC24M	PIN 51	HLDA	PIN 76	MA4
PIN 2	AD0	PIN 27	TRESET	PIN 52	REFRESH	PIN 77	MA3
PIN 3	BUSALE	PIN 28	RDYIN	PIN 53	WELB	PIN 78	MA2
PIN 4	CPUALE	PIN 29	RSTINB	PIN 54	WEHB	PIN 79	MA1
PIN 5	CPUCLK	PIN 30	IOCHCKB	PIN 55	RESET	PIN 80	MA0
PIN 6	DRQ1	PIN 31	DACK1B	PIN 56	READY	PIN 81	ADD19
PIN 7	FDDMARQ	PIN 32	FDDMACKB	PIN 57	NMIOUT	PIN 82	ADD18
PIN 8	DRQ3	PIN 33	DACK3B	PIN 58	INTAB	PIN 83	ADD17
PIN 9	IOD0	PIN 34	A0	PIN 59	SEL2	PIN 84	ADD16
PIN 10	IOD1	PIN 35	A1	PIN 60	SEL1	PIN 85	AD15
PIN 11	IOD2	PIN 36	A2	PIN 61	SEL0	PIN 86	AD14
PIN 12	IOD3	PIN 37	A3	PIN 62	ROMCSB1	PIN 87	AD13
PIN 13	IOD4	PIN 38	A4	PIN 63	ROMCSB0	PIN 88	AD12
PIN 14	VDD	PIN 39	A5	PIN 64	DMATC	PIN 89	VDD1
PIN 15	VSS	PIN 40	VSS	PIN 65	CASB	PIN 90	VSS
PIN 16	IOD5	PIN 41	VDD	PIN 66	VSS	PIN 91	AD11
PIN 17	IOD6	PIN 42	A6	PIN 67	VDD	PIN 92	AD10
PIN 18	IOD7	PIN 43	A7	PIN 68	RAS3B	PIN 93	AD9
PIN 19	IORB	PIN 44	A8	PIN 69	RAS2B	PIN 94	AD8
PIN 20	IOWB	PIN 45	A9	PIN 70	RAS1B	PIN 95	AD7
PIN 21	MEMRB	PIN 46	A10	PIN 71	RAS0B	PIN 96	AD6
PIN 22	MEMWB	PIN 47	A11	PIN 72	MA8	PIN 97	AD5
PIN 23	RQGTB	PIN 48	S0B	PIN 73	MA7	PIN 98	AD4
PIN 24	COPRNMI	PIN 49	S1B	PIN 74	MA6	PIN 99	AD3
PIN 25	BHEB	PIN 50	S2B	PIN 75	MA5	PIN 100	AD2

6.0 PORT DEFINITION MAP

```
PORT 00    DMA Controller
           IOW* = 0: Channel 0 Base and Current Address
                     Internal Flip/Flop = 0: Write A0-A7
                     Internal Flip/Flop = 1: Write A8-A15
           IOR* = 0: Channel 0 Current Address
                     Internal Flip/Flop = 0: Read A0-A7
                     Internal Flip/Flop = 1: Read A8-A15

PORT 01    DMA Controller
           IOW* = 0: Channel 0 Base and Current Word Count
                     Internal Flip/Flop = 0: Write W0-W7
                     Internal Flip/Flop = 1: Write W8-W15
           IOR* = 0: Channel 0 Current Word Count
                     Internal Flip/Flop = 0: Read W0-W7
                     Internal Flip/Flop = 1: Read W8-W15

PORT 02    DMA Controller
           IOW* = 0: Channel 1 Base and Current Address
                     Internal Flip/Flop = 0: Write A0-A7
                     Internal Flip/Flop = 1: Write A8-A15
           IOR* = 0  Channel 1 Current Address
                     Internal Flip/Flop = 0: Read A0-A7
                     Internal Flip/Flop = 1: Read A8-A15

PORT 03    DMA Controller
           IOW* = 0: Channel 1 Base and Current Word Count
                     Internal Flip/Flop = 0: Write W0-W7
                     Internal Flip/Flop = 1: Write W8-W15
           IOR* = 0: Channel 1 Current Word Count
                     Internal Flip/Flop = 0: Read W0-W7
                     Internal Flip/Flop = 1: Read W8-W15

PORT 04    DMA Controller
           IOW* = 0: Channel 2 Base and Current Address
                     Internal Flip/Flop = 0: Write A0-A7
                     Internal Flip/Flop = 1: Write A8-A15
           IOR* = 0: Channel 2 Current Address
                     Internal Flip/Flop = 0: Read A0-A7
                     Internal Flip/Flop = 1: Read A8-A15

PORT 05    DMA Controller
           IOW* = 0: Channel 2 Base and Current Word Count
                     Internal Flip/Flop = 0: Write W0-W7
                     Internal Flip/Flop = 1: Write W8-W15
           IOR* = 0: Channel 2 Current Word Count
                     Internal Flip/Flop = 0: Read W0-W7
                     Internal Flip/Flop = 1: Read W8-W15
```

PORT 06 DMA Controller

IOW* = 0: Channel 3 Base and Current Address
Internal Flip/Flop = 0: Write A0-A7
Internal Flip/Flop = 1: Write A8-A15

IOR* = 0: Channel 3 Current Address
Internal Flip/Flop = 0: Read A0-A7
Internal Flip/Flop = 1: Read A8-A15

PORT 07 DMA Controller

IOW* = 0: Channel 3 Base and Current Word Count
Internal Flip/Flop = 0: Write W0-W7
Internal Flip/Flop = 1: Write W8-W15

IOR* = 0: Channel 3 Current Word Count
Internal Flip/Flop = 0: Read W0-W7
Internal Flip/Flop = 1: Read W8-W15

PORT 08 DMA Controller

IOW* = 0, Write Command Register

BIT	Description
0	0 = Memory to Memory Disable
	1 = Memory to Memory Enable
1	0 = Channel 0 Address Hold Disable
	1 = Channel 0 Address Hold Enable
	X If bit 0 = 0
2	0 = Controller enable
	1 = Controller disable
3	0 = Normal timing
	1 = Compressed timing
	X If bit 0 = 1
4	0 = Fixed priority
	1 = Rotating priority
5	0 = Late write selection
	1 = Extended write selection
	X If bit 3 = 1
6	0 = DREQ sense active high
	1 = DREQ sense active low
7	0 = DACK sense active low
	1 = DACK sense active high

IOR* = 0, Read Status Register

BIT	Description
0	1 = Channel 0 has reached TC
1	1 = Channel 1 has reached TC
2	1 = Channel 2 has reached TC
3	1 = Channel 3 has reached TC
4	1 = Channel 0 Request
5	1 = Channel 1 Request
6	1 = Channel 2 Request
7	1 = Channel 3 Request

```
PORT 09    DMA Controller
           IOW* = 0, Write Request Register
  BIT        Description
  0-1        Bitl Bit0
             0    0   Select channel 0
             0    1   Select channel 1
             1    0   Select channel 2
             1    1   Select channel 3
  2          0    Reset request bit
             1    Set request bit
  3-7        Don't Care
           IOR* = 0, Illegal

PORT 0A    DMA Controller
           IOW* = 0, Write Single Mask Register
  BIT        Description
  0-1        Bitl Bit0
             0    0   Select channel 0 mask bit
             0    1   Select channel 1 mask bit
             1    0   Select channel 2 mask bit
             1    1   Select channel 3 mask bit
  2          0    Clear mask bit (Enable Channel)
             1    Set mask bit (Disable Channel)
  3-7        Don't Care
           IOR* = 0, Illegal
```

```
PORT 0B     DMA Controller
           IOW* = 0, Write Mode Register
  BIT        Description
  0-1        Bit1 Bit0
             0    0  Channel 0 select
             0    1  Channel 1 select
             1    0  Channel 2 select
             1    1  Channel 3 select
  2-3        Bit3 Bit2
             0    0  Verify transfer
             0    1  Write transfer to memory
             1    0  Read transfer to memory
             1    1  Illegal
             X    If bits 6 and 7 = 11
  4          0    Autoinitialization disable
             1    Autoinitialization enable
  5          0    Address increment select
             1    Address decrement select
  6-7        Bit7 Bit6
             0    0  Demand mode select
             0    1  Single mode select
             1    0  Block mode select
             1    1  Cascade mode select
           IOR* = 0, Illegal

PORT 0C    DMA Controller
           IOW* = 0, Clear Byte Pointer Flip/Flop
           IOR* = 0, Illegal

PORT 0D    DMA Controller
           IOW* = 0, Master Clear
           IOR* = 0, Read Temporary Register

PORT 0E    DMA Controller
           IOW* = 0, Clear Mask Register
           IOR* = 0, Illegal

PORT 0F    DMA Controller
           IOW* = 0, Write all Mask Register Bits
  Bit        Description
   0         0 = Clear channel 0 mask bit (Enable)
             1 = Set channel 0 mask bit (Disable)
   1         0 = Clear channel 1 mask bit (Enable)
             1 = Set channel 1 mask bit (Disable)
   2         0 = Clear channel 2 mask bit (Enable)
             1 = Set channel 2 mask bit (Disable)
   3         0 = Clear channel 3 mask bit (Enable)
             1 = Set channel 3 mask bit (Disable)
   4-7       Don't Care
           IOR* = 0, Illegal
```

PORT 62 - WRITE ONLY IN BUFFER BLUE
BIT 3: 0 = Slow CPUCLK (default)
1 = Fast CPUCLK

PORT 65 - WRITE ONLY IN BUFFER BLUE
BIT 2: 0 = 16 Bit Video
1 = 8 Bit Video (default)

PORT 80 DMA Page Reg. (Not Used)

PORT 81 - WRITE ONLY

Bit	Description
0	DMA Ch 2 Address A16
1	DMA Ch 2 Address A17
2	DMA Ch 2 Address A18
3	DMA Ch 2 Address A19
4-7	Not Used

PORT 82 - WRITE ONLY

Bit	Description
0	DMA Ch 3 Address A16
1	DMA Ch 3 Address A17
2	DMA Ch 3 Address A18
3	DMA Ch 3 Address A19
4-7	Not Used

PORT 83 - WRITE ONLY

Bit	Description
0	DMA Ch 0 - 1 Address A16
1	DMA Ch 0 - 1 Address A17
2	DMA Ch 0 - 1 Address A18
3	DMA Ch 0 - 1 Address A19
4-7	Not Used

PORT A0 - NMI Mask Register, Write only

Bit	Description
7	1 = Enable NMI
	0 = Disable NMI (default)

```
PORT FFE9 - WRITE/READ
  BIT 0:  0 = Zero Wait States for Internal Memory
          1 = One Wait State for Internal Memory
  BIT       Description
  1-2       Bit2 Bitl
            0    0  Zero Wait States for Internal Memory
            0    1  One Wait State for Internal Memory
            1    0  Two Wait States for Internal Memory
            1    1  Three Wait States for Internal Memory
  BIT       Description
  3-4       Bit4 Bit3
            0    0  Zero Wait States for CPU I/O cycle
            0    1  One Wait State for CPU I/O cycle
            1    0  Two Wait States for CPU I/O cycle
            1    1  Three Wait States for CPU I/O cycle
  BIT 5:  0 = Early Write Strobe for DMA cycle
          1 = No Early Write Strobe for DMA cycle
  BIT 6:  0 = Zero Wait States for 16 Bit Video
          1 = One Wait State for 16 Bit Video
  BIT 7:  Must be 0 when OSCIN is equal to 28.63636MHz
          Must be 1 when OSCIN is equal to 24 MHz (default)

PORT FFEA - WRITE/READ
  BIT 0:  ROM PAGING 0
  BIT 1:  ROM PAGING 1
  BIT 2:  ROM PAGING 2
  BIT 3:  ROM PAGING 3
  BIT 4:  ROM PAGING 4
  BIT 5:  Not Used

  BIT     Description
  6-7     Bit7 Bit6
           0    0  Two Banks of 128K memory
           0    1  Four Banks of 128K memory
           1    0  One Bank of 512K memory
           1    1  One Bank of 512K memory, One Bank of 128K memory
```

NOTE: When reading Port FFEA, bit 4 will be inverted from what was written, (i.e. when a 0 was written, a 1 will be read; when a 1 was written, a 0 will be read.)

ROM Paging Definition:

Two 2 Meg ROMs (Two 1 Meg ROMs)	ADDRESS 19	18	17	16	ROM PAGES 4	3	2	1	0	ROMCS #0	#1	SELECT 2	1	0	64K Page ROM0	ROM1
F0000-FFFFF	1	1	1	1	x	x	x	x	x	0	1	x	1	1	1	
E0000-EFFFF	1	1	1	0	1	x	1	1	1	1	1	x	x	x		
E0000-EFFFF	1	1	1	0	1	x	1	1	0	0	1	x	1	0	2	
E0000-EFFFF	1	1	1	0	1	x	1	0	1	0	1	x	x	1	3	
E0000-EFFFF	1	1	1	0	1	x	1	0	0	0	1	x	0	0	4	
E0000-EFFFF	1	1	1	0	1	x	0	1	1	1	0	x	1	1		1
E0000-EFFFF	1	1	1	0	1	x	0	1	0	1	0	x	1	0		2
E0000-EFFFF	1	1	1	0	1	x	0	0	1	1	0	x	0	1		3
E0000-EFFFF	1	1	1	0	1	x	0	0	0	1	0	x	0	0		4
Two 4 Meg ROMs	**19**	**18**	**17**	**16**	**4**	**3**	**2**	**1**	**0**	**#0**	**#1**	**2**	**1**	**0**	**ROM0**	**ROM1**
F0000-FFFFF	1	1	1	1	x	x	x	x	x	0	1	1	1	1	1	
E0000-EFFFF	1	1	1	0	0	1	1	1	1	1	1	x	x	x		
E0000-EFFFF	1	1	1	0	0	1	1	1	0	0	1	1	1	0	2	
E0000-EFFFF	1	1	1	0	0	1	1	0	1	0	1	1	0	1	3	
E0000-EFFFF	1	1	1	0	0	1	1	0	0	0	1	1	0	0	4	
E0000-EFFFF	1	1	1	0	0	1	0	1	1	0	1	0	1	1	5	
E0000-EFFFF	1	1	1	0	0	1	0	1	0	0	1	0	1	0	6	
E0000-EFFFF	1	1	1	0	0	1	0	0	1	0	1	0	0	1	7	
E0000-EFFFF	1	1	1	0	0	1	0	0	0	0	1	0	0	0	8	
E0000-EFFFF	1	1	1	0	0	0	1	1	1	1	0	1	1	1		1
E0000-EFFFF	1	1	1	0	0	0	1	1	0	1	0	1	1	0		2
E0000-EFFFF	1	1	1	0	0	0	1	0	1	1	0	1	0	1		3
E0000-EFFFF	1	1	1	0	0	0	1	0	0	1	0	1	0	0		4
E0000-EFFFF	1	1	1	0	0	0	0	1	1	1	0	0	1	1		5
E0000-EFFFF	1	1	1	0	0	0	0	1	0	1	0	0	1	0		6
E0000-EFFFF	1	1	1	0	0	0	0	0	1	1	0	0	0	1		7
E0000-EFFFF	1	1	1	0	0	0	0	0	0	1	0	0	0	0		8

8237A
HIGH PERFORMANCE PROGRAMMABLE DMA CONTROLLER (8237A, 8237A-4, 8237A-5)

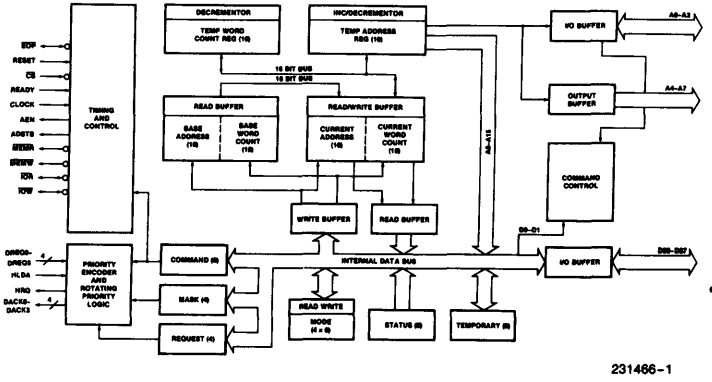
- **Enable/Disable Control of Individual DMA Requests**
- **Four Independent DMA Channels**
- **Independent Autoinitialization of All Channels**
- **Memory-to-Memory Transfers**
- **Memory Block Initialization**
- **Address Increment or Decrement**
- **High Performance: Transfers up to 1.6M Bytes/Second with 5 MHz 8237A-5**
- **Directly Expandable to Any Number of Channels**
- **End of Process Input for Terminating Transfers**
- **Software DMA Requests**
- **Independent Polarity Control for DREQ and DACK Signals**
- **Available in EXPRESS — Standard Temperature Range**
- **Available in 40-Lead Cerdip and Plastic Packages**

(See Packaging Spec, Order #231369)

The 8237A Multimode Direct Memory Access (DMA) Controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The 8237A offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

The 8237A is designed to be used in conjunction with an external 8-bit address latch. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips. The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to Autoinitialize to its original condition following an End of Process ($\overline{EOP}$). Each channel has a full 64K address and word count capability.

The 8273A-4 and 8237A-5 are 4 MHz and 5 MHz versions of the standard 3 MHz 8237A respectively.



231466-1

Figure 1. Block Diagram

231466-2

Figure 2. Pin Configuration

October 1987
Order Number: 231466-003

Table 1. Pin Description

Symbol	Type	Name and Function
V_{CC}		**POWER:** +5V supply.
V_{SS}		**GROUND:** Ground.
CLK	I	**CLOCK INPUT:** Clock Input controls the internal operations of the 8237A and its rate of data transfers. The input may be driven at up to 3 MHz for the standard 8237A and up to 5 MHz for the 8237A-5.
$\overline{CS}$	I	**CHIP SELECT:** Chip Select is an active low input used to select the 8237A as an I/O device during the Idle cycle. This allows CPU communication on the data bus.
RESET	I	**RESET:** Reset is an active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/last flip/flop and sets the Mask register. Following a Reset the device is in the Idle cycle.
READY	I	**READY:** Ready is an input used to extend the memory read and write pulses from the 8237A to accommodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time.
HLDA	I	**HOLD ACKNOWLEDGE:** The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses.
DREQ0–DREQ3	I	**DMA REQUEST:** The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active.
DB0–DB7	I/O	**DATA BUS:** The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program condition during the I/O Read to output the contents of an Address register, a Status register, the Temporary register or a Word Count register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the 8237A control registers. During DMA cycles the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the 8237A on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs place the data into the new memory location.
$\overline{IOR}$	I/O	**I/O READ:** I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the 8237A to access data from a peripheral during a DMA Write transfer.
$\overline{IOW}$	I/O	**I/O WRITE:** I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the 8237A. In the Active cycle, it is an output control signal used by the 8237A to load data to the peripheral during a DMA Read transfer.

Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
$\overline{EOP}$	I/O	**END OF PROCESS:** End of Process is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional $\overline{EOP}$ pin. The 8237A allows an external signal to terminate an active DMA service. This is accomplished by pulling the $\overline{EOP}$ input low with an external $\overline{EOP}$ signal. The 8237A also generates a pulse when the terminal count (TC) for any channel is reached. This generates an $\overline{EOP}$ signal which is output through the $\overline{EOP}$ line. The reception of $\overline{EOP}$, either internal or external, will cause the 8237A to terminate the service, reset the request, and, if Autoinitialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for Autoinitialize. In that case, the mask bit remains unchanged. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ should be tied high with a pull-up resistor if it is not used to prevent erroneous end of process inputs.
A0–A3	I/O	**ADDRESS:** The four least significant address lines are bidirectional three-state signals. In the Idle cycle they are inputs and are used by the CPU to address the register to be loaded or read. In the Active cycle they are outputs and provide the lower 4 bits of the output address.
A4–A7	O	**ADDRESS:** The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the DMA service.
HRQ	O	**HOLD REQUEST:** This is the Hold Request to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes 8237A to issue the HRQ.
DACK0–DACK3	O	**DMA ACKNOWLEDGE:** DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.
AEN	O	**ADDRESS ENABLE:** Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.
ADSTB	O	**ADDRESS STROBE:** The active high, Address Strobe is used to strobe the upper address byte into an external latch.
$\overline{MEMR}$	O	**MEMORY READ:** The Memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a memory-to-memory transfer.
$\overline{MEMW}$	O	**MEMORY WRITE:** The Memory Write is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.
PIN5	I	**PIN5:** This pin should always be at a logic HIGH level. An internal pull-up resistor will establish a logic high when the pin is left floating. It is recommended however, that PIN5 be connected to V_{CC}.

FUNCTIONAL DESCRIPTION

The 8237A block diagram includes the major logic blocks and all of the internal registers. The data interconnection paths are also shown. Not shown are the various control signals between the blocks. The 8237A contains 344 bits of internal memory in the form of registers. Figure 3 lists these registers by name and shows the size of each. A detailed description of the registers and their functions can be found under Register Description.

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

Figure 3. 8237A Internal Registers

The 8237A contains three basic blocks of control logic. The Timing Control block generates internal timing and external control signals for the 8237A. The Program Command Control block decodes the various commands given to the 8237A by the microprocessor prior to servicing a DMA Request. It also decodes the Mode Control word used to select the type of DMA during the servicing. The Priority Encoder block resolves priority contention between DMA channels requesting service simultaneously.

The Timing Control block derives internal timing from the clock input. In 8237A systems, this input will usually be the $\phi 2$ TTL clock from an 8224 or CLK from an 8085AH or 8284A. 33% duty cycle clock generators, however, may not meet the clock high time requirement of the 8237A of the same frequency. For example, 82C84A-5 CLK output violates the clock high time requirement of 8237A-5. In this case 82C84A CLK can simply be inverted to meet 8237A-5 clock high and low time requirements. For 8085AH-2 systems above 3.9 MHz, the 8085 CLK(OUT) does not satisfy 8237A-5 clock LOW and HIGH time requirements. In this case, an external clock should be used to drive the 8237A-5.

DMA OPERATION

The 8237A is designed to operate in two major cycles. These are called Idle and Active cycles. Each device cycle is made up of a number of states. The 8237A can assume seven separate states, each composed of one full clock period. State I (SI) is the inactive state. It is entered when the 8237A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State S0 (S0) is the first state of a DMA service. The 8237A has requested a hold but the processor has not yet returned an acknowledge. The 8237A may still be programmed until it receives HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the Ready line on the 8237A. Note that the data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active at the same time. The data is not read into or driven out of the 8237A in I/O-to-memory or memory-to-I/O DMA transfers.

Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22, S23, S24) for the write-to-memory half of the transfer.

IDLE CYCLE

When no channel is requesting service, the 8237A will enter the Idle cycle and perform "SI" states. In this cycle the 8237A will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample $\overline{CS}$, looking for an attempt by the microprocessor to write or read the internal registers of the 8237A. When $\overline{CS}$ is low and HLDA is low, the 8237A enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers. Address lines A0–A3 are inputs to the device and select which registers will be read or written. The $\overline{IOR}$ and $\overline{IOW}$ lines are used to select and time reads or writes. Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional bit of address. This bit is used to determine the upper or lower byte of the 16-bit Address and Word Count registers. The flip-flop is reset by Master Clear or Reset. A separate software command can also reset this flip-flop.

Special software commands can be executed by the 8237A in the Program Condition. These commands are decoded as sets of addresses with the $\overline{CS}$ and $\overline{IOW}$. The commands do not make use of the data bus. Instructions include Clear First/Last Flip-Flop and Master Clear.

ACTIVE CYCLE

When the 8237A is in the Idle cycle and a non-masked channel requests a DMA service, the device will output an HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode—In Single Transfer mode the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count "rolls over" from zero to FFFFH, a Terminal Count (TC) will cause an Autoinitialize if the channel has been programmed to do so.

DREQ must be held active until DACK becomes active in order to be recognized. If DREQ is held active throughout the single transfer, HRQ will go inactive and release the bus to the system. It will again go active and, upon receipt of a new HLDA, another single transfer will be performed. In 8080A, 8085AH, 8088, or 8086 system, this will ensure one full machine cycle execution between DMA transfers. Details of timing between the 8237A and other bus control protocols will depend upon the characteristics of the microprocessor involved.

Block Transfer Mode—In Block Transfer mode the device is activated by DREQ to continue making transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process ($\overline{EOP}$) is encountered. DREQ need only be held active until DACK becomes active. Again, an Autoinitialization will occur at the end of the service if the channel has been programmed for it.

Demand Transfer Mode—In Demand Transfer mode the device is programmed to continue making transfers until a TC or external $\overline{EOP}$ is encountered or until DREQ goes inactive. Thus transfers may continue until the I/O device has exhausted its data capacity. After the I/O device has had a chance to catch up, the DMA service is re-established by means of a DREQ. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the 8237A Current Address and Current Word Count registers. Only an $\overline{EOP}$ can cause an Autoinitialize at the end of the service. $\overline{EOP}$ is generated either by TC or by an external signal. DREQ has to be low before S4 to prevent another Transfer.

Cascade Mode—This mode is used to cascade more than one 8237A together for simple system expansion. The HRQ and HLDA signals from the additional 8237A are connected to the DREQ and DACK signals of a channel of the initial 8237A. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial 8237A is used only for prioritizing the additional device, it does not output any address or control

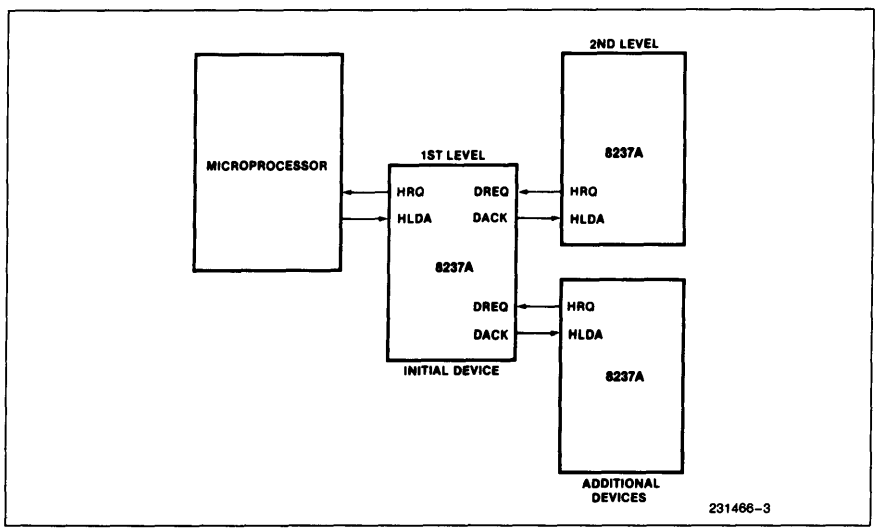


Figure 4. Cascaded 8237As

signals of its own. These could conflict with the outputs of the active channel in the added device. The 8237A will respond to DREQ and DACK but all other outputs except HRQ will be disabled. The ready input is ignored.

Figure 4 shows two additional devices cascaded into an initial device using two of the previous channels. This forms a two level DMA system. More 8237As could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level device, forming a third level.

TRANSFER TYPES

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{MEMW}$ and $\overline{IOR}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$. Verify transfers are pseudo transfers. The 8237A operates as in Read or Write transfers generating addresses, and responding to EOP, etc. However, the memory and I/O control lines all remain inactive. The ready input is ignored in verify mode.

Memory-to-Memory—To perform block moves of data from one memory address space to another with a minimum of program effort and time, the 8237A includes a memory-to-memory transfer feature. Programming a bit in the Command register selects channels 0 and 1 to operate as memory-to-memory transfer channels. The transfer is initiated by setting the software DREQ for channel 0. The 8237A requests a DMA service in the normal manner. After HLDA is true, the device, using four state transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the 8237A internal Temporary register. Channel 1 then performs a four-state transfer of the data from the Temporary register to memory using the address in its Current Address register and incrementing or decrementing it in the normal manner. The channel 1 current Word Count is decremented. When the word count of channel 1 goes to FFFFH, a TC is generated causing an $\overline{EOP}$ output terminating the service.

Channel 0 may be programmed to retain the same address for all transfers. This allows a single word to be written to a block of memory.

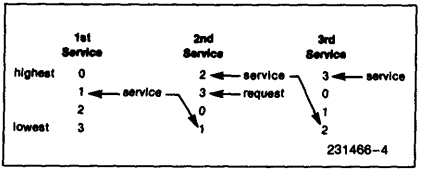
The 8237A will respond to external $\overline{EOP}$ signals during memory-to-memory transfers. Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of memory-to-memory transfers is found in Figure 12. Memory-to-memory operations can be detected as an active AEN with no DACK outputs.

Autoinitialize—By programming a bit in the Mode register, a channel may be set up as an Autoinitialize channel. During Autoinitialize initialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word count registers of that channel following $\overline{EOP}$. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not altered when the channel is in Autoinitialize. Following Autoinitialize the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected. In order to Autoinitialize both channels in a memory-to-memory transfer, both word counts should be programmed identically. If interrupted externally, $\overline{EOP}$ pulses should be applied in both bus cycles.

Priority—The 8237A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interfering with that service until it is completed.

After completion of a service, HRQ will go inactive and the 8237A will wait for HLDA to go low before activating HRQ to service another channel.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.



With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.

Compressed Timing—In order to achieve even greater throughput where system characteristics permit, the 8237A can compress the transfer time to two clock cycles. From Figure 11 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8–A15 need updating (see Address Generation). Timing for compressed transfers is found in Figure 14.

Address Generation—In order to reduce pin count, the 8237A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are output by the 8237A directly. Lines A0–A7 should be connected to the address bus. Figure 11 shows the time relationships between CLK, AEN, ADSTB, DB0–DB7 and A0–A7.

During Block and Demand Transfer mode services, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the 8237A executes S1 states only when updating of A8–A15 in the latch is necessary. This means for long services, S1 states and Address Strobes may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

REGISTER DESCRIPTION

Current Address Register—Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an $\overline{EOP}$.

Current Word Register—Each channel has a 16-bit Current Word Count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count register (i.e., programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialization back to its original value. Autoinitialize can occur only when an $\overline{EOP}$ occurs. If it is not Autoinitialized, this register will have a count of FFFFH after TC.

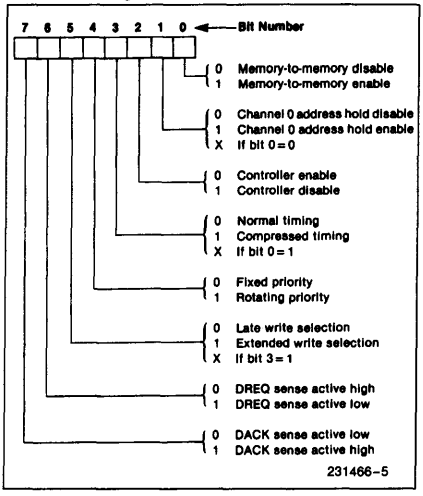
Base Address and Base Word Count Registers—Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. These registers cannot be read by the microprocessor.

Command Register—This 8-bit register controls the operation of the 8237A. It is programmed by the microprocessor in the Program Condition and is cleared by Reset or a Master Clear instruction. The following table lists the function of the command bits. See Figure 6 for address coding.

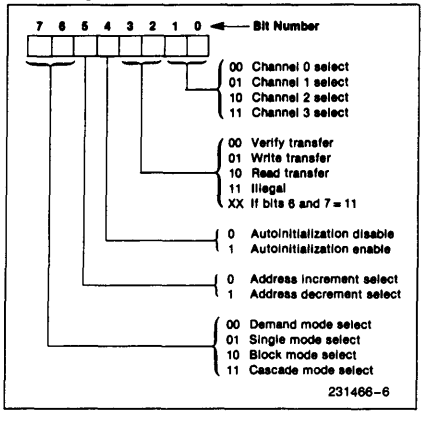
Mode Register—Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register is to be written.

Request Register—The 8237A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are non-maskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external $\overline{EOP}$. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 5 for register address coding. In order to make a software request, the channel must be in Block Mode.

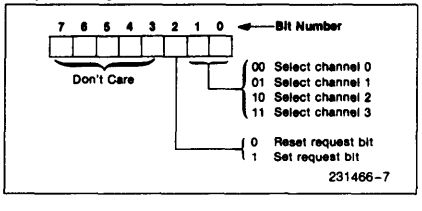
Command Register



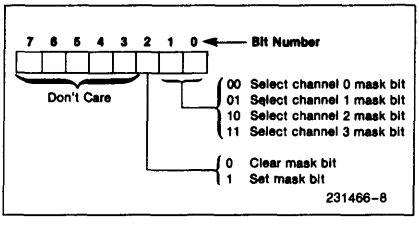
Mode Register



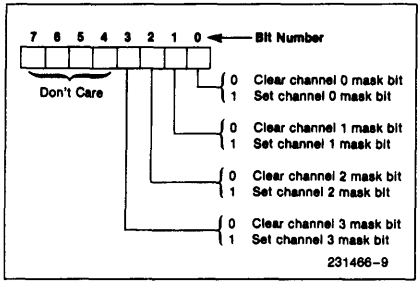
Request Register



Mask Register—Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. See Figure 5 for instruction addressing.



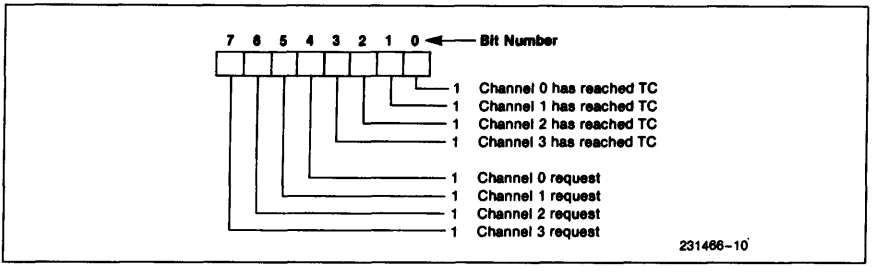
All four bits of the Mask register may also be written with a single command.



Register	Operation	Signals						
		$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

Figure 5. Definition of Register Codes

Status Register—The Status register is available to be read out of the 8237A by the microprocessor. It contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which chan-



nels have pending DMA requests. Bits 0–3 are set every time a TC is reached by that channel or an external $\overline{EOP}$ is applied. These bits are cleared upon Reset and on each Status Read. Bits 4–7 are set whenever their corresponding channel is requesting service.

Temporary Register—The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

Software Commands—These are additional special software commands which can be executed in the Program Condition. They do not depend on any specific bit pattern on the data bus. The three software commands are:

Clear First/Last Flip-Flop: This command must be executed prior to writing or reading new address or word count information to the 8237A. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary, and Internal First/Last Flip-Flop registers are cleared and the Mask register is set. The 8237A will enter the Idle cycle.

Clear Mask Register: This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Figure 6 lists the address codes for the software commands.

Signals						Operation
A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$	
1	0	0	0	0	1	Read Status Register
1	0	0	0	1	0	Write Command Register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write Request Register
1	0	1	0	0	1	Illegal
1	0	1	0	1	0	Write Single Mask Register Bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write Mode Register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear Byte Pointer Flip/Flop
1	1	0	1	0	1	Read Temporary Register
1	1	0	1	1	0	Master Clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Clear Mask Register
1	1	1	1	0	1	Illegal
1	1	1	1	1	0	Write All Mask Register Bits

Figure 6. Software Command Codes

Channel	Register	Operation	Signals							Internal Flip-Flop	Data Bus DB0–DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0–A7
			0	1	0	0	0	0	0	1	A8–A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0–A7
			0	0	1	0	0	0	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0–W7
			0	1	0	0	0	0	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0–W7
			0	0	1	0	0	0	1	1	W8–W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0–A7
			0	1	0	0	0	1	0	1	A8–A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0–A7
			0	0	1	0	0	1	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0–W7
			0	1	0	0	0	1	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0–W7
			0	0	1	0	0	1	1	1	W8–W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0–A7
			0	1	0	0	1	0	0	1	A8–A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0–A7
			0	0	1	0	1	0	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0–W7
			0	1	0	0	1	0	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0–W7
			0	0	1	0	1	0	1	1	W8–W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0–A7
			0	1	0	0	1	1	0	1	A8–A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0–A7
			0	0	1	0	1	1	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0–W7
			0	1	0	0	1	1	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0–W7
			0	0	1	0	1	1	1	1	W8–W15

Figure 7. Word Count and Address Register Command Codes

PROGRAMMING

The 8237A will accept programming from the host processor any time that HLDA is inactive; this is true even if HRQ is active. The responsibility of the host is to assure that programming and HLDA are mutually exclusive. Note that a problem can occur if a DMA request occurs, on an unmasked channel while the 8237A is being programmed. For instance, the CPU may be starting to reprogram the two byte Address register of channel 1 when channel 1 receives a DMA request. If the 8237A is enabled (bit 2 in the command register is 0) and channel 1 is unmasked, a DMA service will occur after only one byte of the Address register has been reprogrammed. This can be avoided by disabling the controller (setting bit 2 in the command register) or masking the channel before programming any other registers. Once the programming is complete, the controller can be enabled/unmasked.

After power-up it is suggested that all internal locations, especially the Mode registers, be loaded with some valid value. This should be done even if some channels are unused. An invalid mode may force all control signals to go active at the same time.

APPLICATION INFORMATION (Note 1)

Figure 8 shows a convenient method for configuring a DMA system with the 8237A controller and an 8080A/8085AH microprocessor system. The multimode DMA controller issues a HRQ to the processor whenever there is at least one valid DMA request from a peripheral device. When the processor replies with a HLDA signal, the 8237A takes control of the address bus, the data bus and the control bus. The address for the first transfer operation comes out in two bytes—the least significant 8 bits on the eight address outputs and the most significant 8 bits on the data bus. The contents of the data bus are then latched into an 8-bit latch to complete the full 16 bits of the address bus. The 8282 is a high speed, 8-bit, three-state latch in a 20-pin package. After the initial transfer takes place, the latch is updated only after a carry or borrow is generated in the least significant address byte. Four DMA channels are provided when one 8237A is used.

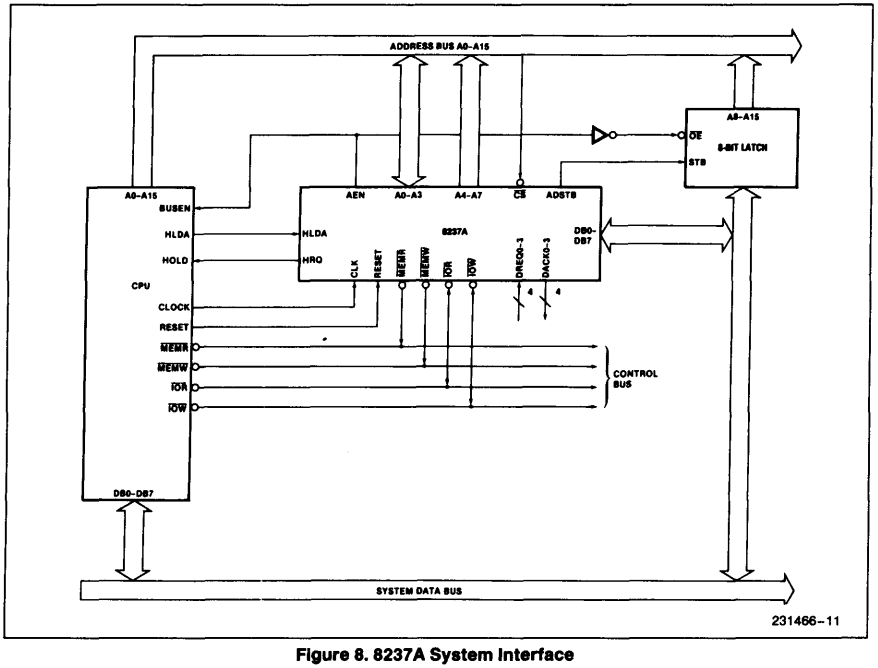


Figure 8. 8237A System Interface

NOTE:
1. See Application Note AP-67 for 8086 design information.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias .....0°C to 70°C
Case Temperature .....0°C to +75°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin with Respect to Ground.....−0.5V to +7V
Power Dissipation.....1.5 Watt

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, T_{CASE} = 0°C to 75°C, V_{CC} = +5.0V ±5%, GND = 0V

Symbol	Parameter	Min	Typ (Note 1)	Max	Unit	Test Conditions
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −200 μA
		3.3			V	I_{OH} = −100 μA (HRQ Only)
V_{OL}	Output LOW Voltage			0.40	V	I_{OL} = 3.2 mA
V_{IH}	Input HIGH Voltage	2.0		V_{CC} + 0.5	V	
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
I_{LI}	Input Load Current			±10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current			±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current		110	130	mA	T_A = +25°C
			130	150	mA	T_A = 0°C
C_O	Output Capacitance		4	8	pF	fc = 1.0 MHz, Inputs = 0V
C_I	Input Capacitance		8	15	pF	
C_{IO}	I/O Capacitance		10	18	pF	

NOTE:
1. Typical values are for T_A = 25°C, nominal supply voltage and nominal processing parameters.

A.C. CHARACTERISTICS—DMA (MASTER) MODE

T_A = 0°C to 70°C, T_{CASE} = 0°C to 75°C, V_{CC} = +5V ±5%, GND = 0V

Symbol	Parameter	8237A		8237A-4		8237A-5		Unit
		Min	Max	Min	Max	Min	Max	
TAEL	AEN HIGH from CLK LOW (S1) Delay Time		300		225		200	ns
TAET	AEN LOW from CLK HIGH (SI) Delay Time		200		150		130	ns
TAFAB	ADR Active to Float Delay from CLK HIGH		150		120		90	ns
TAFC	$\overline{READ}$ or $\overline{WRITE}$ Float from CLK HIGH		150		120		120	ns
TAFDB	DB Active to Float Delay from CLK HIGH		250		190		170	ns
TAHR	ADR from $\overline{READ}$ HIGH Hold Time	TCY-100		TCY-100		TCY-100		ns
TAHS	DB from ADSTB LOW Hold Time	40		40		30		ns
TAHW	ADR from $\overline{WRITE}$ HIGH Hold Time	TCY-50		TCY-50		TCY-50		ns
TAK	DACK Valid from CLK LOW Delay Time (Note 1)		250		220		170	ns
	$\overline{EOP}$ HIGH from CLK HIGH Delay Time (Note 2)		250		190		170	ns
	$\overline{EOP}$ LOW from CLK HIGH Delay Time		250		190		170	ns
TASM	ADR Stable from CLK HIGH		250		190		170	ns
TASS	DB to ADSTB LOW Setup Time	100		100		100		ns
TCH	Clock High Time (Transitions ≤ 10 ns)	120		100		80		ns
TCL	Clock LOW Time (Transitions ≤ 10 ns)	150		110		68		ns
TCY	CLK Cycle Time	320		250		200		ns
TDCL	CLK HIGH to $\overline{READ}$ or $\overline{WRITE}$ LOW Delay (Note 3)		270		200		190	ns
TDCTR	$\overline{READ}$ HIGH from CLK HIGH (S4) Delay Time (Note 3)		270		210		190	ns
TDCTW	$\overline{WRITE}$ HIGH from CLK HIGH (S4) Delay Time (Note 3)		200		150		130	ns
TDQ1	HRQ Valid from CLK HIGH Delay Time (Note 4)		160		120		120	ns
TDQ2			250		190		120	ns
TEPS	$\overline{EOP}$ LOW from CLK LOW Setup Time	60		45		40		ns
TEPW	$\overline{EOP}$ Pulse Width	300		225		220		ns
TFAAB	ADR Float to Active Delay from CLK HIGH		250		190		170	ns
TFAC	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK HIGH		200		150		150	ns
TFADB	DB Float to Active Delay from CLK HIGH		300		225		200	ns
THS	HLDA Valid to CLK HIGH Setup Time	100		75		75		ns
TIDH	Input Data from $\overline{MEMR}$ HIGH Hold Time	0		0		0		ns
TIDS	Input Data to $\overline{MEMR}$ HIGH Setup Time	250		190		170		ns
TODH	Output Data from $\overline{MEMW}$ HIGH Hold Time	20		20		10		ns
TODV	Output Data Valid to $\overline{MEMW}$ HIGH	200		125		125		ns
TQS	DREQ to CLK LOW (SI, S4) Setup Time (Note 1)	0		0		0		ns
TRH	CLK to READY LOW Hold Time	20		20		20		ns
TRS	READY to CLK LOW Setup Time	100		60		60		ns
TSTL	ADSTB HIGH from CLK HIGH Delay Time		200		150		130	ns
TSTT	ADSTB LOW from CLK HIGH Delay Time		140		110		90	ns

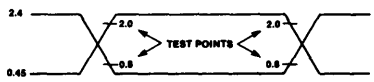
A.C. CHARACTERISTICS—PERIPHERAL (SLAVE) MODE

T_A = 0°C to 70°C, T_{CASE} = 0°C to 75°C, V_{CC} = +5V ±5%, GND = 0V

Symbol	Parameter	8237A		8237A-4		8237A-5		Unit
		Min	Max	Min	Max	Min	Max	
TAR	ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	50		50		50		ns
TAW	ADR Valid to $\overline{WRITE}$ HIGH Setup Time	200		150		130		ns
TCW	CS LOW to $\overline{WRITE}$ HIGH Setup Time	200		150		130		ns
TDW	Data Valid to $\overline{WRITE}$ HIGH Setup Time	200		150		130		ns
TRA	ADR or CS Hold from $\overline{READ}$ HIGH	0		0		0		ns
TRDE	Data Access from $\overline{READ}$ LOW (Note 5)		200		200		140	ns
TRDF	DB Float Delay from $\overline{READ}$ HIGH	20	100	20	100	0	70	ns
TRSTD	Power Supply HIGH to RESET LOW Setup Time	500		500		500		ns
TRSTS	RESET to First $\overline{IOWR}$	2TCY		2TCY		2TCY		ns
TRSTW	RESET Pulse Width	300		300		300		ns
TRW	$\overline{READ}$ Width	300		250		200		ns
TWA	ADR from $\overline{WRITE}$ HIGH Hold Time	20		20		20		ns
TWC	CS HIGH from $\overline{WRITE}$ HIGH Hold Time	20		20		20		ns
TWD	Data from $\overline{WRITE}$ HIGH Hold Time	30		30		30		ns
TWWS	Write Width	200		200		160		ns
TWR	End of Write to End of Read in DMA Transfer	0		0		0		ns

NOTES:
1. DREQ and DACK signals may be active high or active low. Timing diagrams assume the active high mode.
2. $\overline{EOP}$ is an open collector output. This parameter assumes the presence of a 2.2K pullup to V_{CC}.
3. The net $\overline{IOW}$ or $\overline{MEMW}$ Pulse width for normal write will be TCY−100 ns and for extended write will be 2TCY−100 ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be 2TCY−50 ns and for compressed read will be TCY−50 ns.
4. TDQ is specified for two different output HIGH levels. TDQ1 is measured at 2.0V. TDQ2 is measured at 3.3V. The value for TDQ2 assumes an external 3.3 KΩ pull-up resistor connected from HRQ to V_{CC}.
5. Output Loading on the Data Bus is 1 TTL Gate plus 100 pF capacitance.

A.C. TESTING INPUT/OUTPUT WAVEFORM

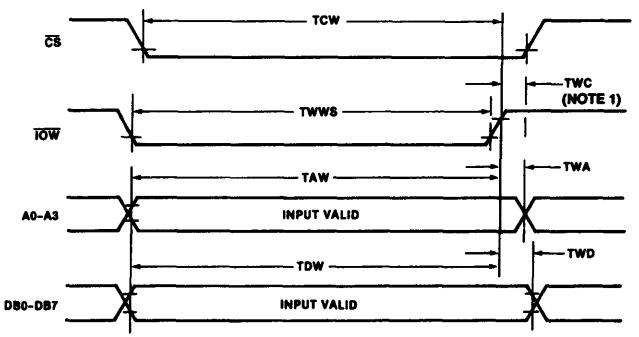


231466-12

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0." Input timing parameters assume transition times of 20 ns or less. Waveform measurement points for both input and output signals are 2.0V for HIGH and 0.8V for LOW, unless otherwise noted.

WAVEFORMS

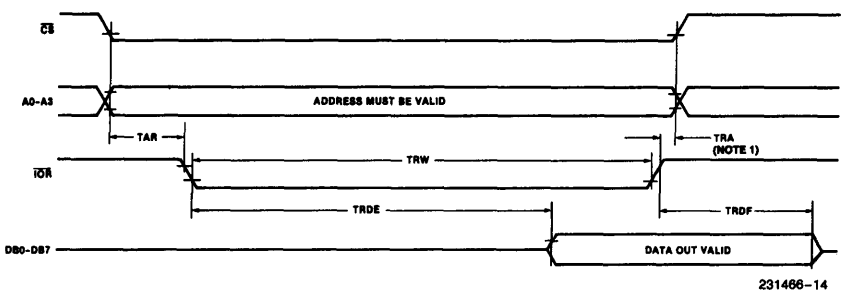
SLAVE MODE WRITE TIMING



NOTE:
1. Successive read and/or write operations by the external processor to program or examine the controller must be timed to allow at least 600 ns for the 8237A, at least 500 ns for the 8237A-4, and at least 400 ns for the 8237A-5 as recovery time between active read or write pulses. The same recovery time is needed between an active read or write pulse followed by a DMA transfer.

Figure 9. Slave Mode Write

SLAVE MODE READ TIMING

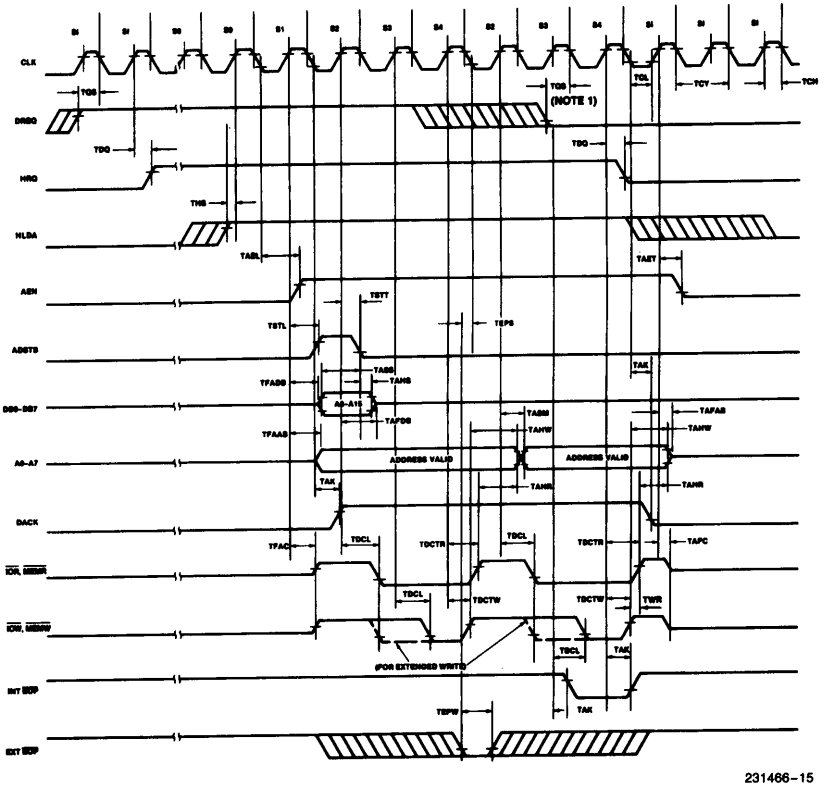


NOTE:
1. Successive read and/or write operations by the external processor to program or examine the controller must be timed to allow at least 600 ns for the 8237A, at least 500 ns for the 8237A-4, and at least 400 ns for the 8237A-5 as recovery time between active read or write pulses. The same recovery time is needed between an active read or write pulse followed by a DMA transfer.

Figure 10. Slave Mode Read

WAVEFORMS (Continued)

DMA TRANSFER TIMING



231466-15

NOTE:
1. DREQ should be held active until DACK is returned.

Figure 11. DMA Transfer

WAVEFORMS (Continued)

MEMORY-TO-MEMORY TRANSFER TIMING

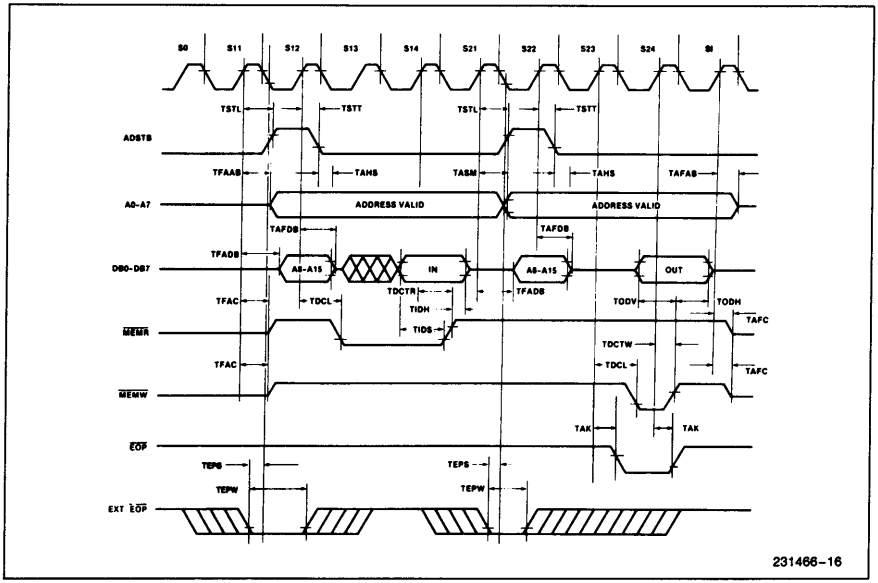


Figure 12. Memory-to-Memory Transfer

READY TIMING

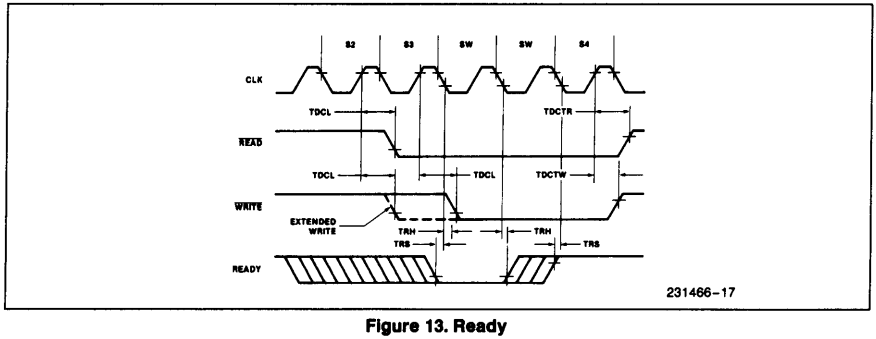


Figure 13. Ready

WAVEFORMS (Continued)

COMPRESSED TRANSFER TIMING

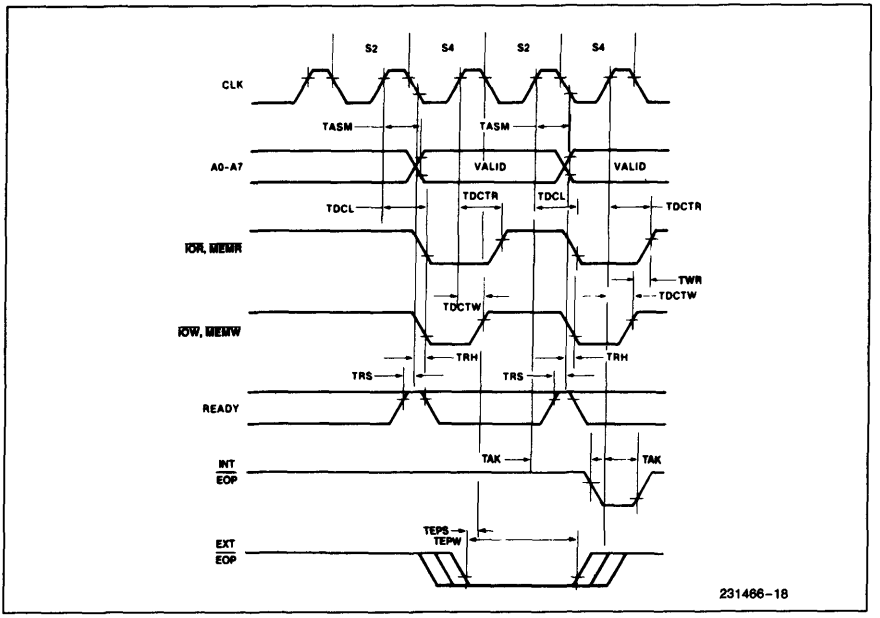


Figure 14. Compressed Transfer

RESET TIMING

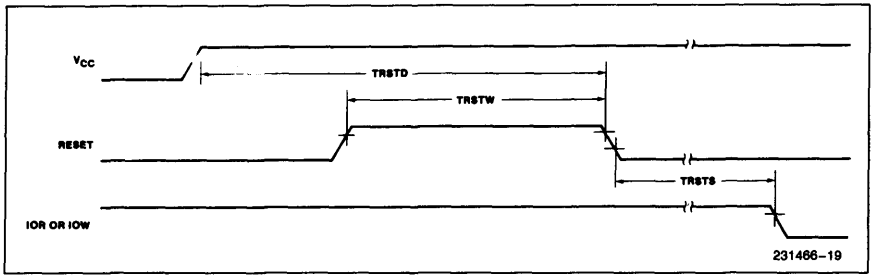


Figure 15. Reset

DESIGN CONSIDERATIONS

1. ***Cascading from channel zero.*** When using multiple 8237s, always start cascading with channel zero. Channel zero of the 8237 will operate incorrectly if one or more of channels 1, 2, or 3 are used in the cascade mode while channel zero is used in a mode other than cascade.
2. ***Do not treat the DREQ signal as an asynchronous input while the channel is in the "demand" or "cascade" modes.*** If DREQ becomes inactive at any time during state S4, an illegal state may occur causing the 8237 to operate improperly.
3. ***HRQ must remain active until HLDA becomes active.*** If HRQ goes inactive before HLDA is received the 8237 can enter an illegal state causing it to operate improperly.
4. ***Make sure the MEMR# line has 50 pF loading capacitance on it.*** When doing memory to memory transfers, the 8237 requires at least 50 pF loading capacitance on the MEMR# signal for proper operation. In most cases board capacitance is sufficient.
5. ***Treat the READY input as a synchronous input.*** If a transition occurs during the setup/hold window, erratic operation may result.

DATA SHEET REVISION REVIEW

The following list represents key differences between this and the -002 data sheet. Please review this summary carefully.

1. Major cleanup on the "NOTE" sections of this data sheet.
   a. Pin 5 no longer references a note. It is now included in the pin description area under the name "PIN5".
   b. The note placed in the "typical" section of the D.C. Characteristics table is now referenced to a note section included with that table.
   c. Notes in the A.C. Characteristics table have been renumbered and are included in a notes section for the A.C. Characteristics.
   d. The note that was previously referenced in the A.C. TESTING INPUT/OUTPUT WAVEFORM diagram has been replaced with the actual note.
   e. The note that was previously referenced in the SLAVE MODE WRITE TIMING diagram has been included in a "NOTE" section with the diagram.
   f. The note that was previously referenced in the SLAVE MODE READ TIMING diagram has been included in a "NOTE" section with the diagram.
   g. The note that was previously referenced in the DMA TRANSFER TIMING diagram has been included in a "NOTE" section with the diagram.
2. A "Design Considerations" section was added to alert designers to certain design aspects of the 8237.
3. The timing parameters TAR for the 8237A-4 and 8237A-5 have been changed from 50 ns to 0 ns.

KFIT CUSTOM CHIP

(KEYBOARD, FLOPPY SUPPORT, INTERRUPT, TIMER)

Tandy Corporation
1000 Two Tandy Center
Fort Worth, Tx 76102

TANDY PART #: 8079019

Table Of Contents

FUNCTIONAL DESCRIPTIONS

This Tandy KFIT custom IC consists of the following functional blocks:

- Programmable Peripheral Interface (PPI)
- Keyboard Interface Logic
- Floppy Disk Interface Logic
- Programmable Interrupt (equivalent to Intel 8259A) and sharing interrupt logic
- Programmable Timer (equivalent to Intel 8254-2 and Clock Divider
- Address Decoding Logic

Programmable Peripheral Interface

This section of the KFIT custom integrated circuit replaces the Intel 8255A that was used on the original Tandy 1000 computer. On the block diagram for this section of logic, the 8255A is represented by three 74LS244 buffers addressed by read A (0060), read B (0061), read C (0062). Also the two latches addressed by write B (0061), write C (0062) which are part of the original 8255A logic.

Keyboard Interface Logic

This section of the KFIT custom integrated circuit is design to support Tandy 1000 keyboard or Tandy 101 enhanced keyboard. KYBDTYP signal is used to select Tandy 1000 keyboard when is LOW or Tandy 101 enhanced keyboard when is HIGH. The KYBDTYP is being read in to port FFEB(hex) bit 7. The KBDDATA - keyboard data is serial data bit stream and then is converted to 8 bits parallel data by 74LS322. The serial data is entered in the LOW to HIGH transition of the KBCLK.

Floppy Disk Interface Logic

This section of the KFIT custom integrated circuit is design to support Floppy Disk Digital Output Register (DOR) function. This register is mapped in address 03F2 hex - data bit 0 to 7 (write only) to generate drive select DS0B,DS1B,DS2B; FDCRST (FDC reset) DMA/I and MTRONB (motor ON) signal. The DMA/I signal is used to disable FDCINTI, FDCDMRQ, and FDACKI signals for allowing the used of external FDC controller.

Programmable Interval Timer

This section of the KFIT custom integrated circuit is equivalent to an Intel 8254-5 and is designed to use with the Tandy 1000 TX. It is organized as three independent 16-bit counters, each with a clock of 1.19 MHZ. The 1.19 MHZ clock is generated from 14MHZ divided by 12. All modes of operation are software programmable.

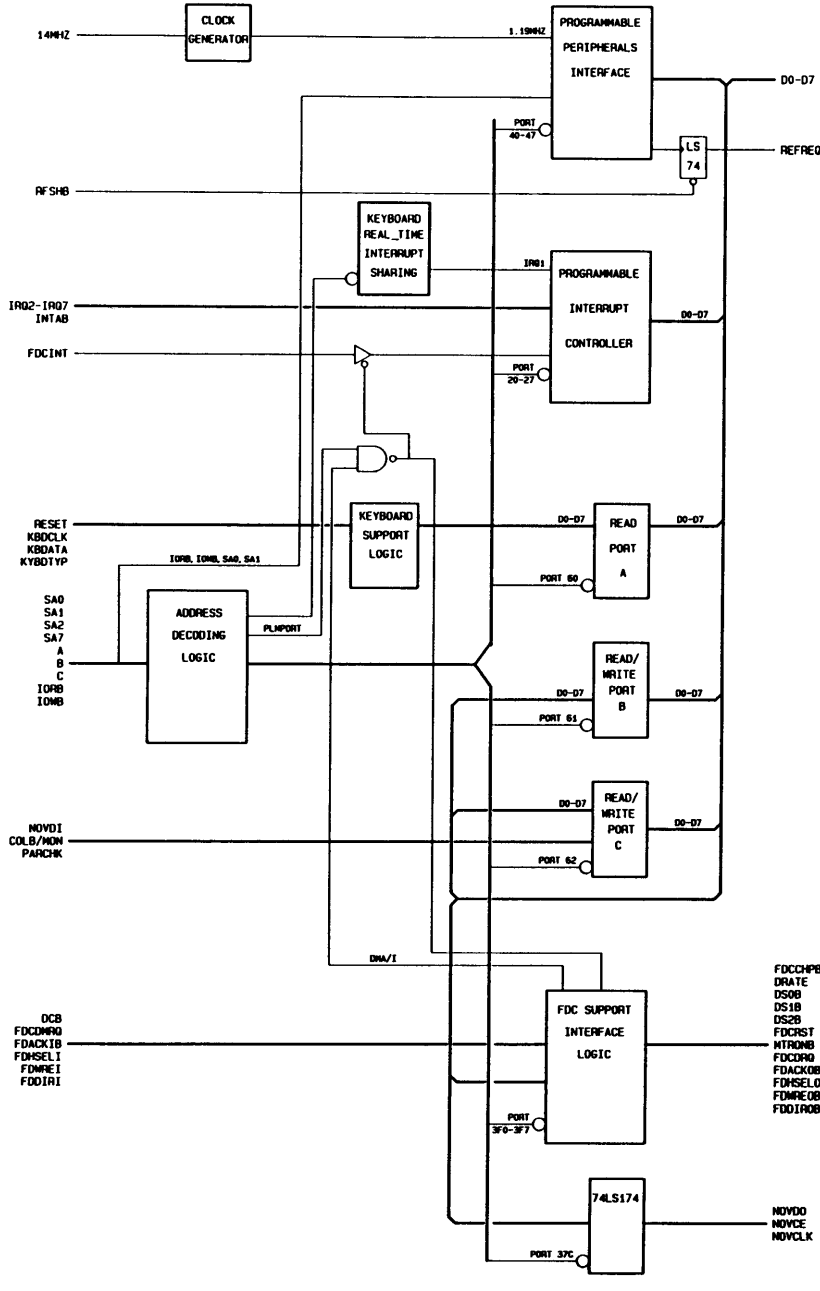
Programmable Interrupt

This section of the KTIF custom integrated circuit is equivalent to an Intel 8259A that capable of handling eight-vector priority interrupt, individual request mask and programmable interrupt modes. This circuit generates INTR output signal for the CPU. In addition, the sharing interrupt logics are implemented in the design for IRQ1 (between keyboard and real time clock interrupt)

Address Decoding Logic

This section contains 3 to 8 address decode to generate Programmable Interrupt Chip select, Programmable Interval Timer chip select, Floppy Disk chip select (FDCCHP*) and Programmable Peripheral Interface address of three decoded address A, B and C. (see IO signal definition). The FDC port is enabled by Planar register-port 0065hex bit 3 when bit 3 is HIGH.

BLOCK DIAGRAM



INPUT/OUTPUT PIN DESCRIPTIONS

#	Signal	Output Current	Pin Number	Type	Descriptions
1	XD0 (S.T input)	8ma	14	I/O	Data bus 0
2	XD1 (S.T input)	8ma	15	I/O	Data bus 1
3	XD2 (S.T input)	8ma	16	I/O	Data bus 2
4	XD3 (S.T input)	8ma	17	I/O	Data bus 3
5	XD4 (S.T input)	8ma	19	I/O	Data bus 4
6	XD5 (S.T input)	8ma	20	I/O	Data bus 5
7	XD6 (S.T input)	8ma	21	I/O	Data bus 6
8	XD7 (S.T input)	8ma	22	I/O	Data bus 07
9	SA0		28	I	System address 0
10	SA1		29	I	System address 1
11	SA2		30	I	System address 2
12	SA7		31	I	System address 7
13	A		32	I	CPU I/O address decode LSB
14	B		33	I	CPU I/O address decode
15	C		34	I	CPU I/O address decode MSB
16	IOWB		37	I	Active LOW. CPU I/O write signal
17	IORB		36	I	Active LOW. CPU I/O read signal

#	Signal	Output Current	Pin Number	Type	Descriptions
18	14MHZ		27	I	Clock signal 14.318 MHZ
19	BUSY (O.C., Pull_up)*	8ma	58	O	Keyboard busy When High
20	KYBDTYP (Pull-up)		61	I	Keyboard type select. When High, selects IBM PC keyboard. When Low selects Tandy keyboard
21	PPITM	2ma	12	O	Programmable Peripheral Interface Timer output signal for sound generator.
22	KBDDATA (3-state)	8ma	60	I/O	Input data signal from keyboard. In the IBM PC keyboard this pin is used as an output to hold the data Low.
23	KBDCLK (3-state)	8ma	59	I/O	Input clock signal from keyboard. In the IBM PC keyboard this pin is used as an output to hold the clock LOW.
24	DS0B (O.C. Pull_up*)	8ma	57	O	Drive select signal When Low.
25	DS1B (O.C. Pull_up*)	8ma	56	O	Drive select signal when is LOW.
26	DS2B (O.C. Pull_up*)	8ma	55	O	Drive select signal when is LOW.
27	DCB (Pull_up)		38	I	Disk change signal when is LOW.

#	Signal	Output Current	Pin Number	Type	Descriptions
28	DRATE (O.C.)	16ma	54	O	Data rate select signal. When is LOW, 500 kbps is selected. When is HIGH 250kbps is selected.
29	FDCRST	4ma	46	O	FDC reset signal to the FDC controller when is HIGH.
30	RESET		66	I	System reset input signal when is HIGH.
31	MTRONB (O.C.)	16ma	53	O	Floppy disk motor ON output signal when is LOW.
32	FDHSELI		42	I	Head select input signal from floppy disk controller.
33	FDHSELOB (O.C.)	16ma	49	O	Head select input signal for floppy drives when is LOW.
34	FDWREI		41	I	Write enable input signal from floppy disk controller.
35	FDWREOB (O.C.)	16ma	50	O	Write enable output signal for floppy drives when is LOW.
36	FDDIRI		40	I	Head travel direction input signal from FDC controller.
37	FDDIROB (O.C.)	16ma	51	O	Head travel direction for floppy drive.
38	FDCCHPB	4ma	47	O	FDC chip select output signal or FDC controller when is LOW.

#	Signal	Output Current	Pin Number	Type	Descriptions
39	FDACKIB		44	I	FDC controller acknowledge output signal when is LOW.
40	FDACKOB	2ma	45	O	FDC controller acknowledge output signal when is LOW.
41	FDCINT		39	I	Floppy disk interrupt input signal when is HIGH.
42	FDCDMRQ		43	I	Floppy disk service request input signal to DMA when is LOW.
43	FDCDRQ	4ma	48	O	Floppy disk service request output signal to the DMA when is LOW.
44	IRQ2 (S.T. Pull_up)		5	I	Interrupt request 2 input signal
45	IRQ3 (S.T. Pull_up)		6	I	Interrupt request 3 input signal
46	IRQ4 (S.T. Pull_up)		7	I	Interrupt request 4 input signal
47	IRQ5 (S.T. Pull_up)		8	I	Interrupt request 5 input signal
48	IRQ6 (3-state, Pull_up)		10	I	Interrupt request 6 input/output signal
49	IRQ7 (S.T. Pull_up)		9	I	Interrupt request 7 input signal

#	Signal	Output Current	Pin Number	Type	Descriptions
50	INTAB		4	I	Interrupt acknowledge signal. This signal is used to enable interrupt vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU
51	INTR	2ma	11	O	Interrupt request signal. This signal is used to interrupt the CPU when HIGH
52	RTCINTB (S.T. Pull_up)		2	I	Real time clock interrupt signal from the Real Time Clock device when LOW.
53	NOVDI		26	I	NOV_RAM data in signal
54	NOVCE	2ma	23	O	NOV_RAM chip enable signal
55	NOVDO	2ma	25	O	NOV_RAM data out signal
56	NOVCK	2ma	24	O	NOV_RAM clock
57	RFRSHB		3	I	DMA acknowledge signal from 8237. This signal is active HIGH
58	REFREQ	2ma	13	O	DMA Request signal for 8237. This signal is active HIGH
59	COL/MON		68	I	Input configuration control signal
60	PARCHK		67	I	Parity Check input signal

#	Signal	Output Current	Pin Number	Type	Descriptions
61	VCC		1		Power supply +5V
62	VCC		35		Power supply +5V
63	GND		52		Ground
64	GND		18		Ground
65	not used		62		
66	not used		63		
67	not used		64		
68	not used		65		

Notes:- O.C. = Open_Collector
- 3-State = Tri_State
- S.T. = Schmitt Trigger
- * = Max.=1.6ma, Min.=0.4ma sinking current.
These signals must have external termination.

I/O MAPS

I/O Signal Definition:

C	B	A	Address Range Hex	Function
0	0	0	0020 - 0027	Interrupts
0	0	1	0040 - 0047	Timer
			00C0 - 00C7	Sound
0	1	0	0060 - 0067	PPI
			0065	Planar Register
0	1	1	03F0 - 03F7	Floppy
1	0	0	0200 - 0207	Joystick
1	0	1	0378 - 037F	Printer
			037C	NOVRAM
			03F8 - 03FF	Serial
1	1	0	FFE8 - FFEF	Non IBM compatible
1	1	1	----------	Inactive

Register Definition:

Address Range Hex	Bit	Description
Interrupt		
0020	~	Initialization Command Word 1
0021	~	Initialization Command Word 2
0022 - 0027		Not used
Timer		
0040/0044	~	Timer
0041/0045	~	Timer
0042/0047	~	Timer

Note: ~ = refers to system I/O maps.

PPI/Keyboard

Address Range Hex	Bit	Description
0060 - Port A		Keyboard Read Data Input
	0	Read only Keyboard bit 0 LSB
	1	Read only Keyboard bit 1
	2	Read only Keyboard bit 2
	3	Read only Keyboard bit 3
	4	Read only Keyboard bit 4
	5	Read only Keyboard bit 5
	6	Read only Keyboard bit 6
	7	Read only Keyboard bit 7 MSB
0061 - Port B		Read/Write
	0	R/W Timer gate #2 enable
	1	R/W Speaker data out enable
	2	R/W not used
	3	R/w not used
	4	R/W 1=disable internal speaker
	5	R/W not used
	6	R/W HOLDCK
	7	R/W 1=keyboard clear

Address Range Hex	Bit	Description
0062 - Port C		Read/Write
	0	R/W not used
	1	R/W not used
	2	R/W not used
	3	R/W 0=slow speed
	4	Read NOVDI
	5	Read output Timer #2
	6	Read 0=color
	7	Read 1=Parity check
0063-0064		Port not used

Planar Control

0065		Planar Register Read/Write
	0	Reserved
	1	Reserved
	2	Reserved
	3	1=FDC chip select enable
	4	Reserved
	5	Reserved
	6	Reserved
	7	Reserved
0066		Not Used
0067		Port D not used

Non Volatile Memory Access

037C		Non-volatile memory write only
	0	NOVDO
	1	NOVCE
	2	NOVCLK
	3	Reserved
	4	Reserved
	5	Reserved
	6	Reserved
	7	Reserved

Floppy Disk Control

Address Range Hex	Bit	Description
03F0		Not used
03F1		FDC Mode Control
	0	Not used
	1	Write - Drive Select switch 0 = 0-0 1-1 1 = 0-1 1-0
	2	Not used
	3	Not used
	4	Not used
	5	Not used
	6	Not used
	7	Not used
03F2		FDC Digital Output Register (DOR) Write Only
		DS0 DS1 DS2
	0	Write - 0 1 0
	1	Write - 0 0 1
	2	Write - FDC reset
	3	Write - Enable DMA Req/Int.
	4	Write - Drive 0 Motor ON
	5	Write - Drive 1 Motor ON
	6	Not used
	7	Not used
03F3		Not used
03F4		FDC chip select
03F5		FDC chip select
03F6		Not used
03F7		FDC Data Rate Selection
	0	Not used
	1	Write - Data Rate 0 = 500K bits per second 1 = 250K bits per second
	2	Not used
	3	Not used
	4	Not used
	5	Not used
	6	Not used
	7	0=Disk Change

System Configuration Register

FFEB		Non IBM Compatible Read/Write
	0	Reserved
	1	Reserved
	2	Reserved
	3	Reserved
	4	Reserved
	5	Read 1=Keyboard Interrupt
	6	Read 1=Real Time Clock Interrupt Write 1=Enable Real-Time clock Interrupt
	7	Read Keyboard Select 0=Tandy Keyboard 1=101 Enhanced Keyboard

Summary on the active/float data bits. (READ ONLY)

Address	Net Name	Active Bits	Float Bits
0065	CSEN	XD3	XD0-XD2, XD4-XD7
03F7	FDMDRDB	XD7	XD0-XD6
FFEB	CDENRDB	XD5	XD0-XD4
		XD6	
		XD7	

ELECTRICAL SPECIFICATIONS

Absolute Maximum Rating

Parameter	Min.	Typ.	Max.	Unit	Condition
Voltage, any pin	-0.5		7.0	V	W.R.T gnd
Power Dissipation					

D.C. Electrical Characteristics at Ta= 0 to 70 degree Celsius

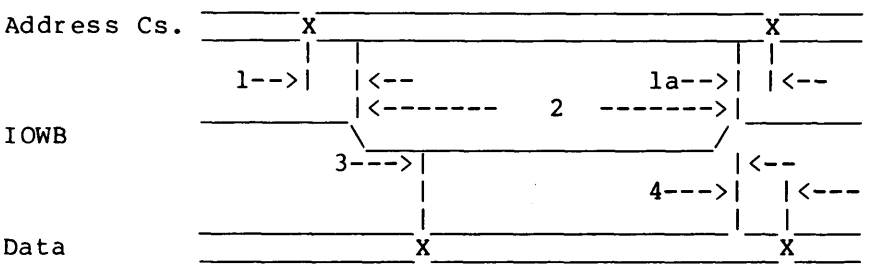
SYM.	Parameter	Min.	Typ.	Max.	Unit	Condition
Vdd	Supply Voltage	4.5		5.5	V	
Vil	Input Low Voltage			0.8	V	TTL input
Vih	Input High Voltage	2.0			V	TTL input
Iin	Input Leakage Current	-10		10	UA	
Cin	Input Capacitance			10	PF	
Vol	Output Low Voltage Unless otherwise specified in I/O Pin Descriptions			0.4	V	2MA
Voh	Output High Voltage Unless otherwise specified in I/O Pin Descriptions	2.4			V	-2MA
Ioz	High Impedance leak	-10		10	UA	
Voh(INTR)	Output High	3.5			V	@ -100ua
	Voltage for INTR	2.4			V	@ -400ua
Zo	Output Capacitance					
	XD0 - XD7	100			PF	Note A

Notes: A. 50 PF is used in manufacture test.

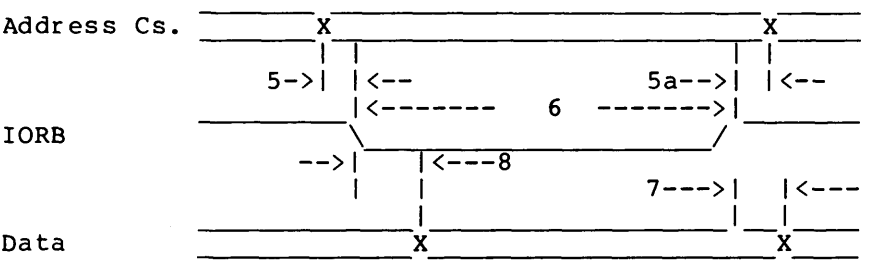
KEYBOARD TIMING SPECIFICATIONS

NUM.	Parameter	Min.	Typ.	Max	Unit	
1	Address valid to IOWB active	15			ns	
1a	Address hold from IOWB Inactive	20			ns	
2	IOWB pulse width	125			ns	
3	Data setup from IOWB Inactive	65			ns	Write
4	Data hold from IOWB Inactive	30			ns	Write
5	Address valid to IORB active	15			ns	
5a	Address hold from IORB inactive	30			ns	Read
6	IORB pulse width	120			ns	
7	Data hold/release from IORB inactive	5		55	ns	Read
8	Data access time			100	ns	Read

I/O Write Cycle



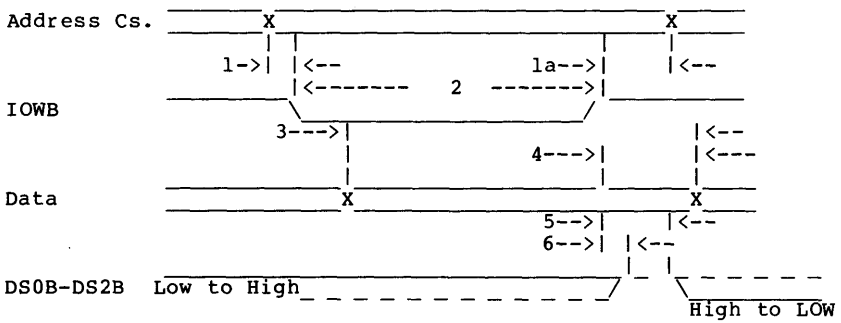
I/O Read Cycle



FLOPPY DISK TIMING SPECIFICATIONS:

NUM.	Parameter	Min.	Typ.	Max	Unit	
1	Address setup from IOWB active	15			ns	
1a	Address hold from IOWB Inactive	20			ns	
2	IOWB pulse width	125			ns	
3	Data setup from IOWB inactive	65			ns	
4	Data hold from IOWB inactive	30			ns	
5	DS0B-DS2B,FDCRST, MTRONB inactive delay from IOWB inactive			43	ns	
6	DS0B-DS2B,FDCRST, MTRONB active delay from IOWB inactive			41	ns	

I/O Write Cycle



PROGRAMMABLE INTERRUPT TIMING AND DESCRIPTIONS
Must meet Intel 8259A. Any differences must be specified.

PROGRAMMABLE TIMER TIMING AND DESCRIPTIONS
Must meet Intel 8254-5.

Any differences must be specified.

ADDRESS PORT EQUATIONS

```
/*************************************************************/
/*                                                           */
/*      KEYBOARD, TIMER CONTROL, INTERRUPT CONTROL, FDC-DOR  */
/*      AND DECODE LOGIC                                     */
/*************************************************************/
/*  Allowable Target Device Types:    F153                   */
/*************************************************************/

/**  Inputs  **/

PIN     1    =  sa01     ;    /* System address 1             */
PIN     2    =  sa00     ;    /* System address 0             */
PIN     3    =  sa02     ;    /* System address 2             */
PIN     4    =  !iow     ;    /* I/O Write                    */
PIN     5    =  !ior     ;    /* I/O Read                     */
PIN     6    =  !fdcport ;    /* FDC Port 03F0-03F8 hex       */
PIN     7    =  !keyport ;    /* Keyboard Port 0060 - 0067    */

/**  Outputs  **/

PIN     9    =  !fdmdrd  ;    /* Read FDC Port 03F7 hex       */
PIN     11   =  !fdmdwt  ;    /* Write FDC Port 03F7 hex      */
PIN     12   =  !fdcchp  ;    /* FDC Chip Select 03F4 - 03F5  */
PIN     13   =  dorltch  ;    /* Write DORLTCH Port 03F2      */
PIN     14   =  drvsck   ;    /* Write Port 03Fl DriveSwitch  */
PIN     15   =  writdp   ;    /* Write Keyboard Port 0067 or D*/
PIN     16   =  cp       ;    /* Port 0062 or C               */
PIN     17   =  bp       ;    /* Port 0061 or B               */
PIN     18   =  readap   ;    /* Read Port 0060               */
PIN     19   =  csen     ;    /* Chip Select Enable Port 0065 */

/**  Logic Equations  **/

fdmdrd = fdcport & sa02 & sa01 & sa00 & ior;

fdmdwt = fdcport & sa02 & sa01 & sa00 & iow;

fdcchp = fdcport & sa02 & !sa01;

!dorltch = fdcport & iow & !sa02 & sa01 & !sa00;

!drvsck = fdcport & iow & !sa02 & !sa01 & sa00;

!readap = keyport & ior & !sa02 & !sa01 & !sa00;

bp = keyport & !sa02 & !sa01 & sa00;

cp = keyport & !sa02 & sa01 & !sa00;

csen = keyport & sa02 & !sa01 & sa00;
```

JACKSBORO SPECIFICATION

jmp 05-26-88

Table of Contents

1.0 GENERAL

1.1 Functional Description

The PSSJ Tandy ASIC is contained in a 68 pin PLCC package, and comprises the Printer port, a Serial (RS232) port, the Sound function, and the Joystick function of the Tandy 1000 computers.

2.0 PIN LIST

PIN NAME	PIN NO.	DRIVE	DESCRIPTION
VCC	1,35	--	Power inputs
VBB	59	--	Analog Power input
GND	18,52	--	Grounds
RST	25	TTL in	System reset signal, active high.
CLK14M	2	TTL in	Clock signal input, 14.31313 MHz, 50% duty cycle.
CLK2IN	37	TTL in	Clock signal input, either 24 MHz or 1.8432 MHz, 50% duty cycle.
IOD0 - IOD7	14,15,16,17 19,20,21,22	DS1218, 8 mA TS	Eight bit peripheral data bus intended to drive 5 XT type I/O slots, as well as all on board peripherals.
IOR-	10	TTL in	CPU/DMA I/O Read signal, active low. System control line.
IOW-	11	DS1218	CPU/DMA I/O Write signal, active low. System control line.
A0 - A2, A7	6,7,8,9	TTL in	System address lines.
CS0 - CS2	3,4,5	TTL in	Address decode inputs.
PINT	12	2 mA TS	Printer Interrupt, tristate.

PIN NAME	PIN NO.	DRIVE	DESCRIPTION
SINT	13	2 mA TS	Serial Interrupt, tristate.
PPITIM	68	TTL in	Low frequency sound input.
AUDIO_IN	55	An in.	Analog audio input, 1 V p-p.
SND_OUT	57	An out	Analog audio output, 2 V p-p.
GAIN_OUT	56	An out	Analog audio output, 2 V p-p
DRQ	23	2 mA TS	Data request for DMA operations, tristate.
TC	27	TTL in	Terminal Count input.
DACK1	26	TTL in	Data acknowledge for DMA ops.
WAIT-	24	2 mA OD	Sound chip wait output, open drain.
JPOS1 - JPOS4	60,61,62,63	DS1218	Digital joystick position input.
JSW1 - JSW4	64,65,66,67	DS1218	Digital joystick switch inputs.
DAC_OUT	58	An out	Analog DAC output for external integration, comparison with joystick voltages.
PD0 - PD7	51,50,49,48 47,46,45,44	DS1218 4 mA TS	Printer data inputs/outputs.
INIT	40	4 mA OD	Printer initialization output.
AFXT-	39	4 mA OD	Printer auto feed output.
STROBE-	38	4 mA OD	Printer strobe output.
ACK-	41	TTL in	Printer acknowledge input.

PIN NAME	PIN NO.	DRIVE	DESCRIPTION
PE	43	TTL in	Printer paper empty input.
SLCTIN-	53	TTL in	Printer select input.
BUSY-	42	TTL in	Printer busy input.
FAULT-	54	TTL in	Printer fault input.
DTR-	36	2 mA	RS232 data terminal ready output.
RTS-	33	2 mA	RS232 request to send output.
TXD-	34	2 mA	RS232 transmit data output.
RI-	29	TTL in	RS232 ring indicator input.
DCD-	30	TTL in	RS232 carrier detect input.
DSR-	28	TTL in	RS232 data set ready input.
CTS-	32	TTL in	RS232 clear to send input.
RXD-	31	TTL in	RS232 receive data input.

3.0 ABSOLUTE MAXIMUM RATINGS

	Min	Typ	Max	Units
Storage Temperature:	-65		150	degrees C
Operating Temperature:	0	25	55	degrees C
All output pins	-0.5		7.0	volts DC
All input pins	-0.5		7.0	volts DC
Power Supply (Vcc)	-0.5		7.0	volts DC
Power dissipation			700	milliwatts

4.0 D. C. ELECTRICAL CHARACTERISTICS

4.1 Inputs

Leakage current	Min	Typ	Max	Units
			+/-10	uA
Vih (TTL in)	2.0		Vcc+.5	volts DC
Vih (DS1218)	2.1		Vcc+.5	volts DC
Vil	-0.5		0.8	volts DC
Input capacitance			10	pF

4.2 PD0 - PD7, INIT, /AFXT, /STROBE

	Min	Typ	Max	Units
Iol	4			mA
Vol			0.4	volts DC
Ioh	1			mA
Voh	2.4			volts DC
Capacitive load	100			pF

4.3 /WAIT

	Min	Typ	Max	Units
Iol	4			mA
Vol			0.4	volts DC
Capacitive load	100			pF

4.4 DRQ, /TXD, /DTR, /RTS, PINT, SINT

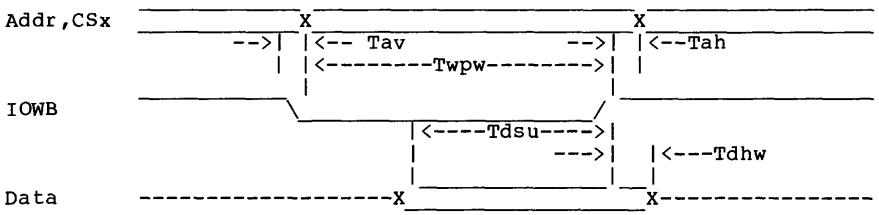
	Min	Typ	Max	Units
Iol	2			mA
Vol			0.4	volts DC
Ioh	1			mA
Voh	2.4			volts DC
Capacitive load	40			pF

4.5 IOD0 - IOD7

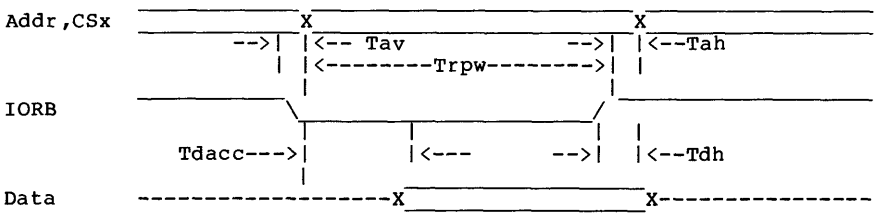
	Min	Typ	Max	Units
Iol	8			mA
Vol			0.4	volts DC
Ioh	2			mA
Voh	2.4			volts DC
Capacitive load	100			pF

5.0 AC CHARACTERISTICS

Parameter	Min	Typ	Max	Units
Tav (Address Valid)	-15			nSec
Tah (Address Hold)	30			nSec
Trpw (Read Pulse Width)	120			nSec
Twpw (Write Pulse Width)	125			nSec
Tdsu (Data Setup (Write))	65			nSec
Tdacc (Data Access (Read))			100	nSec
Tdhr (Data Hold (Read))	10		30	nSec
Tdhw (Data Hold (Write))	25			nSec



I/O Write Cycle



I/O Read Cycle

6.0 Modifications to the 76496

6.1 Extra Bit of Division by each channel.

When clocked by a 3.579545 MHz signal, the lowest frequency generated by the 76496 (with its 10 bit dividers) is 109.24 Hz. It is desired to be able to generate lower frequencies. An extra bit of division will allow frequencies down to 54.62 Hz, or an octave lower than the lowest note currently available. Since there is an extra bit in the frequency update register (second byte), it makes sense to implement this feature here. However, to maintain backwards compatibility, since it is not known what is programmed in this bit, there needs to be a way of defeating the extra bit of division. Therefore, there is a signal (SEDE), which enables the extra bit for all three channels. This bit defaults to a logic zero (low) on reset. When it is set, by writing to port C4 with bit 6 high, the extra divider will be enabled.

6.2 Synchronization of frequency dividers.

The current 76496 design loads each divider when initially written to, with no provision for synchronization of the dividers. This is a handicap when programming frequencies of low integer relationships to each other, because it is not possible to guarantee the phase of the signals. Therefore, if synchronization is desired, it is enabled by writing to port C4, with bit 5 set (which defaults to reset). When this bit is high, any write to a frequency register of the new sound channel will not only load its divider, but reload the dividers in the present 76496.

6.3 Minimum Wait State Generation

The 32 wait states generated by the 76496 need to be reduced. The chip must be guaranteed to latch the data written in the same time allotted for the 8250A megacell. Any wait states generated should only apply to a successive write (not the first in a series). All write timing should be referenced to the rising edge of the IOW- strobe.

7.0 Software Specification

Port C0 - C3 Write

Access 76496 megacell

Port	R/W	7	6	5	4	3	2	1	0
C4	W	(res)	SEDE	SDSE	DIEN	DICL-	DMAEN	DF1	DF0

Where:

DF1	DF0	=	Dac Function Select
0	0	=	Joystick
0	1	=	Sound Channel
1	0	=	Successive Approximation
1	1	=	Direct write to DAC
DMAEN		=	DMA Enable (for SA, direct R/W)
0		=	DMA Disabled
1		=	DMA Enabled for SA, DA
DICL-		=	DMA interrupt clear
0		=	DMA interrupt held clear
1		=	DMA interrupt allowed
DIEN		=	DMA Interrupt enable
0		=	DMA EOP interrupt disabled
1		=	DMA EOP interrupt enabled
SDSE		=	Sound Divider Sync Enable
0		=	Synchronization Disabled
1		=	Sync Enabled: Write to C6 or C7 reloads all dividers
SEDE		=	Sound Chip Extra Divide Enable
0		=	Extra Divide disabled
1		=	Extra Divide enabled
(res)		=	reserved

Port C4 Read

[Readback all bits except bit 3. In addition:]

bit 7	=	SAD-	=	Successive Approximation done. Useful when polling instead of DMA for successive approximation.
bit 3	=	DIO	=	DMA interrupt has occurred. To clear the interrupt it is necessary bring DICL low, then back high.

Port C5 Write

Direct write to DAC (DF1,0 = 11 bin).
Pulse width and waveshape (DF1,0 = 01 bin).

7	6	5	4	3	2	1	0
WS1	WS0	(res)	(res)	= (res)	PW2	PW1	PW0

Where:

WS1	WS0	=	Waveshape select bits
0	0	=	Pulse
0	1	=	Ramp
1	0	=	Triangle
1	1	=	Reserved

PW2	PW1	PW0	=	
0	0	0	=	6.25% duty cycle
0	0	1	=	12.5% duty cycle
0	1	0	=	18.75% duty cycle
0	1	1	=	25.0% duty cycle
1	0	0	=	31.25% duty cycle
1	0	1	=	37.5% duty cycle
1	1	0	=	43.75% duty cycle
1	1	1	=	50% duty cycle

Port C5 Read

Direct read of DAC (Succ. Approx.) (DF1,0 = 1X bin).
Direct read of Snd Control register (DF1,0 = 01 bin).

Port C6 R/W

Frequency LSB for DAC sound channel.

7	6	5	4	3	2	1	0
F7	F6	F5	F4	F3	F2	F1	F0

Port C7 R/W

Amplitude/frequency MSN for DAC sound channel.

7	6	5	4	3	2	1	0
SAMP3	SAMP2	SAMP1	res	F11	F10	F9	F8

The amplitude will be programmable in 7 levels, with approximately 3 dB per level. The maximum level ('111') will closely approximate that in the existing sound chip. A value of '000' will result in no output. This level control also applies to the raw DAC output when outputting digitized sound.

The ramp will count up the five MSB's of the DAC. The triangle will count up the four MSB's of the DAC for the first half of the wave, then count them back down for the second half. The frequency range of the DAC as a sound channel will have the same upper limit and a lower limit of one octave lower than the new frequency range of the sound chip (down to 27.3 Hz.). Obviously, the bit programming order of the frequency is different. The actual frequency will be 111.86 KHz divided by the number programmed into the sound frequendy register(s).

Port 200 - 207 WR -- Clear Joystick DAC counter

A write to port 20X, where X = 0 to 7, will clear a free-running counter, and load a value of 16 into the 12-bit divider. The eight bit free-running counter will be clocked by the 3.58 MHz signal divided by 24, or 149.1 KHz. The output of the eight bit counter will drive the DAC to produce a stairstep wave, which simulates a ramp for use by the joystick comparators. When the counter reaches a count of 255, it will stop until port 20X is written to again.

The elapsed time for the complete ramp will be approximately 1.7 milliseconds, closely approximating the elapsed time of the current Tandy 1000 Joystick circuitry.

Port 200 - 207 RD -- Joystick Status

The data read at port 20X, where X = 0 to 7, will be the outputs of the joystick position comparators and the states of the joystick pushbuttons, in the same manner as the current Tandy 1000 Joystick circuitry.

Planar Control

Port 65 contains three bits which are used to enable the printer interface (bit 1), the printer output (bit 7), and the serial port (bit 4). These bits are all enabled (set high) on reset, and must be cleared by software to disable the appropriate function. The printer output enable function is logically "or-ed" with the current Tandy 1000 printer output enable bit, so that either one will enable the printer output buffer.

Additional control is available at port FFEB. Bit D0 selects whether the serial clock is divided by 13 or 1. Bit D1 must be high to enable the joystick function, and bit D2 must be high to enable the sound chip functions. Bits D1 and D2 default to high on power up.

I/O Map Summary

The following ports are utilized in the PSSJ part:

PORT	R/W	BITS	FUNCTION
0061	W	4	Sound Chip Enable
0065	R/W	1,4,7	Planar Control
00C0-00C3	W	all	Sound Chip Data
00C4-00C7	R/W	all	DAC Functions
0200-0207	R/W	all	Joystick Function
0378-037A	R/W	all	Printer Interface
03F8-03FF	R/W	all	Serial Interface
FFEB	R/W	0,1,2	UART clock select,JSE,DSE

Floppy Disk Support Chip Specification

Floppy Disk Support Chip Specification
Contents

Flopy Disk Support Logig
Tandy Part #8041404
January 29, 1987

1.0 GENERAL DESCRIPTION

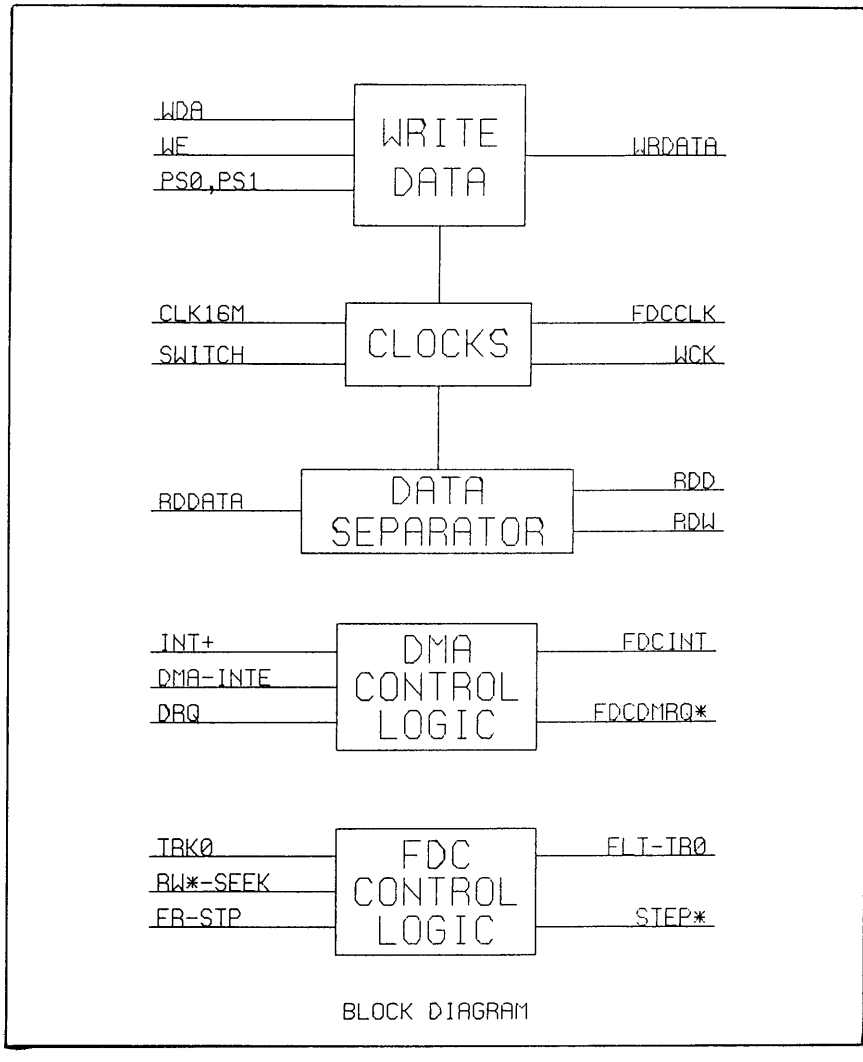
1.1 The Tandy Part #8041404 - Floppy Disk Support Logic:
-Generates the clock to the 765 Floppy Disk Controller.
-Generates the write clock to the Floppy Disk.
-Generates step pulses, track 0 indicator, DMA request, and FDC interrupt signals.

1--	CLK16M	+5	--24
2--	WCK	SWITCH	--23
3--	FDCCLK	INT+	--22
4--	RDDATA*	DMA/INTE	--21
5--	RDD	DRQ	--20
6--	RDW	FDCINT	--19
7--	FRES/S	FDCDMRQ*	--18
8--	RW*/SEEK	PS0	--17
9--	TRK0*	PS1	--16
10--	F/TRK0	WRD	--15
11--	STEP*	WRE	--14
12--	GND	WRDATA*	--13

FIGURE 1. Pin Assignment

1.2 DESCRIPTION OF PINS:

PIN #	PIN NAME	TYPE	DESCRIPTION
1	CLK16M	INPUT	Frequency = 16.0000 Tolerance = 100pmm
2	WCK	OUTPUT	If SWITCH = 0, period = 2 us, 250 ns pulse If SWITCH = 1, period = 1 us, 250 ns pulse
3	FDCCLK	OUTPUT	If SWITCH = 0, then CLK16M/4 If SWITCH = 1, then CLK16M/2
4	RDDATA	INPUT	Serial data from FDD
5	RDD	OUTPUT	Serial data from FDC
6	RDW	OUTPUT	Read Data Window
7	FRES/S	INPUT	Step pulses to move head to another cylinder
8	RW*/SEEK	INPUT	Specifies seek mode when high
9	TRK0*	INPUT	From FDD, indicating head is on track 0
10	F/TRK0	OUTPUT	To FDC, indicating head is on track 0
11	STEP*	OUTPUT	Moves head of FDD
12	GND		Ground
13	WRDATA*	OUTPUT	Serial Data to FDD
14	WRE	INPUT	Write Enable
15	WRD	INPUT	Serial Data from FDC
16	PS1	INPUT	Write precompensation status
17	PS0	INPUT	Write precompensation status
18	FDCDMRQ*	OUTPUT	DRQ delayed by 1.0 usec.
19	FDCINT	OUTPUT	Interrupt request
20	DRQ	INPUT	FDC DMA Request
21	DMA/INTE	INPUT	DMA request and FDC interrupt enable
22	INT+	INPUT	Interrupt request generated by FDC
23	SWITCH	INPUT	0 = low density drive 1 = high density drive
24	+5V		+5 Volts



BLOCK DIAGRAM

2.0 ENVIROMENTAL SPECIFICATIONS

2.1 Storage temperature: -65°C min., +150°C max.
2.2 Operating temperature: 0°C min., +25°C typ, +70°C max.

3.0 DC ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Rating:
Voltage on any pin
w.r.t. Ground: -0.5 min., 7.0 max. volts

3.2 Operating Electrical Specifications:

	Min.	Typ.	Max.	Units
3.2.1 Operating Ambient:				
Air Temperatue Range	0	25	70	°C
3.2.2 Power Supplies:				
VCC	4.5	5.0	5.5	volts
VSS	0	0	0	volts
ICC				milli-amps
Total Power				milli-watts
3.2.3 Leakage Current, All Inputs:				
Vin = 0.0 v			-10	micro-amps
Vin = 5.0 v			+10	micro-amps
3.2.4 Input voltages:				
3.2.4.1 Except RDDATA*, TRK*				
Logic "0"			.8	volts
Logic "1"	2.0			volts
3.2.4.2 RDDATA*, TRK*				
Positive going threshold		1.8		volts
Negative going threshold		1.2		volts
Hysteresis voltage	220			milli-volts
3.2.5 Output Voltages:				
3.2.5.1 Except WRDATA*, STEP*				
Logic "0" @ 4.0 mA load			.4	volts
Logic "1" @ 4.0 mA load	2.4			volts
3.2.5.2 WRDATA*, STEP*				
Logic "0" @ 48 mA			.5	volts
3.2.6 Input Capacitance (0.0 < Vin < 5.0)				
All inputs			10	pf
3.2.7 Output Capacitance				
All loads			50	pf

4.0 AC CHARACTERISTICS

4.1 FDCCLK Timing

Parameter	Min.	Typ.	Max.	Units
t_H	90	120	130	nSec
t_R, t_F		5	10	nSec
t_L	100	120	160	nSec
t_{CY}	245	250	255	nSec

4.2 WCK Timing

t_H	100	250	250	nSec
t_R, t_F		5	10	nSec
t_L		$t_{CY}-(t_H+t_R+t_F)$		
t_{CY}		2.0		µSec

4.3 WRDATA* Timing

WCK_H-WE_H	20			nSec
WCK_L-WE_L	20			nSec
PSD	20		100	nSec
WDD	20		100	nSec
WDA_W		WCK_H-50		nSec
WRD_W	115	125	135	nSec
WDD_H-WRD_L early	150		250	nSec
WDD_H-WRD_L nominal	275		375	nSec
WDD_H-WRD_L late	400		500	nSec

4.4 DMA/INTERRUPT Timing

I_H-FI_H			30	nSec
I_L-FI_L			30	nSec
DI_L-FI_L			30	nSec
WCK_H-DRQ_H	0			nSec
WCK_L-DRQ_H		-20		nSec
DRQ_H-$FDRQ_H$	750		1050	nSec
DRQ_L-$FDRQ_L$			30	nSec
DI_L-$FDRQ_L$			30	nSec
FCK_H-$FDRQ_H$			30	nSec

4.5 CONTROL Timing

Parameter	Min.	Typ.	Max.	Units
T_L-FT_H			30	nSec
T_H-FT_L			30	nSec
RS_L-FT_L			30	nSec
F_H-S_L			30	nSec
F_L-S_H			30	nSec
RS_L-S_H			30	nSec

4.6 DATA SEPARATOR Timing

RDA_W	200	350	550	nSec
RDA_L-RDD_H	188		313	nSec
RDD_W	240	250	260	nSec
RDD_H-RDW_C	850	875	900	nSec
$RDW(ND)_W$		2.0		µSec
"A"				
RDA_S	3062			nSec
RDW_C-RDD_H	15			nSec
"B"				
RDA_S	4812			nSec
RDW_C-RDD_H			1938	nSec
"C"				
RDA_S	5062			nSec
RDW_C-RDD_H	15			nSec

FDSL AC TIMING

FIG. 1 FDCCLK

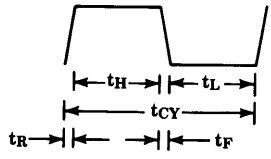
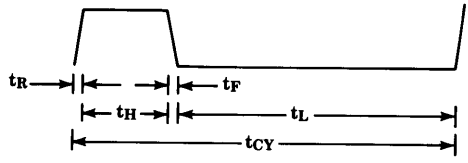


FIG. 2 WCK



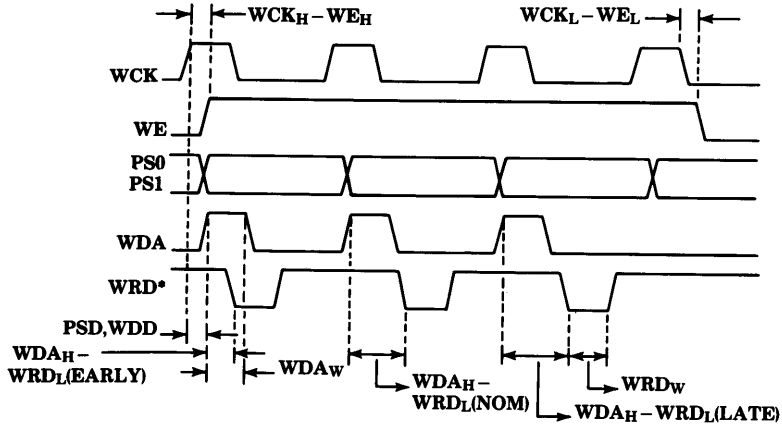


FIG. 3 WRITE DATA TIMING.

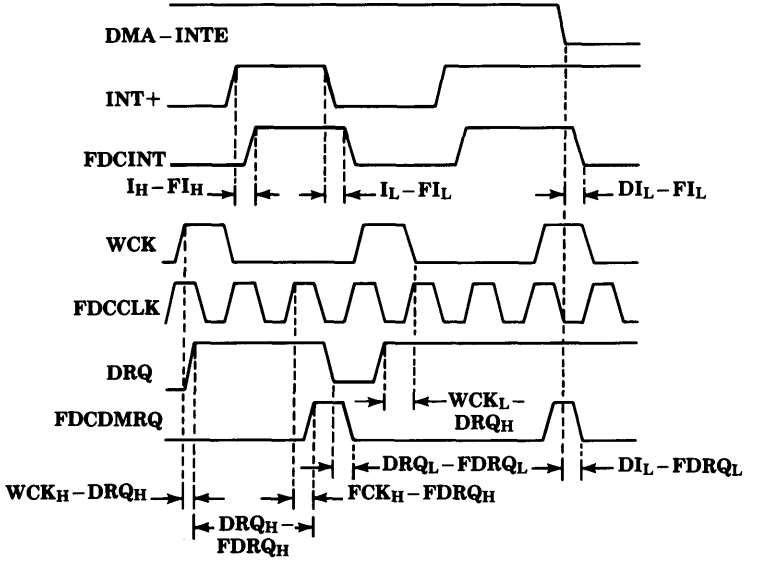


FIG. 4 DMA/INTERRUPT TIMING.

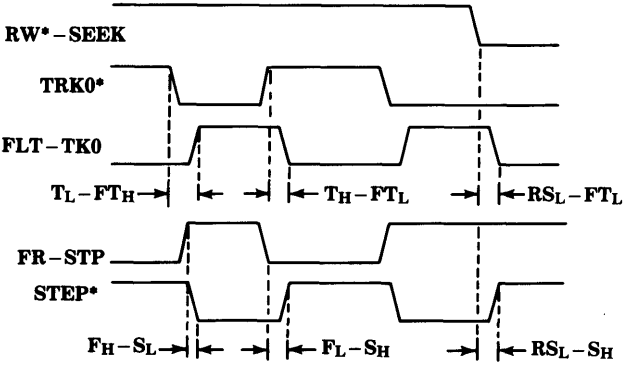


FIG. 5 CONTROL LOGIC TIMING.

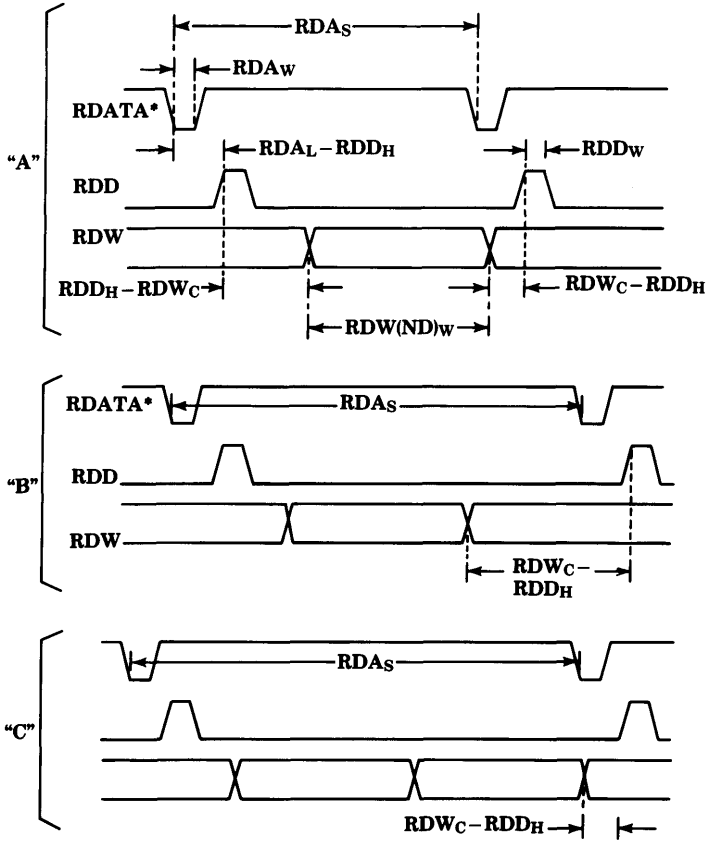


FIG. 6 DATA SEPARATOR TIMING.

μPD765A/7265
SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLERS

Description

The μPD765A is an LSI floppy disk controller (FDC) chip which contains the circuitry and control functions for interfacing a processor to 4 floppy disk drives. It is capable of either IBM 3740 single density format (FM), or IBM System 34 double density format (MFM) including double-sided recording. The μPD765A provides control signals which simplify the design of an external phase-locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy disk interface.

The μPD7265 is an addition to the FDC family that has been designed specifically for the Sony Micro Floppy-disk® drive. The μPD7265 is pin-compatible and electrically equivalent to the 765A but utilizes the Sony recording format. The μPD7265 can read a diskette that has been formatted by the μPD765A.

Each of these devices is also available in a -2 version. The -2 versions represent a reduction from 4-micron to 3-micron design rule. Functionality is the same. Minor differences between the two versions are detailed in the AC Characteristics table. The -2 versions are only available in the plastic package at this time.

Hand-shaking signals are provided in the μPD765A/μPD7265 which make DMA operation easy to incorporate with the aid of an external DMA controller chip, such as the μPD8257. The FDC will operate in either the DMA or non-DMA mode. In the non-DMA mode the FDC generates interrupts to the processor every time a data byte is to be transferred. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the FDC and DMA controllers.

There are 15 commands which the μPD765A/μPD7265 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

Read Data	Read Deleted Data
Read ID	Write Data
Specify	Format Track
Read Track	Write Deleted Data
Scan Equal	Seek
Scan High or Equal	Recalibrate
Scan Low or Equal	Sense Interrupt Status
	Sense Drive Status.

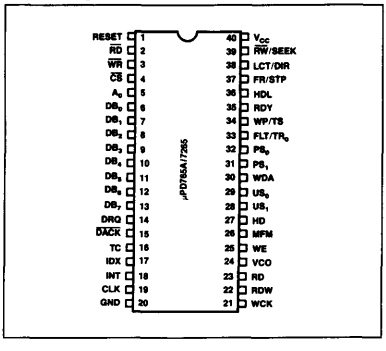
Features

Address mark detection circuitry is internal to the FDC which simplifies the phase-locked loop and read electronics. The track stepping rate, head load time, and head unload time are user-programmable. The μPD765A/μPD7265 offers additional features such as multi-track and multi-side read and write commands and single and double density capabilities.

- ☐ Sony (EMCA)-compatible recording format (μPD7265)
- ☐ IBM-compatible format (single and double density) (μPD765A)
- ☐ Multi-sector and multi-track transfer capability
- ☐ Drive Up to 4 floppy or micro floppydisk drives
- ☐ Data scan capability — will scan a single sector or an entire cylinder comparing byte-for-byte host memory and disk data
- ☐ Data transfers in DMA or non-DMA mode
- ☐ Parallel seek operations on up to four drives
- ☐ Compatible with μPD8080/85, μPD8086/88 and μPD780 (Z80®) microprocessors
- ☐ Single-phase clock (8 MHz)
- ☐ +5 V only

® Z80 is a registered trademark of the Zilog Corporation.

Pin Configuration



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Ordering Information

Part Number	Package Type	Max Freq. of Operation
μPD765AC, μPD765AC-2	40-pin plastic DIP	8 MHz
μPD7265C, μPD7265C-2	40-pin plastic DIP	8 MHz

Pin Identification

No.	Symbol	Function
1	RESET	Reset input
2	$\overline{RD}$	Read control input
3	$\overline{WR}$	Write control input
4	$\overline{CS}$	Chip select input
5	A_0	Data or status select input
6–13	DB_0–DB_7	Bidirectional data bus
14	DRQ	DMA request output
15	$\overline{DACK}$	DMA acknowledge input
16	TC	Terminal count input
17	IDX	Index input
18	INT	Interrupt request output
19	CLK	Clock input
20	GND	Ground
21	WCK	Write clock input
22	RDW	Read data window input
23	RDD	Read data input
24	VCO	VCO sync output
25	WE	Write enable output
26	MFM	MFM output
27	HD	Head select output
28, 29	US_0, US_1	FDD unit select output
30	WDA	Write data output
31, 32	PS_0, PS_1	Preshift output
33	FLT / TR_0	Fault / track zero input
34	WP / TS	Write protect / two side input
35	RDY	Ready input
36	HDL	Head load output
37	FR / STP	Fault reset / step output
38	LCT / DIR	Low current direction output
39	RW / SEEK	Read / write / seek output
40	V_{CC}	DC power

Pin Functions

RESET (Reset)

The RESET input places the FDC in the idle state. It resets the output lines to the FDD to 0 (low). It does not affect SRT, HUT, or HLT in the Specify command. If the RDY input is held high during reset, the FDC will generate an interrupt within 1.024 ms. To clear this interrupt, use the Sense Interrupt Status command.

$\overline{RD}$ (Read Strobe)

The $\overline{RD}$ input allows the transfer of data from the FDC to the data bus when low. Disabled when $\overline{CS}$ is high.

$\overline{WR}$ (Write Strobe)

The $\overline{WR}$ input allows the transfer of data to the FDC from the data bus when low. Disabled when $\overline{CS}$ is high.

A_0 (Data / Status Select)

The A_0 input selects the data register ($A_0 = 1$) or status register ($A_0 = 0$) contents to be sent to the data bus.

$\overline{CS}$ (Chip Select)

The FDC is selected when $\overline{CS}$ is low, enabling $\overline{RD}$, $\overline{WR}$, and A_0.

DB_0–DB_7 (Data Bus)

DB_0–DB_7 are a bidirectional 8-bit data bus. Disabled when $\overline{CS}$ is high.

DRQ (DMA Request)

The FDC asserts the DRQ output high to request a DMA transfer.

$\overline{DACK}$ (DMA Acknowledge)

When the $\overline{DACK}$ input is low, a DMA cycle is active and the controller is performing a DMA transfer.

TC (Terminal Count)

When the TC input is high, it indicates the termination of a DMA transfer. It terminates data transfer during Read/Write/Scan commands in DMA or interrupt mode.

IDX (Index)

The IDX input goes high at the beginning of a disk track.

INT (Interrupt)

The INT output is FDC's interrupt request.

CLK (Clock)

CLK is the input for the FDC's single-phase, 8 MHz squarewave clock.

WCK (Write Clock)

The WCK input sets the data write rate to the FDD. It is 500 kHz for FM, 1 MHz for MFM drives, with a 250 ns pulse for both FM and MFM.

RDW (Read Data Window)

The RDW input is generated by the phase-locked loop (PLL). It is used to sample data from the FDD.

RDD (Read Data)

The RDD input is the read data from the FDD, containing clock and data bits.

WDA (Write Data)

WDA is the serial clock and data output to the FDD.

WE (Write Enable)

The WE output enables write data into the FDD.

VCO (VCO Sync)

The VCO output inhibits the VCO in the PLL when low, enables it when high.

MFM (MFM Mode)

The MFM output shows the FDD's mode. It is high for MFM, low for FM.

HD (Head Select)

Head 1 is selected when the HD output is 1 (high), head 0 is selected when HD is 0 (low).

US_0, US_1 (Unit Select 0, 1)

The US_0 and US_1 outputs select the floppy disk drive unit.

PS_0, PS_1 (Preshift 0, 1)

The PS_0 and PS_1 outputs are the write precompensation status for MFM mode. They determine early, late, and normal times.

RDY (Ready)

The RDY input indicates that the FDD is ready to receive data.

HDL (Head Load)

The HDL output is the command which causes the read/write head in the FDD to contact the diskette.

FLT/TR0 (Fault/Track 0)

In the read/write mode, the FLT input detects FDD fault conditions. In the seek mode, TR0 detects track 0.

WP/TS (Write Protect/Two Side)

In the read/write mode, the WP input senses write protected status. In the seek mode, TS senses two-sided media.

FR/STP (Fault Reset/Step)

In the read/write mode, the FR output resets the fault flip-flop in the FDD. In the seek mode, STP outputs step pulses to move the head to another cylinder. A fault reset pulse (FR) is issued at the beginning or each Read or Write command prior to the HDL signal.

LCT/DIR (Low Current/Direction)

In the read/write mode, the LCT output lowers the write current on the inner tracks. In the seek mode, the DIR output determines the direction the head will move in when it receives a step pulse.

$\overline{RW}$/SEEK (Read/Write/Seek)

The $\overline{RW}$/SEEK output specifies the read/write mode when low, and the seek mode when high.

GND (Ground)

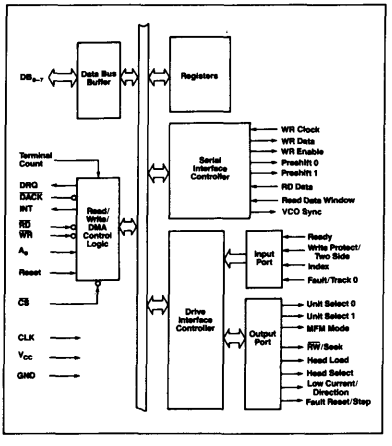
Ground.

V_{CC} (+5 V)

+5 V power supply.

6

Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{CC}	−0.5 to +7 V
Input voltage, V_I	−0.5 to +7 V
Output voltage, V_O	−0.5 to +7 V
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−40°C to +125°C
Power dissipation, P_D	1W

Comment: Exposing the device to stresses above those listed in the Absolute Maximum Ratings could cause permanent damage. The device should not be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{CC} = +5\,V \pm 5\%$ (μPD765A/7265A) and $V_{CC} = +5V \pm 10\%$ (μPD765A-2/7265A-2)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.5		+0.8	V	
Input voltage high	V_{IH}	2.0		V_{CC}+0.5	V	
Output voltage low	V_{OL}			0.45	V	$I_{OL} = 2.0\,mA$
Output voltage high	V_{OH}	2.4		V_{CC}	V	$I_{OH} = -200\,\mu A$
Input voltage low (CLK + $\overline{WR}$ clock)	$V_{IL(\Phi)}$	−0.5		0.65	V	
Input voltage high (CLK + $\overline{WR}$ clock)	$V_{IH(\Phi)}$	2.4		V_{CC}+0.5	V	
Supply current (V_{CC})	I_{CC}			150	mA	
Input load current high	I_{LIH}			10	μA	$V_{IN} = V_{CC}$
Input load current low	I_{LIL}			−10	μA	$V_{IN} = 0\,V$
Output leakage current high	I_{LOH}			10	μA	$V_{OUT} = V_{CC}$
Output leakage current low	I_{LOL}			−10	μA	$V_{OUT} = +0.45\,V$

Capacitance

$T_A = 25°C$, $f_C = 1\,MHz$, $V_{CC} = 0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input clock capacitance	$C_{IN(\Phi)}$			20	pF	(Note 1)
Input capacitance	C_{IN}			10	pF	(Note 1)
Output capacitance	C_{OUT}			20	pF	(Note 1)

Note:
(1) All pins except pin under test tied to AC ground

AC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{CC} = +5\ V \pm 5\%$ (μPD765A/7265A) and $V_{CC} = +5V \pm 10\%$ (μPD765A-2/7265A-2)

Parameter	Symbol	Limits						Unit	Test Conditions
		765A, 7265			765A-2, 7265-2				
		Min	Typ (1)	Max	Min	Typ (1)	Max		
Clock period	Φ_{CY}	120	125	500	120	125	500	ns	(Note 4)
			125			125		ns	8″ FDD
			250			250		ns	5¼″ FDD
			125			125		ns	3½″ Sony (3)
Clock active (high, low)	Φ_0	40			40			ns	
Clock rise time	Φ_r			20			20	ns	
Clock fall time	Φ_f			20			20	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{RD}\downarrow$	t_{AR}	0			0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{RD}\uparrow$	t_{RA}	0			0			ns	
$\overline{RD}$ width	t_{RR}	250			200			ns	
Data access time from $\overline{RD}\downarrow$	t_{RD}			200			140	ns	$C_L = 100$ pF
DB to float delay time from $\overline{RD}\uparrow$	t_{DF}	20		100	10		85	ns	$C_L = 100$ pF
A_0, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{WR}\downarrow$	t_{AW}	0			0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ hold time to $\overline{WR}\uparrow$	t_{WA}	0			0			ns	
$\overline{WR}$ width	t_{WW}	250			200			ns	
Data setup time to $\overline{WR}\uparrow$	t_{DW}	150			100			ns	
Data hold time from $\overline{WR}\uparrow$	t_{WD}	5			0			ns	
INT delay time from $\overline{RD}\uparrow$	t_{RI}			500			400	ns	
INT delay time from $\overline{WR}\uparrow$	t_{WI}			500			400	ns	
DRQ cycle time	t_{MCY}	13			13			μs	$\Phi_{CY} = 125$ ns (4)
$\overline{DACK}\downarrow \rightarrow$ DRQ↓ delay	t_{AM}			200			140	ns	
DRQ↑ → $\overline{DACK}\downarrow$ delay	t_{MA}	200			200			ns	$\Phi_{CY} = 125$ ns (4)
$\overline{DACK}$ width	t_{AA}	2			2			Φ_{CY}	
TC width	t_{TC}	1			1			Φ_{CY}	
Reset width	t_{RST}	14			14			Φ_{CY}	
WCK cycle time	t_{CY}		4			16		Φ_{CY}	MFM = 0, 5¼″
			2			8		Φ_{CY}	MFM = 1, 5¼″
			2			8		Φ_{CY}	MFM = 0, 8″
			1			4		Φ_{CY}	MFM = 1, 8″
			2			8		Φ_{CY}	MFM = 0, 3½″ (3)
			1			4		Φ_{CY}	MFM = 1, 3½″(3)
WCK active time (high)	t_0		2			2		Φ_{CY}	
CLK↑ → WCK↑ delay	t_{CWH}	0		40	0		40	ns	
CLK↑ → WCK↓ delay	t_{CWL}	0		40	0		40	ns	
WCK rise time	t_r			20			20	ns	
WCK fall time	t_f			20			20	ns	
Preshift delay time from WCK↑	t_{CP}	20		100	20		100	ns	
WCK↑ → WE↑ delay	t_{CWE}	20		100	20		100	ns	
WDA delay time from WCK↑	t_{CD}	20		100	20		100	ns	
RDD active time (high)	t_{RDD}	40			40			ns	

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AC Characteristics (cont)

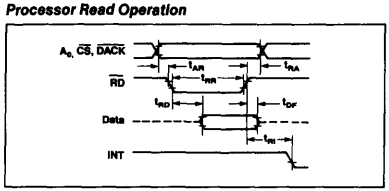
T_A = −10°C to +70°C, V_{CC} = +5 V ±5% (μPD765A/7265A) and V_{CC} = +5V ±10% (μPD765A-2/7265A-2)

Parameter	Symbol	Limits 765A, 7265 Min	Typ (1)	Max	765A-2, 7265-2 Min	Typ (1)	Max	Unit	Test Conditions
Window cycle time	t_{WCY}		4			4		μs	MFM = 0, 5¼"
			2			2		μs	MFM = 1, 5¼"
			2			2		μs	MFM = 0, 8"
			1			1		μs	MFM = 1, 8"
			2			2		μs	MFM = 0, 3½" (3)
			1			1		μs	MFM = 1, 3½"(3)
Window hold time to RDD	t_{RDW}	15			15			ns	
Window hold time from RDD	t_{WRD}	15			15			ns	
$US_{0,1}$ hold time to $\overline{RW}$ / seek↑	t_{US}	12			12			μs	8 MHz clock period(4)
$\overline{RW}$ / seek hold time to low current / direction↑	t_{SD}	7			7			μs	8 MHz clock period(4)
Low current / direction hold time to fault reset / step↑	t_{DST}	1.0			1.0			μs	8 MHz clock period(4)
$US_{0,1}$ hold time from fault reset / step↑	t_{STU}	5.0			5.0			μs	8 MHz clock period(4)
Step active time (high)	t_{STP}	6	7	8	6	7	8	μs	(Note 4)
Step cycle time	t_{SC}	33	(Note 2)	(Note 2)	33	(Note 2)	(Note 2)	μs	(Note 4)
Fault reset active time (high)	t_{FR}	8.0		10	8.0		10	μs	(Note 4)
Write data width	t_{WDD}	t_D−50			t_D−50			ns	
$US_{0,1}$ hold time after seek	t_{SU}	15			15			μs	8 MHz clock period(4)
Seek hold time from DIR	t_{DS}	30			30			μs	8 MHz clock period(4)
DIR hold time after step	t_{STD}	24			24			μs	8 MHz clock period(4)
Index pulse width	t_{IDX}	4			4			Φ_{CY}	
$\overline{RD}$↓ delay from DRQ	t_{MR}	800			800			ns	8 MHz clock period(4)
$\overline{WR}$↓ delay from DRQ	t_{MW}	250			250			ns	8 MHz clock period(4)
WE or $\overline{RD}$ response time from DRQ↑	t_{MRW}			12			12	μs	8 MHz clock period(4)

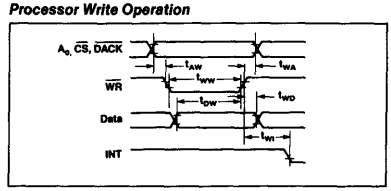
Note:
(1) Typical values for T_A = 25°C and nominal supply voltage.
(2) Under software control. The range is from 1 ms to 16 ms at 8 MHz clock period, and 2 ms to 32 ms at 4 MHz clock period.
(3) Sony Micro Floppydisk 3½" drive.
(4) Double these values for a 4 MHz clock period.

Timing Waveforms

Processor Read Operation

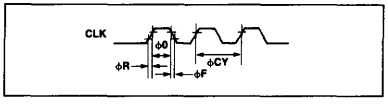


Processor Write Operation

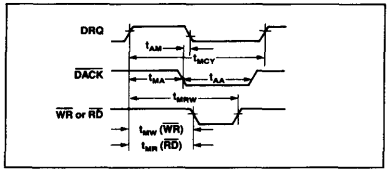


Timing Waveforms (cont)

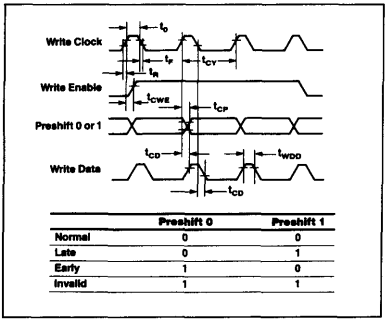
Clock



DMA Operation

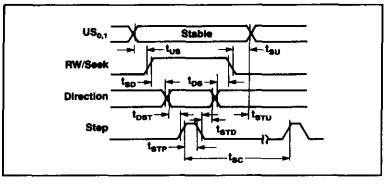


FDD Write Operation

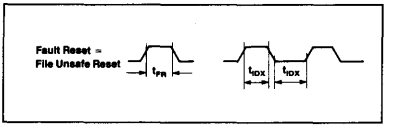


	Preshift 0	Preshift 1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1

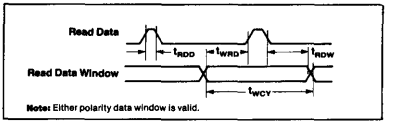
Seek Operation



FLT Reset

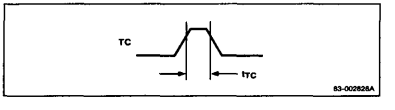


FDD Read Operation

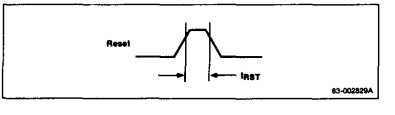


Note: Either polarity data window is valid.

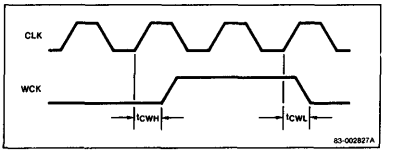
Terminal Count



Reset



Write Clock



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Internal Registers

The μPD765A/μPD7265 contains two registers which may be accessed by the main system processor: a status register and a data register. The 8-bit main status register contains the status information of the FDC, and may be accessed at any time. The 8-bit data register (which actually consists of four registers, ST0-ST3, in a stack with only one register presented to the data bus at a time), stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the data register in order to program or obtain the results after a particular command (table 3). Only the status register may be read and used to facilitate the transfer of data between the processor and μPD765A/μPD7265.

The relationship between the status/data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown in table 1.

Table 1. Status/Data Register Addressing

A_0	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	Read main status register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from data register
1	1	0	Write into data register

The bits in the main status register are defined in table 2.

Table 2. Main Status Register

No.	Pin Name	Function
DB_0	D_0B (FDD 0 Busy)	FDD number 0 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_1	D_1B (FDD 1 Busy)	FDD number 1 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_2	D_2B (FDD 2 Busy)	FDD number 2 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_3	D_3B (FDD 3 Busy)	FDD number 3 is in the seek mode. If any of the D_nB bits is set FDC will not accept read or write command.
DB_4	CB (FDC Busy)	A Read or Write command is in process. FDC will not accept any other command.
DB_5	EXM (Execution Mode)	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended and result phase has started. It operates only during non-DMA mode of operation.

Table 2. Main Status Register (cont)

No.	Pin Name	Function
DB_6	DIO (Data Input / Output)	Indicates direction of data transfer between FDC and data register. If DIO = 1, then transfer is from data register to the processor. If DIO = 0, then transfer is from the processor to data register.
DB_7	RQM (Request for Master)	Indicates data register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the status register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last $\overline{RD}$ or $\overline{WR}$ during a command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time the main status register is read the CPU should wait 12 μs. The maximum time from the trailing edge of the last $\overline{RD}$ in the result phase to when DB_4 (FDC busy) goes low is 12 μs. See figure 1.

Figure 1. DIO and RQM

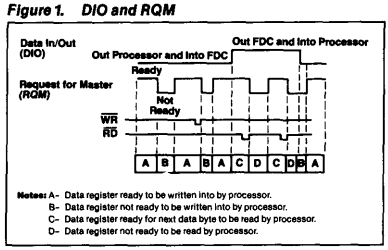

Table 3. Status Register Identification

Pin No.	Name	Function
Status Register 0		
D_7, D_6	IC (Interrupt Code)	$D_7=0$ and $D_6=0$ Normal termination of command, (NT). Command was completed and properly executed.
		$D_7=0$ and $D_6=1$ Abnormal termination of command, (AT). Execution of command was started but was not successfully completed.
		$D_7=1$ and $D_6=0$ Invalid command issue, (IC). Command which was issued was never started.
		$D_7=1$ and $D_6=1$ Abnormal termination because during command execution the ready signal from FDD changed state.
D_5	SE (Seek End)	When the FDC completes the Seek command, this flag is set to 1 (high).
D_4	EC (Equipment Check)	If a fault signal is received from the FDD, or if the track 0 signal fails to occur after 77 step pulses (Recalibrate Command) then this flag is set.
D_3	NR (Not Ready)	When the FDD is in the not-ready state and a Read or Write command is issued, this flag is set. If a Read or Write command is issued to side 1 of a single-sided drive, then this flag is set.
D_2	HD (Head Address)	This flag is used to indicate the state of the head at interrupt.
D_1	US_1 (Unit Select 1)	This flag is used to indicate a drive unit number at interrupt.
D_0	US_0 (Unit Select 0)	This flag is used to indicate a drive unit number at interrupt.
Status Register 1		
D_7	EN (End of Cylinder)	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D_6		Not used. This bit is always 0 (low).
D_5	DE (Data Error)	When the FDC detects a CRC(1) error in either the ID field or the data field, this flag is set.
D_4	OR (Overrun)	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D_3		Not used. This bit is always 0 (low).

Table 3. Status Register Identification (cont)

Pin No.	Name	Function
Status Register 1 (cont)		
D_2	ND (No Data)	During execution of Read Data, Write Deleted Data or Scan command, if the FDC cannot find the sector specified in the IDR(2) Register, this flag is set.
		During execution of the Read ID command, if the FDC cannot read the ID field without an error, then this flag is set.
		During execution of the Read A Cylinder command, if the starting sector cannot be found, then this flag is set.
D_1	NW (Not Writable)	During execution of Write Data, Write Deleted Data or Format A Cylinder command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	MA (Missing Address Mark)	If the FDC cannot detect the data address mark or deleted data address mark, this flag is set. Also at the same time, the MD (missing address mark in data field) of status register 2 is set.
Status Register 2		
D_7		Not used. This bit is always 0 (low).
D_6	CM (Control Mark)	During execution of the Read Data or Scan command, if the FDC encounters a sector which contains a deleted data address mark, this flag is set.
D_5	DD (Data Error in Data Field)	If the FDC detects a CRC error in the data field then this flag is set.
D_4	WC (Wrong Cylinder)	This bit is related to the ND bit, and when the contents of C(3) on the medium is different from that stored in the IDR, this flag is set.
D_3	SH (Scan Equal Hit)	During execution of the Scan command, if the condition of "equal" is satisfied, this flag is set.
D_2	SN (Scan Not Satisfied)	During execution of the Scan command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D_1	BC (Bad Cylinder)	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FFH, then this flag is set.
D_0	MD (Missing Address Mark in Data Field)	When data is read from the medium, if the FDC cannot find a data address mark or deleted data address mark, then this flag is set.

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Table 3. Status Register Identification (cont)

Pin No.	Name	Function
Status Register 3		
D_7	FT (Fault)	This bit is used to indicate the status of the fault signal from the FDD.
D_6	WP (Write Protected)	This bit is used to indicate the status of the write protected signal from the FDD.
D_5	RY (Ready)	This bit is used to indicate the status of the ready signal from the FDD.
D_4	T0 (Track 0)	This bit is used to indicate the status of the track 0 signal from the FDD.
D_3	TS (Two-Side)	This bit is used to indicate the status of the two-side signal from the FDD.
D_2	HD (Head Address)	This bit is used to indicate the status of the side select signal to the FDD.
D_1	US_1 (Unit Select 1)	This bit is used to indicate the status of the unit select 1 signal to the FDD.
D_0	US_0 (Unit Select 0)	This bit is used to indicate the status of the unit select 0 signal to the FDD.

Note:
(1) CRC = Cyclic Redundancy Check
(2) IDR = Internal Data Register
(3) Cylinder (C) is described more fully in the Command Symbol Description.

Command Sequence

The μPD765A/μPD7265 is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the μPD765A/μPD7265 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase: The FDC receives all information required to perform a particular operation from the processor.

Execution Phase: The FDC performs the operation it was instructed to do.

Result Phase: After completion of the operation, status and other housekeeping information are made available to the processor.

Table 4 shows the required preset parameters and results for each command. Most commands require 9 command bytes and return 7 bytes during the result phase. The "W" to the left of each byte indicates a command phase byte to be written, and an "R" indicates a result byte. The definitions of other abbriviations used in table are given in the Command Symbol Description table.

Command Symbol Description

Name	Function
A_0 (Address Line 0)	A_0 controls selection of main status register (A_0 = 0) or data register (A_0 = 1).
C (Cylinder Number)	C stands for the current / selected cylinder (track) numbers 0 through 76 of the medium.
D (Data)	D stands for the data pattern which is going to be written into a sector.
D_7–D_0 (Data Bus)	8-bit data bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL (Data Length)	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector.
EOT (End of Track)	EOT stands for the final sector number on a cylinder. During read or write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL (Gap Length)	GPL stands for the length of gap 3. During Read / Write commands this value determines the number of bytes that VCO sync will stay low after two CRC bytes. During Format command it determines the size of gap 3.
H (Head Address)	H stands for head number 0 or 1, as specified in ID field.
HD (Head)	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT (Head Load Time)	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT (Head Unload Time)	HUT stands for the head unload time after a Read or Write operation has occurred (16 to 240 ms in 16 ms increments).
MF (FM or MFM Mode)	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT (Multitrack)	IF MT is high, a multitrack operation is performed. If MT = 1 after finishing read / write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N (Number)	N stands for the number of data bytes written in a sector.
NCN (New Cylinder Number)	NCN stands for a new cylinder number which is going to be reached as a result of the seek operation; desired position of head.
ND (Non-DMA Mode)	ND stands for operation in the non-DMA mode.
PCN (Present Cylinder Number)	PCN stands for the cylinder number at the completion of Sense Interrupt Status command, position of head at present time.
R (Record)	R stands for the sector number which will be read or written.
R / W (Read / Write)	R / W stands for either Read (R) or Write (W) signal.
SC (Sector)	SC indicates the number of sectors per cylinder.
SK (Skip)	SK stands for skip deleted data address mark.

Command Symbol Description (cont)

Name	Function
SRT (Step Rate Time)	SRT stands for the stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (FH = 1 ms, EH = 2 ms, etc.).
ST0–ST3 (Status 0–3)	ST0–ST3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0 = 0$). ST0–ST3 may be read only after a command has been executed and contains information relevant to that particular command.

Command Symbol Description (cont)

Name	Function
STP	During a scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US_0, US_1 (Unit Select)	US stands for a selected drive number 0 or 1.

Table 4. Instruction Set (Notes 1, 2)

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read Data										
Command	W	MT	MF	SK	0	0	1	1	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	(Note 3)
	W	←				C			→	Sector ID information prior to command execution. The 4 bytes
	W	←				H			→	are compared against header on floppy disk.
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Read Deleted Data										
Command	W	MT	MF	SK	0	1	1	0	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution. The 4 bytes
	W	←				H			→	are compared against header on floppy disk.
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the FDD and main system
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	

Note:
(1) Symbols used in this table are described at the end of this section.
(2) A_0 should equal 1 for all operations.
(3) X = Don't care, usually made to equal 0.

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Table 4. Instruction Set (Notes 1, 2) (cont)

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Write Data										
Command	W	MT	MF	0	0	0	1	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution. The 4 bytes are compared against header on floppy disk.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the main system and FDD
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Write Deleted Data										
Command	W	MT	MF	0	0	1	0	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution. The 4 bytes are compared against header on floppy disk.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the FDD and main system
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Read A Track										
Command	W	0	MF	SK	0	0	0	1	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the FDD and main system. FDC reads all data fields from index hole to EOT.
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

Table 4. Instruction Set (Notes 1, 2) (cont)

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read ID										
Command	W	0	MF	0	0	1	0	1	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
Execution										The first correct ID information on the cylinder is stored in data register.
Result	R	←				ST 0			→	Status information after command execution
	R	←				ST 1			→	
	R	←				ST 2			→	
	R	←				C			→	Sector ID information read during execution phase from floppy disk.
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Format A Track										
Command	W	0	MF	0	0	1	1	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				N			→	Bytes / sector
	W	←				SC			→	Sectors / track
	W	←				GPL			→	Gap 3
	W	←				D			→	Filler byte
Execution										FDC formats an entire track.
Result	R	←				ST 0			→	Status information after command execution
	R	←				ST 1			→	
	R	←				ST 2			→	
	R	←				C			→	In this case, the ID information has no meaning
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	
Scan Equal										
Command	W	MT	MF	SK	1	0	0	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				STP			→	
Execution										Data compared between the FDD and main system
Result	R	←				ST 0			→	Status information after command execution
	R	←				ST 1			→	
	R	←				ST 2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	

Note:
(1) Symbols used in this table are described at the end of this section.
(2) A_0 should equal 1 for all operations.
(3) X = Don't care, usually made to equal 0.

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Table 4. Instruction Set (Notes 1, 2) (cont)

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Scan Low or Equal										
Command	W	MT	MF	SK	1	1	0	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			STP				→	
Execution										Data compared between the FDD and main system
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Scan High or Equal										
Command	W	MT	MF	SK	1	1	1	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			STP				→	
Execution										Data compared between the FDD and main system
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Recalibrate										
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	X	X	X	X	X	0	US_1	US_0	
Execution										Head retracted to track 0
Sense Interrupt Status										
Command	W	0	0	0	0	1	0	0	0	Command codes
Result	R	←			ST0				→	Status information about the FDC at the end of seek operation
	R	←			PCN				→	
Specify										
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	←	SRT	→	←	HUT	→			
	W	←		HLT		→	ND			
Sense Drive Status										
Command	W	0	0	0	0	0	1	0	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
Result	R	←			ST3				→	Status information about FDD

Table 4. Instruction Set (Notes 1, 2) (cont)

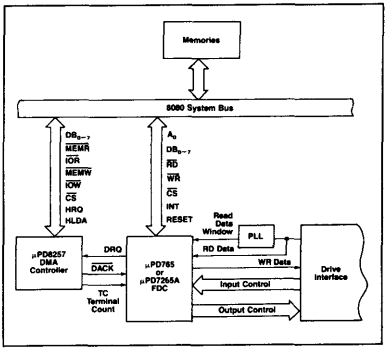
Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Seek										
Command	W	0	0	0	0	1	1	1	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	← NCN →								
Execution										Head is positioned over proper cylinder on diskette
Invalid										
Command	W	← Invalid Codes →								Invalid Command codes (No op — FDC goes into standby state)
Result	R	← ST0 →								ST0 = 80H

Note:
(1) Symbols used in this table are described at the end of this section.
(2) A_0 should equal 1 for all operations.
(3) X = Don't care, usually made to equal 0.

System Configuration

Figure 2 shows an example of a system using a μPD765A/μPD7265.

Figure 2. System Configuration



Processor Interface

During command or result phases the main status register (described earlier) must be read by the processor before each byte of information is written into or read from the data register. After each byte of data read or written to the data register, CPU should wait for 12 μs before reading main status register, bits D_6 and D_7 in the main status register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the μPD765A/μPD7265. Many of the commands require multiple bytes and, as a result, the main status register must be read prior to each byte transfer to the μPD765A/μPD7265. On the other hand, during the result phase, D_6 and D_7 in the main status register must both be 1's ($D_6 = 1$ and $D_7 = 1$) before reading each byte from the data register. Note that this reading of the main status register before each byte transfer to the μPD765A/μPD7265 is required only in the command and result phases, and *not* during the execution phase.

During the execution phase, the main status register need not be read. If the μPD765A/μPD7265 is in the non-DMA mode, then the receipt of each data byte (if μPD765A/μPD7265 is reading data from FDD) is indicated by an interrupt signal on pin 18 (INT = 1). The generation of a read signal ($\overline{RD} = 0$) or write signal ($\overline{WR} = 0$) will clear the interrupt as well as output the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13 μs for the MFM mode and 27 μs for the FM mode), then it may poll the main status register and bit D_7 (RQM) functions as the interrupt signal. If a write command is in process then the $\overline{WR}$ signal negates the reset to the interrupt signal.

Note that in the non-DMA mode it is necessary to examine the main status register to determine the cause of the interrupt, since it could be a data interrupt or a command termination interrupt, either normal or abnormal.

If the μPD765A/μPD7265 is in the DMA mode, no interrupts are generated during the execution phase. The μPD765A/μPD7265 generates DRQs (DMA requests) when each byte of data is available. The DMA controller responds to this request with both a $\overline{DACK} = 0$ (DMA acknowledge) and an RD = 0 (read signal). When the DMA acknowledge signal goes low ($\overline{DACK} = 0$), then the DMA request is cleared (DRQ = 0). If a write command has been issued then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the execution phase has been completed (terminal count has occurred) or the EOT sector read/written, then an interrupt will occur (INT = 1). This signifies the beginning of the result phase. When the first byte of

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data is read during the result phase, the interrupt is automatically cleared (INT = 0).

The $\overline{RD}$ or $\overline{WR}$ signals should be asserted while $\overline{DACK}$ is true. The $\overline{CS}$ signal is used in conjunction with $\overline{RD}$ and $\overline{WR}$ as a gating function during programmed I/O operations. $\overline{CS}$ has no effect during DMA operations. If the non-DMA mode is chosen, the $\overline{DACK}$ signal should be pulled up to V_{CC}.

It is important to note that during the result phase all bytes shown in the command table (table 4) must be read. The read data command, for example, has seven bytes of data in the result phase. All seven bytes must be read in order to successfully complete the Read Data command. The μPD765A/μPD7265 will not accept a new comand until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase.

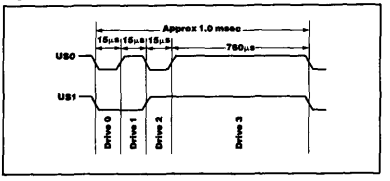
The μPD765A/μPD7265 contains five status registers. The main status register mentioned above may be read by the processor at any time. The other four status registers (ST0, ST1, ST2, and ST3) are available only during the result phase and may be read only after completing a command. The particular command that has been executed determines how many of the status registers will be read.

The bytes of data which are sent to the μPD765A/μPD7265 to form the command phase and are read out of the μPD765A/μPD7265 in the result phase must occur in the order shown in table 4. That is, the command code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the command or result phases is allowed. After the last byte of data in the command phase is sent to the μPD765A/μPD7265, the execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the result phase, the command is automatically ended and the μPD765A/μPD7265 is ready for a new command.

Polling

After reset has been sent to the μPD765A/μPD7265, the unit select lines US_0 and US_1 will automatically go into a polling mode. In between commands (and between step pulses in the Seek command) the μPD765A/μPD7265 polls all four FDDs looking for a change in the ready line from any of the drives. If the ready line changes state (usually due to a door opening or closing), then the μPD765A/μPD7265 will generate an interrupt. When status register 0 (ST0) is read (after Sense Interrupt Status is issued), not ready (NR) will be indicated. The polling of the ready line by the μPD765A/μPD7265 occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands. When used with a 4 MHz clock for interfacing to minifloppies, the polling rate is 2.048 ms. See figure 3.

Figure 3. Polling Feature



Read Data

A set of nine (9) byte words are required to place the FDC into the read data mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID address marks and ID fields. When the current sector number (R) stored in the ID register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the sector number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a multi-sector read operation. The Read Data command may be terminated by the receipt of a terminal count signal. TC should be issued at the same time that the $\overline{DACK}$ for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (cyclic redundancy count) bytes, and then at the end of the sector terminate the Read Data command. The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (number of bytes/sector). Table 5 shows the transfer capacity.

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at sector 1, side 0 and completing at sector L, side 1 (sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond DTL in the sector is not sent to the data bus. The FDC reads (internally) the complete sector performing the CRC check and, depending upon the manner of command

termination, may perform a multi-sector read operation. When N is non-zero, then DTL has no meaning and should be set to FFH.

Table 5. Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskettes
0	0	00	(128) (26) = 3,328	26 at side 0
0	1	01	(256) (26) = 6,656	or 26 at side 1
1	0	00	(128) (52) = 6,656	26 at side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at side 0
0	1	02	(512) (15) = 7,680	or 15 at side 1
1	0	01	(256) (30) = 7,680	15 at side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at side 0
0	1	03	(1024) (8) = 8,192	or 8 at side 1
1	0	02	(512) (16) = 8,192	8 at side 1
1	1	03	(1024) (16) = 16,384	

At the completion of the Read Data command, the head is not unloaded until after head unload time interval (specified in the Specify command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the index hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No data) flag in status register 1 to a 1 (high), and terminates the Read Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1, respectively.)

After reading the ID and data fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (data error) flag in status register 1 to a 1 (high), and if a CRC error occurs in the data field, the FDC also sets the DD (data error in data field) flag in status register 2 to a 1 (high), and terminates the Read Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1, respectively.)

If the FDC reads a deleted data address mark off the diskette, and the SK bit (bit D_5 in the first command word) is not set (SK = 0), then the FDC sets the CM (control mark) flag in status register 2 to a 1 (high), and terminates the Read Data command, after reading all the data in the sector. If SK = 1, the FDC skips the sector with the deleted data address mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM mode, and every 13 μs in the MFM mode, or the FDC sets the OR (Overrun) flag in status register 1 to a 1 (high), and terminates the Read Data command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the values for C, H, R, and N, when the processor terminates the command.

Functional Description of Commands

Write Data

A set of nine (9) bytes is required to set the FDC into the write data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD. See table 6.

Table 6. Command Description

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
0	0	Equal to EOT	C+1	NC	R=01	NC
0	1	Less than EOT	NC	NC	R+1	NC
0	1	Equal to EOT	C+1	NC	R=01	NC
1	0	Less than EOT	NC	NC	R+1	NC
1	0	Equal to EOT	NC	LSB	R=01	NC
1	1	Less than EOT	NC	NC	R+1	NC
1	1	Equal to EOT	C+1	LSB	R=01	NC

Note:

(1) NC (No Change): The same value as the one at the beginning of command execution.

(2) LSB (Least Significant Bit): The least significant bit of H is complemented.

After writing data into the current sector, the sector number stored in R is incremented by one, and the next data field is written into. The FDC continues this multi-sector write operation until the issuance of a terminal count signal. If a terminal count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the terminal count signal is received while a data field is being written then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (CRC error) in one of the ID fields, it sets the DE (Data Error) flag of status register 1 to a 1 (high) and terminates the Write

Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1, respectively.)

The Write command operates in much the same manner as the Read command. The following items are the same, and one should refer to the Read Data command for details:

- Transfer capacity
- EN (end of cylinder) flag
- ND (no data) flag
- Head unload time interval
- ID Information when the processor terminates command
- Definition of DTL when N = 0 and when N≠0

In the write data mode, data transfers between the processor and FDC, via the data bus, must occur every 27 μs in the FM mode and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this, the FDC sets the OR (overrun) flag in status register 1 to a 1 (high) and terminates the Write Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1, respectively.)

Write Deleted Data

This command is the same as the Write Data command except a deleted data address mark is written at the beginning of the data field instead of the normal data address mark.

Read Deleted Data

This command is the same as the Read Data command except that when the FDC detects a data address mark at the beginning of a data field (and SK = 0 (low)), it will read all the data in the sector and set the CM flag in status register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the data address mark and reads the next sector.

Read a Track

This command is similar to the Read Data command except that this is a continuous read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hole, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and sets the ND flag of status register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID address mark on the diskette after it senses the index hole for the second time, it sets the MA (missing address mark) flag in status register 1 to a 1 (high) and terminates the command. (Status register 0 has bits 7 and 6 set to 0 and 1, respectively.)

Read ID

The Read ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID address mark is found on the diskette before the index hole is encountered for the second time, then the MA (missing address mark) flag in status register 1 is set to a 1 (high), and if no data is found then the ND (No data) flag is also set in status register 1 to a 1 (high). The command is then terminated with bits 7 and 6 in status register 0 set to 0 and 1, respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format a Track

The Format a Track command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; gaps, address marks, ID fields, and data fields, all per the IBM System 34 (double density) or System 3740 (single density) format, are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (gap length), and D (data pattern) which are supplied by the processor during the command phase. The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (cylinder number), H (head number), R (sector number), and N (number of bytes/sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the μPD765A/μPD7265 for each sector on the track. If FDC is set for the DMA mode, it will issue four DMA requests per sector. If it is set for the interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R register are incremented by 1 after each sector is formatted; thus, the R register contains a value of R when it is read during the result phase. This incrementing and formatting continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

If a fault signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of status register 0 to a 1 (high) and terminates the command after setting bits 7 and 6 of status register 0 to 0 and 1, respec-

tively. Also, the loss of a ready signal at the beginning of a command execution phase causes bits 7 and 6 of status register 0 to be set to 0 and 1, respectively.

Table 7 shows the relationship between N, SC, and GPL for various sector sizes.

Table 7. Sector Size

Format	Sector Size	N	SC	GPL(1)	GPL(2, 3)
8" Standard Floppy					
FM Mode	128 Bytes / Sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode(4)	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5¼" Minifloppy					
FM Mode	128 Bytes / Sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode(4)	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3½" Sony Micro Floppydisk					
FM Mode	128 Bytes / Sector	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode(4)	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

Note:
(1) Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
(2) Suggested values of GPL in format command.
(3) All values except sector size are hexidecimal.
(4) In MFM mode FDC cannot perform a Read/Write/Format operation with 128 bytes/sector. (N = 00).

Scan Commands

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} < D_{Processor}$, or $D_{FDD} > D_{Processor}$. The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. One's complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (scan hit) flag of status register 2 to a 1 (high) and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (scan not satisfied) flag of status register 2 to a 1 (high) and terminates the Scan command. The receipt of a terminal count signal from the processor or DMA controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process and then to terminate the command. Table 8 shows the status of bits SH and SN under various conditions of Scan.

Table 8. Scan Conditions

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$

If the FDC encounters a deleted data address mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (control mark) flag of status register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the deleted address mark and reads the next sector. In the second case (SK = 1), the FDC sets the CM

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(control mark) flag of status register 2 to a 1 (high) in order to show that a deleted sector has been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02) sectors are read or the MT (multi-track) is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sector 21, the following will happen: sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the index hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA controller for comparison against the data read from the diskette. In order to avoid having the OR (overrun) flag set in status register 1, it is necessary to have the data available in less than 27 μs (FM mode) or 13 μs (MFM mode). If an overrun occurs, the FDC ends the command with bits 7 and 6 of status register 0 set to 0 and 1, respectively.

Seek

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek command. FDC has four independent present cylinder registers for each drive. They are cleared only after the Recalibrate command. The FDC compares the PCN (present cylinder number) which is the current head position with the NCN (new cylinder number), and if there is a difference, performs the following operations:

PCN < NCN: Direction signal to FDD set to a 1 (high), and step pulses are issued. (Step in)

PCN > NCN: Direction signal to FDD set to a 0 (low), and step pulses are issued. (Step out)

The rate at which step pulses are issued is controlled by SRT (stepping rate time) in the Specify command. After each step pulse is issued NCN is compared against PCN, and when NCN = PCN, the SE (seek end) flag is set in status register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits D_0B–D_3B in the main status register are set during the seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the seek operation the FDC is in the FDC busy state, but during the execution phase it is in the non-busy state. While the FDC is in the non-busy state, another Seek command may be issued, and in this manner parallel seek operations may be done on up to four drives at once. No other command can be issued for as long as the FDC is in the process of sending step pulses to any drive.

If an FDD is in a not ready state at the beginning of the command execution phase or during the seek operation, then the NR (not ready) flag is set in status register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of status register 0 are set to 0 and 1, respectively.

If the time to write three bytes of Seek command exceeds 150 μs, the timing between the first two step pulses may be shorter than set in the Specify command by as much as 1 ms.

Recalibrate

The function of this command is to retract the read/write head within the FDD to the track 0 position. The FDC clears the contents of the PCN counter and checks the status of the track 0 signal from the FDD. As long as the track 0 signal is low, the direction signal remains 0 (low) and step pulses are issued. When the track 0 signal goes high, the SE (seek end) flag in status register 0 is set to a 1 (high) and the command is terminated. If the track 0 signal is still low after 77 step pulses have been issued, the FDC sets the SE (seek end) and EC (equipment check) flags of status register 0 to both 1s (highs) and terminates the command after bits 7 and 6 of status register 0 are set to 0 and 1, respectively.

The ability to do overlapping Recalibrate commands to multiple FDDs and the loss of the ready signal, as described in the Seek command, also applies to the Recalibrate command. If the diskette has more than 77 tracks, then Recalibrate command should be issued twice, in order to position the read/write head to the track 0.

Sense Interrupt Status

An interrupt signal is generated by the FDC for one of the following reasons:

(1) Upon entering the result phase of:
  (a) Read Data command
  (b) Read a Track command
  (c) Read ID command
  (d) Read Deleted Data command
  (e) Write Data command
  (f) Format a Cylinder command
  (g) Write Deleted Data command
  (h) Scan commands
(2) Ready line of FDD changes state
(3) End of Seek or Recalibrate command
(4) During execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in non-

DMA mode, DB_5 in the main status register is high. Upon entering the result phase this bit gets cleared. *Reasons 1 and 4 do not require Sense Interrupt Status* commands. The interrupt is cleared by reading/writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status command. This command, when issued, resets the Interrupt signal and, via bits 5, 6, and 7 of status register 0, identifies the cause of the interrupt. See table 9.

Table 9. Interrupt Status

Seek End	Interrupt Code		
Bit 5	Bit 6	Bit 7	Cause
0	1	1	Ready line changed state, either polarity
1	0	0	Normal termination of Seek or Recalibrate command
1	1	0	Abnormal termination of Seek or Recalibrate command

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no result phase. When the disk drive has reached the desired head position the μPD765A/μPD7265 will set the interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be seek end or a change in ready status from one of the drives. A graphic example is shown in figure 4.

Specify

The Specify command sets the initial values for each of the three internal timers. The HUT (head unload time) defines the time from the end of the execution phase of one of the Read/Write commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms... 0FH = 240 ms). The SRT (step rate time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (head load time) defines the time between when the head load signal goes high and the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms... 7F = 254 ms).

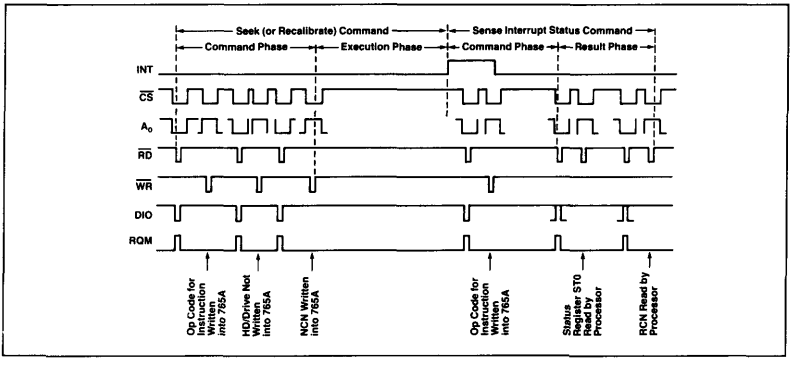
The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock; if the clock was reduced to 4 MHz (minifloppy application), then all time intervals are increased by a factor of 2.

The choice of a DMA or non-DMA operation is made by the ND (non-DMA) bit. When this bit is high (ND = 1) the non-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status regis-

Figure 4. Seek, Recalibrate, and Sense Interrupt Status



ter 3 contains the drive status information stored internally in FDC registers.

Invalid

If an Invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of status register 0 are set to 1 and 0, respectively. No interrupt is generated by the μPD765A/μPD7265 during this condition. Bits 6 and 7 (DIO and RQM) in the main status register are both 1 (high), indicating to the processor that the μPD765A/μPD7265 is in the result phase and the contents of status register 0 (ST0) must be read. When the processor reads status register 0 it will find an 80H, indicating an Invalid command was received.

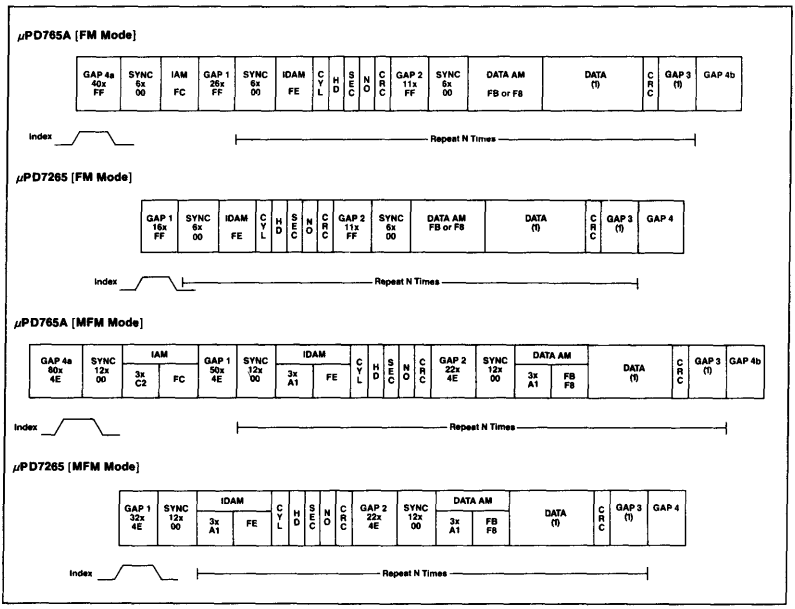
A Sense Interrupt Status command must be sent after a seek or recalibrate interrupt, otherwise the FDC will consider the next command to be an Invalid command.

In some applications the user may wish to use this command as a No-Op command to place the FDC in a standby or no operation state.

Data Format

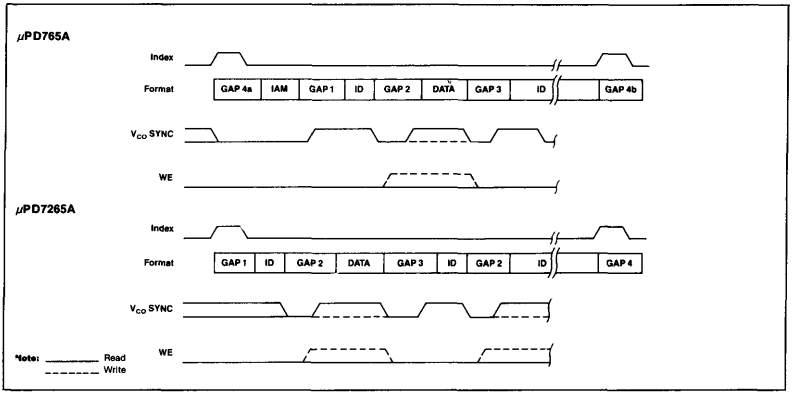
Figure 5 shows the data transfer format for the μPD765A and μPD7265 in various modes.

Figure 5. Data Format (Sheet 1 of 2)



Note: It is suggested that the user refer to the following application notes:
(1) #6 — for an example of an actual interface, as well as a "theoretical" data separator.
(2) #10 — for a well documented example of a working phase-locked loop.

Figure 5. Data Format (Sheet 2 of 2)



6

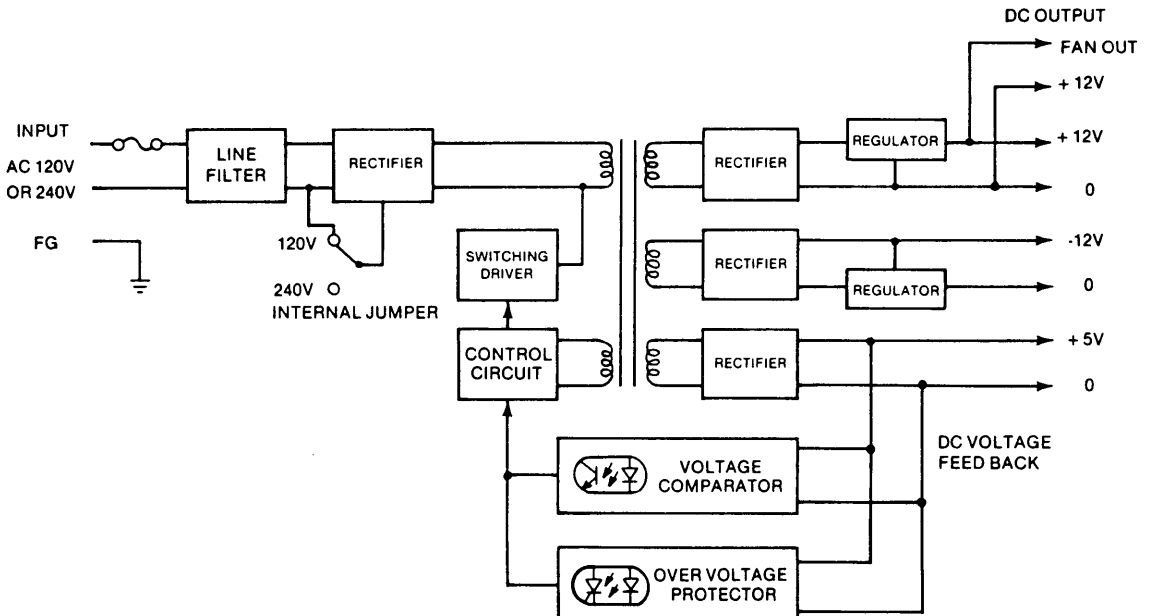
Power Supply

1000SL POWER SUPPLIES
(SINGLE AND DUAL INPUT)

1000SL 67 WATT SINGLE INPUT POWER SUPPLY

CONTENTS

Power Supply Block Diagram



Theory of Operation

AC Input Circuit

This circuit is composed of an AC Power Switch, a fuse, a line filter, and an inrush current limiting circuit and rectifying smoothing circuit. The inrush current limiting circuit controls the charging current to electrolytic capacitors when power is ON. The line filter reduces noise that leaks from the power source to the AC line or that returns from the unit to the power souce; it satisfies the specifications of noise regulations.

Control Circuit & Power Converter Circuit

This circuit is a self oscillation switching system, generally called an R.C.C. (Ringing Choke Converter). The R.C.C. circuit does not fix the oscillating frequency. Whenever input voltage is high or the load becomes light, the oscillating frequency will be high.

The current through R2 supplies transistor Q1's base, then Q1 turns ON. When transistor Q1 is On, the Q1 current excites the transformer T1 and voltage rises in the bias coil of T1(5-6) which leads transistor Q1 positive bias, then transistor Q1 turns ON.

When transistor Q1 turns ON, collector current charges the energy to primary inductance of transformer T1 (1-3). Increasing the collector current of transistor Q1 to the point of:

$$I_C > I_B .hfe$$

Then, transistor Q1 immediately turns OFF. In a moment, transformer T1 will have negative voltage which will be supplied to the secondary circuit through a rectifier. A Short Circuit Protector is provided to protect transistor Q1 from excess amounts of current when the secondary circuit becomes shorted. When transistor Q2 detects the voltage drop at R12, the collector of Q2 shorts the base and emitter of Q1. Then Q1 stops working so that the circuit protects Q1 from over current.

The over current protector in the -12V line is provided by the three terminal positive voltage regulator IC1 (built-in current fold back protection), which protects Q1 against excessive current from the -12V line.

Start-Up

Load power supply with minimum load as specified in Table 1. Bring up power slowly with the Variable Transformer while monitoring the +5 output with the oscilloscope and DVM. Supply should start with approximately 40-60 VAC applied, and should regulate when 90 VAC is reached. If output has reached 5 volts, do a performance test on operating characteristics, if there is no output, refer to "No output" section.

5V Output Voltage Detecting Circuit

The circuit detects the change of output load current compared with the output voltage and AC line input voltage, which feeds back to the control circuit through a photo coupler PHC1 to keep the output voltage stable. The Photo coupler isolates the primary and secondary circuits.

Over-Voltage Protection

When the +5 output voltage rises, between 5.8V to 6.8V, a control signal turns on the photo coupler PHC2 (Photo Thyristor) with the current of zener diode (D11) and stops oscillation by turning on Q3, which turns off Q1 in the switching circuit.

In the case of stopped oscillation, correct the cause of the failure, and reinput the power. The overvoltage protection circuit will reset automatically under good conditions.

The Photo Thyristor isolates the primary and secondary circuits.

Troubleshooting

Equipment for Test Set-Up

Isolation Transformer(minimum of 500 VA rating)

CAUTION

Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 500 VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

0-280V Variable Transformer (Variac)- Used to vary input voltage. Recommend 10 amp, 1.4 KVA rating, minimum.

Voltmeter- Need to measure DC voltages to 50 VDC and AC voltages to 200 VAC. Recommend two digital multimeters.

Oscilloscope- Need x 10 and x 100 probes.

Load board with connectors- See Table 1 for values of loads required. The entry on the table for Safe Load Power is the minimum power ratings for the load resistors used.

NOTE: Because of its design, this power supply must have a load present or damaging oscillations may result. Never test the power supply without a suitable load.

Ohmmeter

Set-Up Procedure

Set up as shown in Figure 1. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 output, with DVM's. Also monitor the +5 output with the oscilloscope using 500 mv/div sensitivity. The DVM monitoring the +5 output can also be used to check the other outputs. See text of "No output" section for the test points within the power supply.

Visual Inspection

Check power supply for any broken, burned, or obviously damaged components. Visually check fuse, if any question check with ohmmeter.

No Output

1. Check fuse:

   If fuse is blown, replace it but do not apply power until the cause of the failure is found.

2. Preliminary Check on Major Primary Components:

   Check diode bridge (D1), power transistor (Q1), and drive transistor (Q2,Q3) for shorted junctions. If any component is found shorted, replace it.

3. Preliminary Check on Major Secondary Components:

   Using an ohmmeter from an output that is common to each output and with output loads disconnected, check for shorted rectifiers or capacitors.

4. Check Over Voltage Protector:

   Read the output voltage with a DVM at the +5 output terminals by increasing the input voltage from 0V. Output voltage will appear at some input voltage and then go down to 0V again. Check the Diode D11 or Photo Coupler (PHC2).

5. Check Q1 Waveforms:

   Read waveform of Q1 Collector with oscilloscope at x 100 probe.

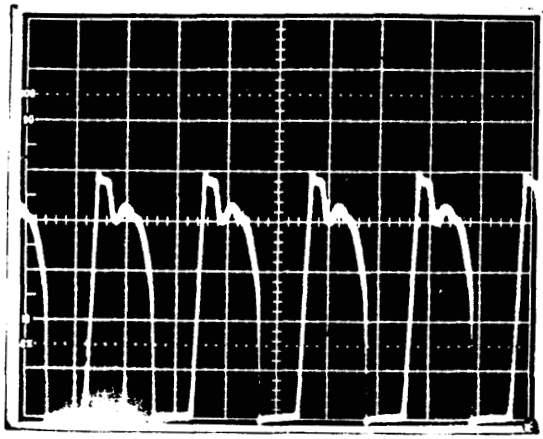
   Figure 2 is Q1 Collector normal waveform.

   Figure 3 is Q1 Base normal waveform.

   Figure 4 is the waveforms when shorted circuits of the secondary parts as listed in Table 2. Check listed parts according to the waveform.

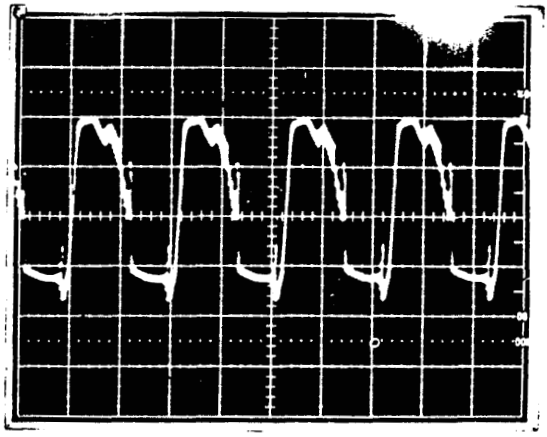
Collector Waveforms	Shorted Secondary Components
Figure 4	D8, D9, D10, C16, C17, C19, C20, C21, C22, C23

Table 2. List of Shorted Circuits



50V/DIV
5µs/DIV

Q1 Collector Waveforms (Input 90 VAC Minimum Load)



0.5V/DIV
5µs/DIV

Q1 Base Waveforms (Input 90 VAC Minimum Load)

OUTPUT	MINLOAD	LOAD R	SAFE LOAD POWER	MAX LOAD	LOAD R	SAFE LOAD POWER
+5 V	1.25 A	4 ohms	20 W	7.0 A	0.7 ohms	60 W
+12 V	0.15 A	80 ohms	5 W	2.4 A	5 ohms	50 W
-12 V	0	0	0	0.25 A	48 ohms	5 W

Table 1 Load Board Values (67 watt)

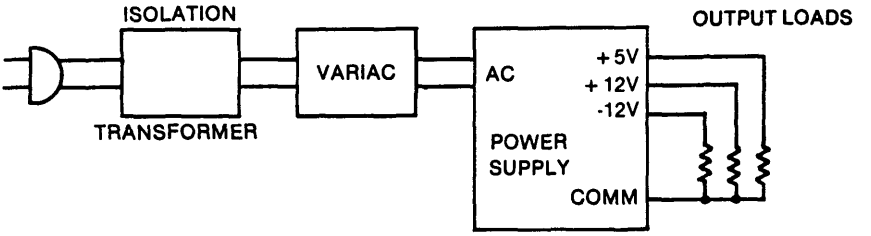
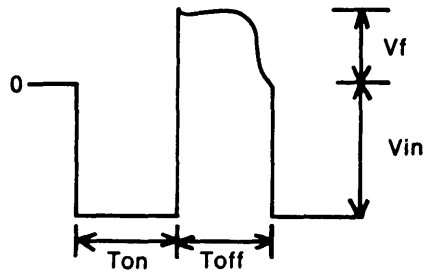


Figure 1 Test Setup

Waveforms

Power Converter Circuit



Collector Voltage Waveform

Collector Current Waveform

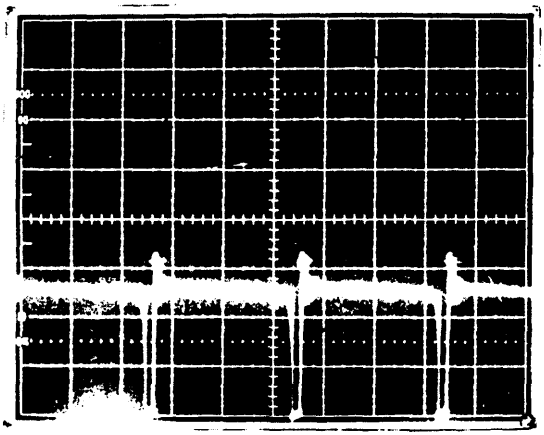
The input and output voltage are represented by the following equations:

Vo = n x Vf

Vo : Output voltage
n : Turn ratio of the transformer Tl
Vf : Collector Voltage at turn-off time

Vin x Ton = Vf x Toff

Vin : Input voltage
Ton : Turn-on time of transistor
Toff: Turn-off time of transistor



50V/DIV
5µs/DIV

Q1 Collector Waveforms -
Shorted Secondary Components (Input 90 VAC)

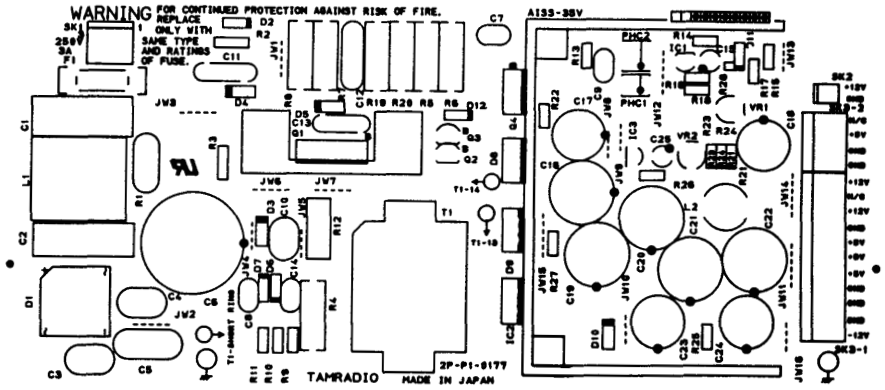
PARTS LIST FOR SWITCHING POWER SUPPLY UNIT

PART NO. 8790085

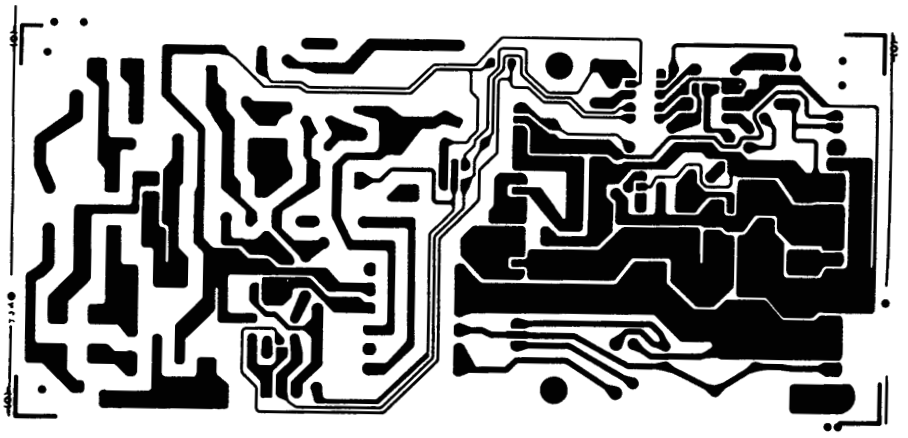
Symbol	Description			QTY	RS Part No.	Mfr's Part No.
CAPACITORS						
C1	Film	0.1uF	250VAC	1		XE-104
C2	Film	0.22uF	250VAC	1		XE-224
C3/4/11	Ceramic	2200pF	400VAC	3		DE7100F222MVA1-KC or CS13-E2GA222MYAS
C5	Ceramic	10000pF	400VAC	1		DE7150FZ103PVA1-KC or CS17-F2GA103ZYAS
C6	Electrolytic	680uF	200WV	1		CETSW2D681 or 200LPSS680
C7/8/9	Film	0.047uF	50V	3		50F2D473K or AMZF473K50V
C10	Film	0.1uF (0.1-0.22uF)	50V	1		50F2D104K or AMZF104K50V (Adjust 104K-224K)
C12	Film	0.22uF	250V	1		250MW224K
C13	Ceramic	1500pF	2KV	1		DE1210R152K2K or CK45-B3DD152KYAR
C15/25	Electrolytic	1uF	50WV	2		CEUSM1H010
C16	Electrolytic	2200uF	25WV	1		CEUSM1E222
C17/23/24	Electrolytic	470uF	25WV	3		CEUSM1E471
C18	Electrolytic	1000uF	16WV	1		CEUSM1C102
C19/20/21	Electrolytic	4700uF	10WV	3		CEUSM1A472
C22	Electrolytic	2200uF	10WV	1		CEUSM1A222
CONNECTORS						
SK1	Connector, 2 conductors Input			1		5277-02A
SK2	Connector, 2 conductors Fan-out			1		5045-02F
SK3-1	Connector, 10 conductors Output			1		5277-10A
SK3-2	Connector, 4 conductors Output			1		5273-04A
DIODES						
D1	Silicon, Stack	400V	4A	1		S4VB40 or RB404 or DBA40E
D2/11	Silicon	5V	400mW	2		HZ5B3
D3/4/5	Silicon	600V	1A	3		FI-06 or V19G
D6/7	Silicon	100V	200mA	2		DS446 or 1S954
D8	Silicon, Stack	200V	5A	1		D5LCA20 or 5CH2SM

Symbol	Description			QTY	RS Part No.	Mfr's Part No.
D9	Silicon, Stack	40V	10A	1		D10SC4M or 10CS04SM
FUSE						
F1	Fuse,	250V	3A	1		MT4 3A250V
	Fuse Clip			2		P#5722113
HEATSINK						
HS1	Heatsink, for Q1			1		40-08440-01
HS2	Heatsink, for D8/D9/Q4/IC2			1		4P-D2-0180
INDUCTORS						
L1	Choke Coil	8mH		1		TO-9161-1 or TO-9161
L2	Choke Coil	4.3uH		1		PSC-156
INTEGRATED						
IC1	IC, Regulator	37V	150mA	1		TL431CLPB or uA431AWC
IC2	IC, Regulator	12V	0.5A	1		L78M12 or NJM78M12
IC3	IC, Regulator	36V	30mA	1		M5236L
PHOTO COUPLERS						
PHC-1	Photo Coupler	35V	50mA	1		TLP521-1 or PC817
PHC-2	Photo Coupler	400V	150mA	1		TLP541G or S22MD1
PRINTED CIRCUIT BOARD						
PC1	Printed Circuit Board 105°C		XPC	1		2P-P1-0177
RESISTORS						
R1	Thermistor	8	1.6A	1		117-080-45202 or 8D-11 or D4FFL8ROP
R2/3	Carbon	100K	1/2W	2		RD50P100KohmsJ or RD50S100KohmsJ
R4	Metal-oxide	27 (10-56)	2W	1		RSF2B27ohmsJ (Adjust 10-56ohms)
R5/6/19/20	Metal-oxide	27K	2W	4		RSF2B27KohmsJ

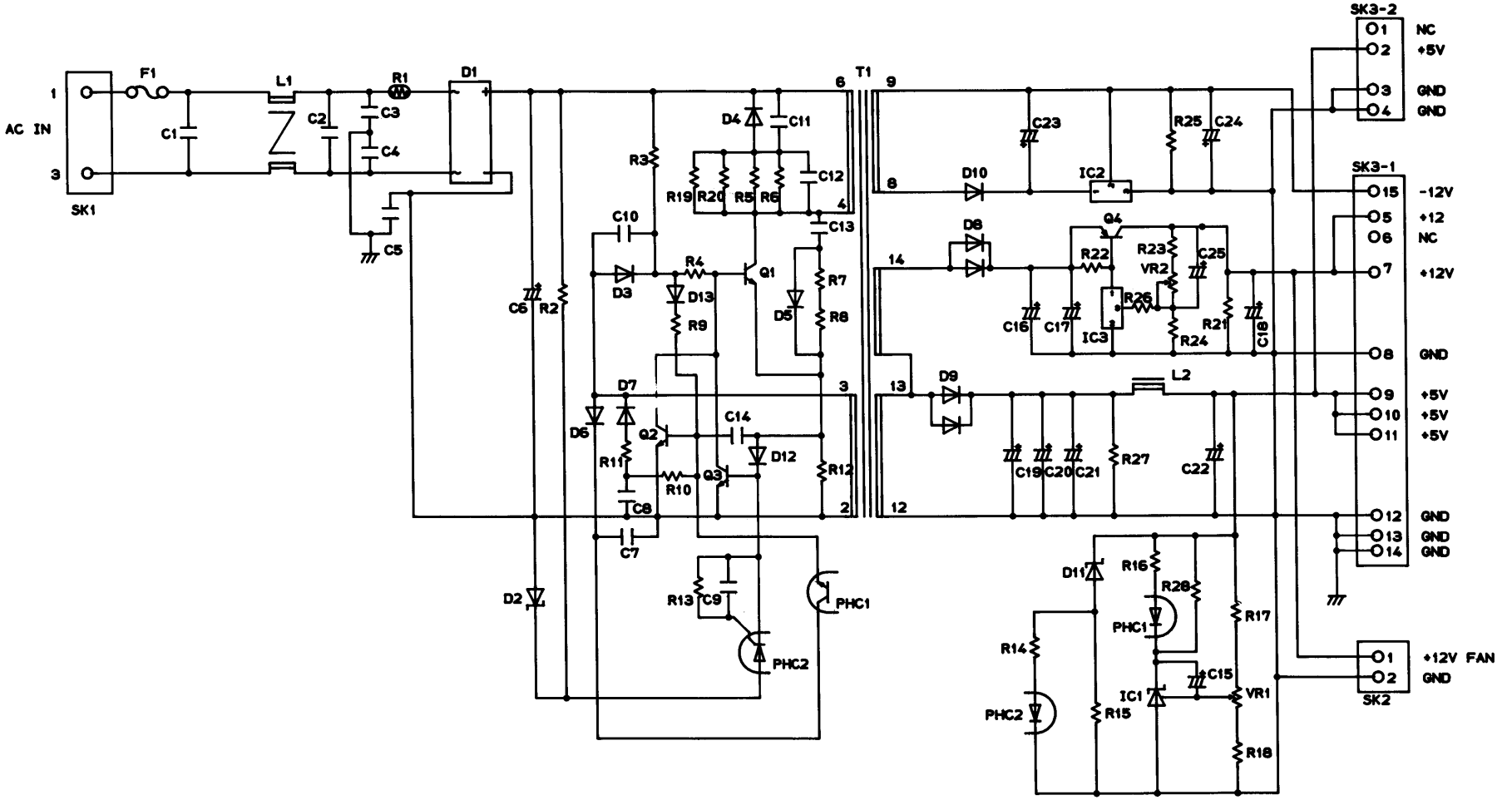
Symbol	Description			QTY	RS Part No.	Mfr's Part No.
R7/8	Metal-oxide	470	2W	2		RSF2B470ohmsJ
R9	Carbon	560 (330-750)	1/4W	1		RD25P560ohmsJ or RD25S560ohmsJ (Adjust 330-750ohms)
R10	Carbon	270 (180-470)	1/4W	1		RD25P270ohmsJ or RD25S270ohmsJ (Adjust 180-470ohms)
R11	Carbon	47	1/4W	1		RD25P47ohmsJ or RD25S47ohmsJ
R12	Cement	0.27	5W	1		MPC71 0.27ohmsK
R13	Carbon	27K	1/4W	1		RD25P27KohmsJ or RD25S27KohmsJ
R14	Carbon	39	1/4W	1		RD25P39ohmsJ or RD25S39ohmsJ
R15	Carbon	180	1/4W	1		RD25P180ohmsJ or RD25S180ohmsJ
R16	Carbon	100	1/4W	1		RD25P100ohmsJ or RD25S100ohmsJ
R17/18/21/24	Carbon	2.2K	1/4W	4		RD25P2.2KohmsJ or RD25S2.2KohmsJ
R22/27	Carbon	220	1/4W	2		RD25P220ohmsJ or RD25S220ohmsJ
R23	Carbon	18K	1/4W	1		RD25P18KohmsJ or RD25S18KohmsJ
R25	Carbon	1K	1/4W	1		RD25P1KohmsJ or RD25S1KohmsJ
R26	Carbon	15K	1/4W	1		RD25P15KohmsJ or RD25S15KohmsJ
R28	Carbon	1K	1/6W	1		RD16P1KohmsJ or RD16S1KohmsJ
VR1/2	Variable	2K	0.5W	2		V6EK-PV(1S)202B or H0615-222B
TRANSFORMER						
T1	Transformer			1		TO-4342
TRANSISTORS						
Q1	Transistor	400V	12A	1		2SC2833 or 2SC2938
Q2/3	Transistor	50V	2A	2		2SD1207 or 2SC2655
Q4	Transistor	60V	5A	1		2SA1441 or 2SB1019



Power Supply PCB - Silkscreen



Power Supply PCB - Component Side



model no. 8790085

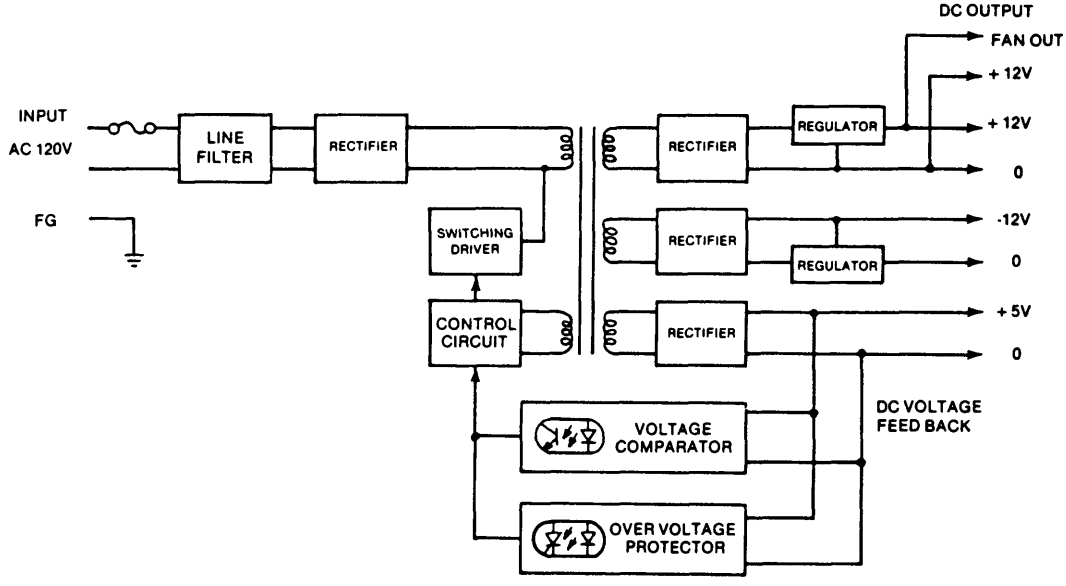
1000SL 67 WATT DUAL INPUT POWER SUPPLY

1000SL 67 WATT DUAL INPUT POWER SUPPLY

CONTENTS

	MINIMUM	TYPICAL	MAXIMUM	UNITS
Operating Voltage Range	90 198	120 240	135 264	VAC
Line Frequency	47	50/60	63	Hz
Output Voltages				
Vol	4.85	5.00	5.15	V
Vo2	11.40	12.00	12.60	V
Vo3	-13.20	-120.00	-10.80	V
Output Loads				
Iol	1.25	-	7.0	A
Io2	0.15	-	2.4	A
Io3	0	-	0.25	A
Over Current Protection				
Current Limit ICL1	-	-	14.0	A
ICL2	-	-	4.8	A
ICL3	-	-	1.0	A
Over Voltage Protection				
Crowbar	5.8	-	6.8	V
Output Noise				
Vol	-	-	50	mV P-P
Vo2	-	-	100	mV P-P
Vo3	-	-	150	mV P-P
Efficiency	63	65	-	%
Holdup Time				
Full Load at Nominal Line	16	-	-	mSec.
Insulation Resistance				
Input to Output	7	1000	-	M ohms
Input to Ground	7	1000	-	M ohms
Isolation				
Input to Ground	1.25	-	-	KVAC
Input to Output	3.75	-	-	KVAC

Power Supply Block Diagram



Theory of Operation

AC Input Circuit

This circuit is composed of an AC Power Switch, a fuse, a line filter, and an inrush current limiting circuit and rectifying smoothing circuit. The inrush current limiting circuit controls the charging current to electrolytic capacitors when power is ON. The line filter reduces noise that leaks from the power source to the AC line or that returns from the unit to the power souce; it satisfies the specifications of noise regulations.

Control Circuit & Power Converter Circuit

This circuit is a self oscillation switching system, generally called an R.C.C. (Ringing Choke Converter). The R.C.C. circuit does not fix the oscillating frequency. Whenever input voltage is high or the load becomes light, the oscillating frequency will be high.

The current through R4 and R5 supplies transistor Q1's base, then Q1 turns ON. When transistor Q1 is On, the Q1 current excites the transformer T1 and voltage rises in the bias coil of T1(2-3) which leads transistor Q1 positive bias, then transistor Q1 turns ON.

When transistor Q1 turns ON, collector current charges the energy to primary inductance of transformer T1 (4-6). Increasing the collector current of transistor Q1 to the point of:

$$I_C > I_B .hfe$$

Then, transistor Q1 immediately turns OFF. In a moment, transformer T1 will have negative voltage which will be supplied to the secondary circuit through a rectifier. A Short Circuit Protector is provided to protect transistor Q1 from excess amounts of current when the secondary circuit becomes shorted. When transistor Q2 detects the voltage drop at R13, the collector of Q2 shorts the base and emitter of Q1. Then Q1 stops working so that the circuit protects Q1 from over current.

The over current protector in the -12V line is provided by the three terminal positive voltage regulators IC2, IC3 (built-in current fold back protection), which protects Q1 against excessive current from the -12V line.

Start-Up

Load power supply with minimum load as specified in Table 1. Check up on the voltage selector jumper and don't apply over voltage. Bring up power slowly with the Variable Transformer while monitoring the +5 output with the oscilloscope and DVM. Supply should start with approximately 40-60/80-120 VAC applied, and should regulate when 90/180 VAC is reached. If output has reached 5 volts, do a performance test on operating characteristics, if there is no output, refer to "No output" section.

5V Output Voltage Detecting Circuit

The circuit detects the change of output load current compared with the output voltage and AC line input voltage, which feeds back to the control circuit through a photo coupler PHCl to keep the output voltage stable. The Photo coupler isolates the primary and secondary circuits.

Over-Voltage Protection

When the +5 output voltage rises, between 5.8V to 6.8V, a control signal turns on the photo coupler PHC2 (Photo Thyristor) with the current of zener diode (Dll) and stops oscillation by turning on Q3, which turns off Ql in the switching circuit.

In the case of stopped oscillation, correct the cause of the failure, and reinput the power. The overvoltage protection circuit will reset automatically under good conditions.

The Photo Thyristor isolates the primary and secondary circuits.

Troubleshooting

Equipment for Test Set-Up

Isolation Transformer(minimum of 500 VA rating)

CAUTION

Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 500 VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

0-280V Variable Transformer (Variac)- Used to vary input voltage. Recommend 5 amp, 1.4 KVA rating, minimum.

Voltmeter- Need to measure DC voltages to 50 VDC and AC voltages to 300 VAC. Recommend two digital multimeters.

Oscilloscope- Need x 10 and x 100 probes.

Load board with connectors- See Table 1 for values of loads required. The entry on the table for Safe Load Power is the minimum power ratings for the load resistors used.

NOTE: Because of its design, this power supply must have a load present or damaging oscillations may result. Never test the power supply without a suitable load.

Ohmmeter

Set-Up Procedure

Set up as shown in Figure 1. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 output, with DVM's. Also monitor the +5 output with the oscilloscope using 500 mv/div sensitivity. The DVM monitoring the +5 output can also be used to check the other outputs. See text of "No output" section for the test points within the power supply.

Visual Inspection

Check power supply for any broken, burned, or obviously damaged components. Visually check fuse, if any question check with ohmmeter.

No Output

1. Check fuse:

   If fuse is blown, replace it but do not apply power until the cause of the failure is found.

2. Preliminary Check on Major Primary Components:

   Check diode bridge (D1), power transistor (Q1), and drive transistors (Q2,Q3) for shorted junctions. If any component is found shorted, replace it.

3. Preliminary Check on Major Secondary Components:

   Using an ohmmeter from an output that is common to each output and with output loads disconnected, check for shorted rectifiers or capacitors.

4. Check Over Voltage Protector:

   Read the output voltage with a DVM at the +5 output terminals by increasing the input voltage from 0V. Output voltage will appear at some input voltage and then go down to 0V again. Check the Diode D11 or Photo Coupler (PHC2).

5. Check Q1 Waveforms:

   Read waveform of Q1 Collector with oscilloscope at x 100 probe.

   Figure 2 is Q1 Collector normal waveform.

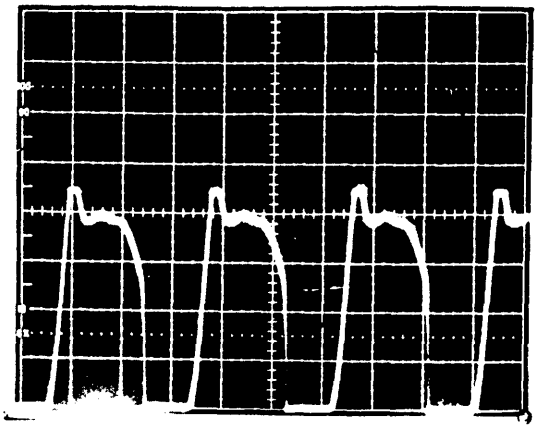
   Figure 3 is Q1 Base normal waveform.

   Figure 4 is the waveforms when shorted circuits of the secondary parts as listed in Table 2. Check listed parts according to the waveform.

Collector Waveforms	Shorted Secondary Components
Figure 4	D8, D9, C17, C18, C20, C21, C22, C23,

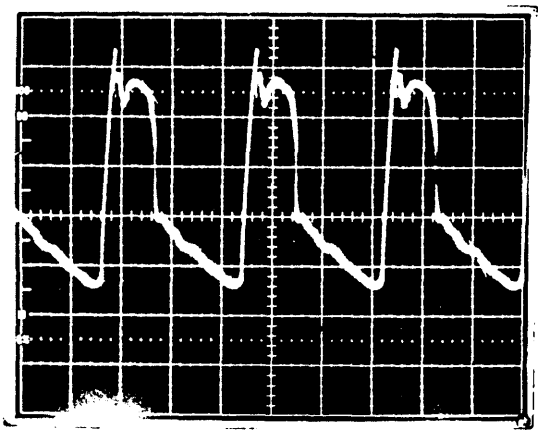
Table 2. List of Shorted Circuits

6. Check Resistor (R26)
   If R26 is open, check D10, C24,and IC2.



100V/DIV
5µs/DIV

Q1 Collector Waveforms (Input 90 VAC Minimum Load)



0.5V/DIV
5µs/DIV

Q1 Base Waveforms (Input 90 VAC Minimum Load)

OUTPUT	MINLOAD	LOAD R	SAFE LOAD POWER	MAX LOAD	LOAD R	SAFE LOAD POWER
+5 V	1.25 A	4 ohms	20 W	7.0 A	0.7 ohms	60 W
+12 V	0.15 A	80 ohms	5 W	2.4 A	5 ohms	50 W
-12 V	0	0	0	0.25 A	48 ohms	5 W

Table 1 Load Board Values (67 watt)

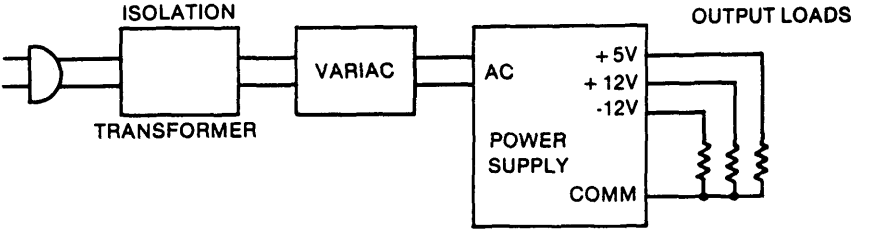
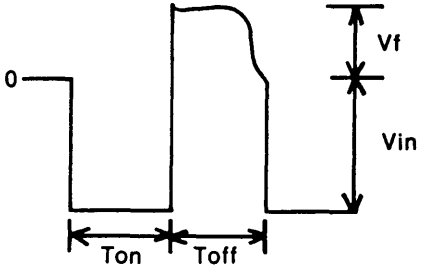


Figure 1 Test Setup

Waveforms

Power Converter Circuit



Collector Voltage Waveform

Collector Current Waveform

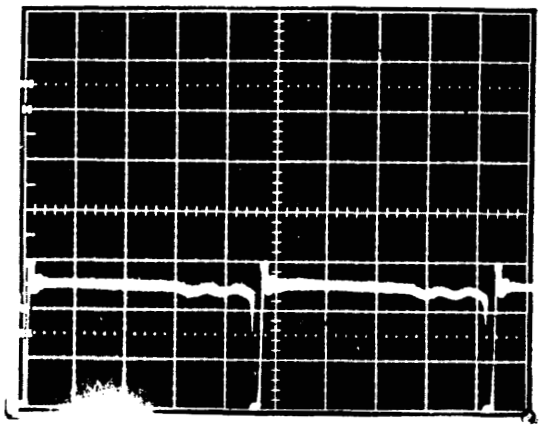
The input and output voltage are represented by the following equations:

Vo = n x Vf

Vo : Output voltage
n : Turn ratio of the transformer Tl
Vf : Collector Voltage at turn-off time

Vin x Ton = Vf x Toff

Vin : Input voltage
Ton : Turn-on time of transistor
Toff: Turn-off time of transistor



100V/DIV
5µs/DIV

Q1 Collector Waveforms -
Shorted Secondary Components (Input 90 VAC)

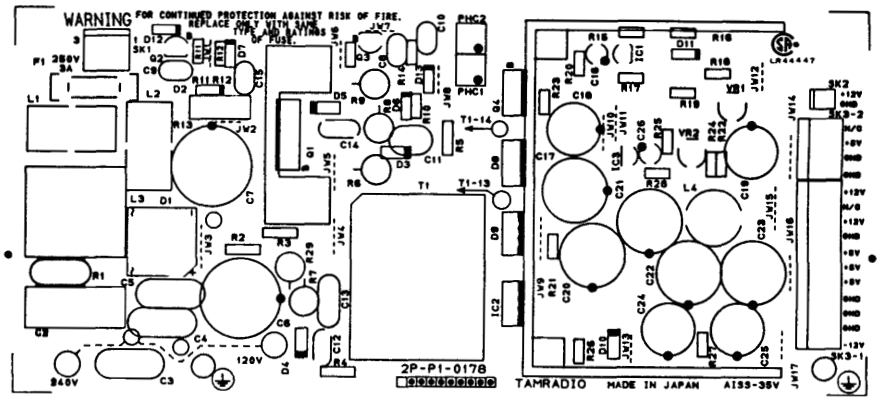
PARTS LIST FOR SWITCHING POWER SUPPLY UNIT

PART NO. 8790084

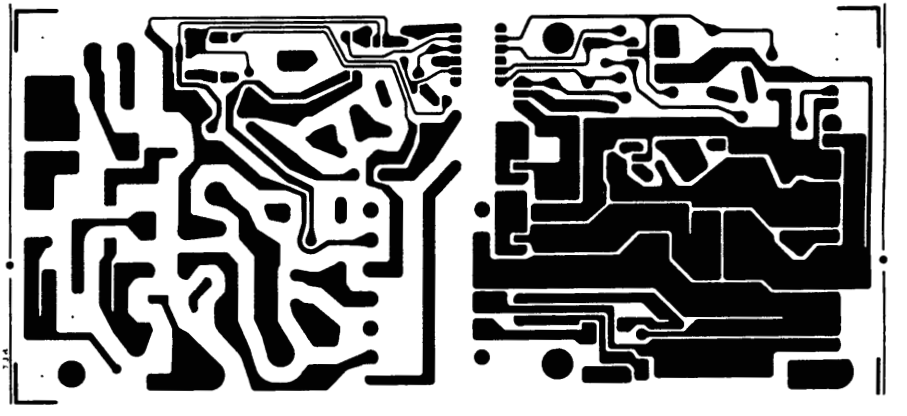
Symbol	Description			QTY	RS Part No.	Mfr's Part No.
CAPACITORS						
C2	Film	0.22uF	400VAC	1		XE-224
C3/4	Ceramic	4700pF	400VAC	2		DE7150F472MVA1-KC or CS17-E2GA472MY.S
C5	Ceramic	10000pF	400VAC	1		DE7150FZ103PVA1-KC or CS17-F2GA103ZYAS
C6/7	Electrolytic	330uF	200WV	2		CETSW2D331 or 200LPSS330
C8/9/10/15	Film	0.047uF	50V	4		50F2D473K or AMZF473K50V
C11	Film	0.1uF (0.1-0.22uF)	50V	1		50F2D104K or AMZF104K50V
C12	Ceramic	470pF	2KV	1		DE0907R471K2K or CK45-B3DD471KYAR
C13	Film	0.01uF	630V	1		CF921L2J103K or MDDZ2J103K
C14	Ceramic	680pF	2KV	1		DE1010R681K2K or CK45-B3DD681KYAR
C16/26	Electrolytic	1uF	50WV	2		CEUSM1H010
C17	Electrolytic	2200uF	25WV	1		CEUSM1E222
C18/24/25	Electrolytic	470uF	25WV	3		CEUSM1E471
C19	Electrolytic	1000uF	16WV	1		CEUSM1C102
C20/21/22	Electrolytic	4700uF	10WV	3		CEUSM1A472
C23	Electrolytic	2200uF	10WV	1		CEUSM1A222
CONNECTORS						
SK1	Connector, 2 conductors Input			1		5277-02A
SK2	Connector, 2 conductors Fan-out			1		5045-02F
SK3-1	Connector, 10 conductors Output			1		5277-10A
SK3-2	Connector, 4 conductors Output			1		5273-04A
	Pin Terminal, Voltage Selector			2		RT-01N-2.3A
	Jumping Connector			1		4P-M3-0017
DIODES						
D1	Silicon, Stack	600V	3A	1		S3WB60
D2/11	Silicon, Zener	5V	400mW	2		HZ5B3
D3/10	Silicon	600V	1A	2		FI-06 or V19C
D4/5	Silicon	800V	1A	2		FI-08 or RU2B
D6/7/13	Silicon	100V	200mA	3		DS446 or 1S954

Symbol	Description			QTY	RS Part No.	Mfr's Part No.
D8	Silicon, Stack	200V	5A	1		D5LCA20 or 5CH2SM
D9	Silicon, Stack	40V	10A	1		D10SC4M or 10CS04SM
FUSE						
F1	Fuse	250V	3A	1		MT4 3A250V
	Fuse Clip			2		P#5722113
HEATSINK						
HS1	Heatsink, for Q1			1		40-08440-01
HS2	Heatsink, for D8/D9/Q4/IC2			1		4P-D2-0180
INDUCTORS						
L1/2	Choke Coil	0.5mH		2		TO-9175
L3	Choke Coil	8mH		1		TO-9161
L4	Choke Coil	4.3uH		1		PSC-156
INTEGRATED CIRCUITS						
IC1	IC, Regulator	37V	150mA	1		TL431CLPB or uA431AWC
IC2	IC, Regulator	12V	0.5A	1		L78M12 or NJM78M12
IC3	IC, Regulator	36V	30mA	1		M5236L
PHOTO COUPLER						
PHC1	Photo Coupler	55V	60mA	1		TLP732 or PC111
PHC2	Photo Coupler	600V	150mA	1		TLP741J
PRINTED CIRCUIT BOARD						
PC1	Printed Circuit Board 105°C		XPC	1		2P-P1-0178
RESISTORS						
R1	Thermister	16	1.2A	1		117-160-45201 or 16D-13 or D4FFL160P
R2/3/4/5	Carbon	100K	1/2W	4		RD50P100KohmsJ or RD50S100KohmsJ
R6	Metal-oxide	47 (15-68)	2W	1		RSF2B47ohmsJ (Adjust 15-68ohms)

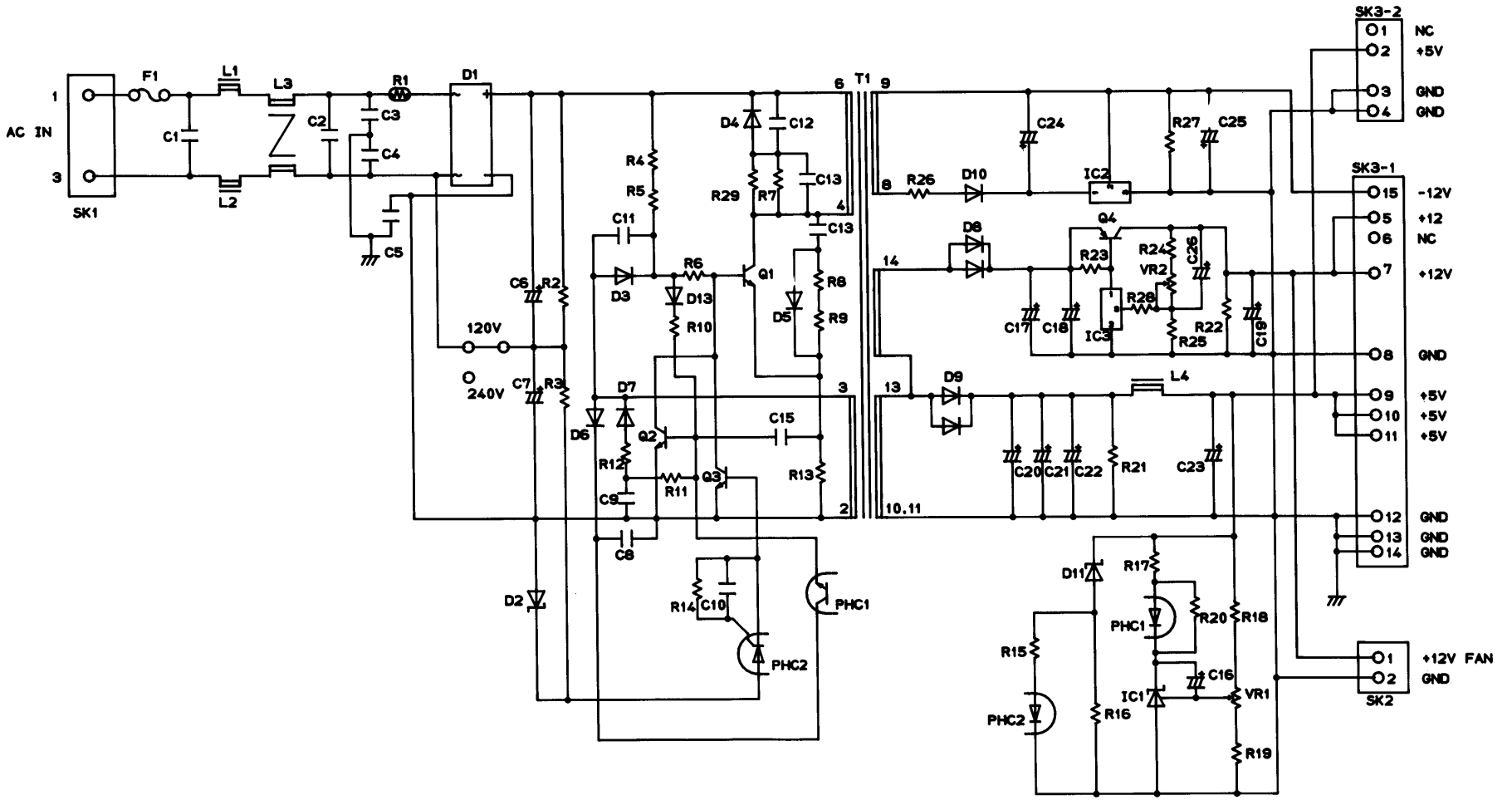
Symbol	Description			QTY	RS Part No.	Mfr's Part No.
R7/29	Metal-oxide	100K	2W	2		RSF2B100KohmsJ
R8/9	Metal-oxide	100	2W	2		RSF2B100ohmsJ
R10	Carbon	560 (330-680)	1/4W	1		RD25P560ohmsJ or RD25S560ohmsJ (Adjust 330-680ohms)
R11	Carbon	330 (220-560)	1/4W	1		RD25P330ohmsJ or RD25S330ohmsJ (Adjust 220-560ohms)
R12	Carbon	47	1/4W	1		RD25P47ohmsJ or RD25S47ohmsJ
R13	Cement	0.56	5W	1		MPC71 0.56ohmsK
R14	Carbon	27K	1/4W	1		RD25P27Kohms or RD25S27KohmsJ
R15	Carbon	39	1/4W	1		RD25P39ohmsJ or RD25S39ohmsJ
R16	Carbon	180	1/4W	1		RD25P180ohmsJ or RD25S180ohmsJ
R17	Carbon	100	1/4W	1		RD25P100ohmsJ or RD25S100ohmsJ
R18/19/22	Carbon	2.2K	1/4W	3		RD25P2.2KohmsJ or RD25S2.2KohmsJ
R20/27	Carbon	1K	1/4W	2		RD25P1KohmsJ or RD25S1KohmsJ
R21/23	Carbon	220	1/4W	2		RD25P220ohmsJ or RD25S220ohmsJ
R24	Carbon	18K	1/4W	1		RD25P18KohmsJ or RD25S18KohmsJ
R26	Fusing	1	1/4W	1		RF25S1ohmsJ
R28	Carbon	15K	1/4W	1		RD25P15KohmsJ or RD25S15KohmsJ
VR1/2	Variable	2K	0.5W	2		V6EK-PV(1S)202B or H0615-222B
TRANSFORMER						
T1	Transformer			1		TO-4341
TRANSISTORS						
Q1	Transistor	800V	6A	1		2SC3460 or 2SC3680
Q2/3	Transistor	50V	2A	2		2SD1207 or 2SC2655
Q4	Transistor	60V	5A	1		2SA1441 or 2SB1019



Power Supply PCB - Silkscreen



Power Supply PCB - Component Side



model no. 8790084

Keyboard

FUJITSU KEYBOARD
ASSEMBLY # N860-4703-T

1.0 GENERAL

The keyboard is a direct, plug-compatible replacement for the Enhanced Keyboard for the IBM PC, XT, and AT personal computer. No software modification or special interface is needed by the user.

2.0 SCOPE

This specification describes the functional, mechanical, electrical, environmental, and reliability characteristics of the FUJITSU N860-4703-T Keyboard assembly.

The keyboard is encoded in such a way as to produce a unique output code for each key that is pressed and/or released. The communication with the host computer is a synchronous serial link. The Key Layout, Switch Encoding and Serial Communication are all compatible with the IBM PC, XT and AT.

3.0 MECHANICAL SPECIFICATION

3.1 Key Layout, Legends, and Colors

Figure 1 shows keytop layout, appropriate legends and keytop colors. The keys are numbered from left to right starting with the spacebar row (Row A) and ending with the function key row (Row F).

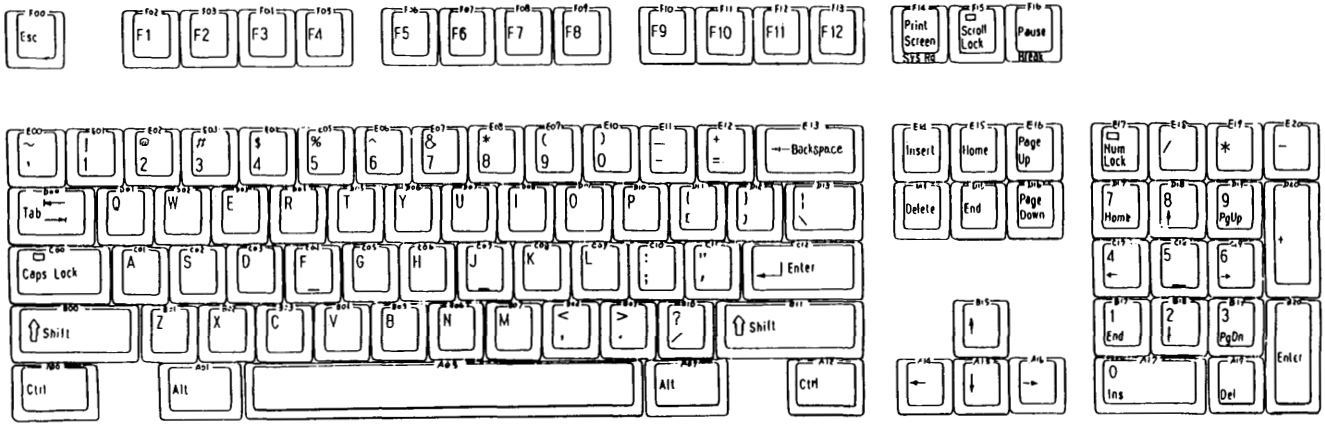

Esc
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
F11
F12
Print Screen
Scroll Lock
Pause
Backspace
Tab
Caps Lock
Enter
Shift
Shift
Ctrl
Alt
Alt
Ctrl
Insert
Home
Page Up
Delete
End
Page Down
Num Lock
7 Home
8
9 PgUp
4
5
6
1 End
2
3 PgDn
0 Ins
Del
Enter

FIGURE 1

3.2 KEYSWITCH

3.2.1 Total Travel: 0.150", +/- 0.020" (3.8, +/-0.5mm)

3.2.2 FORCE: All keyswitches shall utilize a 2.0 ounce (+/- 0.9 oz) operating force. This is accomplished using both a rubber keyswitch membrane and springs.

3.2.3 BREAKOVER FEEDBACK: The keyswitches utilize a tactile feedback to assure the operator that the key has been fully pressed.

4.0 FUNCTIONAL REQUIREMENTS

4.1 SCAN CODES

The keyboard generates a unique Hex scan code for each keyswitch that is pressed (make code) and released (break code). For the AT Mode, the break code is the same as the make code preceded by "F0" Hex. Example: The make code for the "ESC" key is 76 Hex and the break code is two bytes, F0 76 Hex. For the XT Mode, the break code is 80 Hex, plus the make code. Example: The make code for the "ESC" key is 01 Hex and the break code is 81 Hex. The keyswitch-to-scan-code (make and break codes) assignments, Standard ASCII Codes, and Extended ASCII Codes are listed on the following pages.

KEYBOARD SCAN CODES

Key #	Key Descript.	AT Mode Make Code	AT Mode Break Code	XT Mode Make Code	XT Mode Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
1	Esc	76	F076	01	81	011B	011B	011B	-----	011B	011B	011B	0100
2	F1	05	F005	3B	BB	3B00	5400	5E00	6800	3B00	5400	5E00	6800
3	F2	06	F006	3C	BC	3C00	5500	5F00	6900	3C00	5500	5F00	6900
4	F3	04	F004	3D	BD	3D00	5600	6000	6A00	3D00	5600	6000	6A00
5	F4	0C	F00C	3E	BE	3E00	5700	6100	6B00	3E00	5700	6100	6B00
6	F5	03	F003	3F	BF	3F00	5800	6200	6C00	3F00	5800	6200	6C00
7	F6	0B	F00B	40	C0	4000	5900	6300	6D00	4000	5900	6300	6D00
8	F7	83	F083	41	C1	4100	5A00	6400	6E00	4100	5A00	6400	6E00
9	F8	0A	F00A	42	C2	4200	5B00	6500	6F00	4200	5B00	6500	6F00
10	F9	01	F001	43	C3	4300	5C00	6600	7000	4300	5C00	6600	7000
11	F10	09	F009	44	C4	4400	5D00	6700	7100	4400	5D00	6700	7100
12	F11	78	F078	57	D7	-----	-----	-----	-----	8500	8700	8900	8B00
13	F12	07	F007	58	D8	-----	-----	-----	-----	8600	8800	8A00	8C00
14	Print Scrn	E07C	E0F07C	E02AE037	E0B7E0AA	Note[1]	Note[1]	7200	-----	Note[2]	Note[2]	7200	-----
15	Scroll Lock	7E	F07E	46	C6	Note[2]	Note[2]	------	Note[2]	Note[3]	Note[3]	-----	Note[2]
16	Pause Break	E11477	E1F014F077	E11D45	E19DC5	Note[3]	Note[3]	Note[4]	Note[3]	Note[3]	Note[3]	Note[4]	Note[3]
17	~ or \	0E	F00E	2B	AB	2960	297E	-----	-----	6000	7E00	-----	2900
18	! or 1	16	F016	02	82	0231	0221	-----	7800	0231	0221	-----	7800

Table 1

KEYBOARD SCAN CODES

Key #	Key Descript.	AT Mode Make Code	AT Mode Break Code	XT Mode Make Code	XT Mode Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
19	@ or 2	1E	F01E	03	83	0332	0340	0300	7900	0332	0340	0300	7900
20	# or 3	26	F026	04	84	0433	0423	-----	7A00	0433	0423	-----	7A00
21	$ or 4	25	F025	05	85	0534	0524	-----	7B00	0534	0524	-----	7B00
22	% or 5	2E	F02E	06	86	0635	0625	-----	7C00	0635	0625	-----	7C00
23	^ or 6	36	F036	07	87	0736	075E	071E	7D00	0736	075E	071E	7D00
24	& or 7	3D	F03D	08	88	0837	0826	-----	7E00	0837	0826	-----	7E00
25	* or 8	3E	F03E	09	89	0938	092A	-----	7F00	0938	092A	-----	7F00
26	(or 9	46	F046	0A	8A	0A39	0A28	-----	8000	0A39	0A28	-----	8000
27	) or 0	45	F045	0B	8B	0B34	0B29	-----	8100	0B34	0B29	-----	8100
28	_ or -	4E	F04E	0C	8C	0C2D	0C5F	0C1F	8200	0C2D	0C5F	0C1F	8200
29	+ or =	55	F055	0D	8D	0D3D	0D2B	-----	8300	0D3D	0D2B	-----	8300
30	Backspace	66	F066	0E	8E	0E08	0E08	0E7F	-----	0E08	0E08	0E7F	0E00
31	Insert	E070	E0F070	E02AE052	E0D2E0AA	5200	5200	-----	-----	52E0	52E0	92E0	A200
32	Home	E06C	E0F06C	E02AE047	E0C7E0AA	4700	4700	7700	-----	47E0	47E0	77E0	9700
33	Pg Up	E07D	E0F07D	E02AE049	E0C9E0AA	4900	4900	8400	-----	49E0	49E0	84E0	9900
34	Num Lock	77	F077	45	C5	Note[5]	Note[5]	-----	Note[5]	Note[5]	Note[5]	----	Note[5]
35	/	E04A	E0F04A	E035	E0B5	352F	352F	-----	-----	E02F	E02F	9500	A400
36	*	7C	F07C	37	B7	372A	372A	-----	-----	372A	372A	9600	3700
37	-	7B	F07B	4A	CA	4A2D	4A2D	-----	-----	4A2D	4A2D	8E00	4A00

KEYBOARD SCAN CODES

Key #	Key Descript.	AT Mode Make Code	AT Mode Break Code	XTMode Make Code	XTMode Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
38	Tab	0D	F00D	0F	8F	0F90	0F00	-----	-----	0F09	0F00	9400	A500
39	Q or q	15	F015	10	90	1071	1051	1011	1000	1071	1051	1011	1000
40	W or w	1D	F01D	11	91	1177	1157	1117	1100	1177	1157	1117	1100
41	E or e	24	F024	12	92	1265	1245	1205	1200	1265	1245	1205	1200
42	R or r	2D	F02D	13	93	1372	1352	1312	1300	1372	1352	1312	1300
43	T or t	2C	F02C	14	94	1474	1454	1414	1400	1474	1454	1414	1400
44	Y or y	35	F035	15	95	1579	1559	1519	1500	1579	1559	1519	1500
45	U or u	3C	F03C	16	96	1675	1655	1615	1600	1675	1655	1615	1600
46	I or i	43	F043	17	97	1769	1749	1709	1700	1769	1749	1709	1700
47	O or o	44	F044	18	98	186F	184F	180F	1800	186F	184F	180F	1800
48	P or p	4D	F04D	19	99	1970	1950	1910	1900	1970	1950	1910	1900
49	{ or [	54	D054	1A	9A	1A5B	1A7B	1A1B	-----	1A5B	1A7B	1A1B	1A00
50	} or]	5B	F05B	1B	9B	1B5D	1B7D	1B1D	-----	1B5D	1B7D	1B1D	1B00
51	| or \	5D	F05D	2B	AB	2B5C	2B7C	2B1C	-----	2B5C	2B7C	2B1C	2B00
52	Delete	E071	E0F071	E02AE053	E0D3E0AA	5300	5300	-----	-----	53E0	53E0	93E0	A300
53	End	E069	E0F069	E02AE04F	E0CFE0AA	4F00	4F00	7500	-----	4FE0	4FE0	75E0	9F00
54	Page Down	E07A	E0F07A	E02AE051	E0D1E0AA	5100	5100	7600	-----	51E0	51E0	76E0	A100
55	7 or Home	6C	F06C	47	C7	4700	4737	7700	Note[6]	4700	4737	7700	Note[6]
56	8	75	F075	48	C8	4800	4838	----	Note[6]	4800	4838	8D00	Note[6]
57	9 or Page Up	7D	F07D	49	C9	4900	4939	8400	Note[6]	4900	4939	8400	Note[6]

KEYBOARD SCAN CODES

Key #	Key Descript.	AT Mode Make Code	AT Mode Break Code	XT Mode Make Code	XT Mode Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
58	+	79	F079	4E	CE	4E2B[7]	4E2B[7]	----	----	4E2B[7]	4E2B[7]	9000	4E00[7]
59	Caps Lock	58	F058	3A	BA	Note[7]	Note[7]	----	Note[7]	Note[7]	Note[7]	----	Note[7]
60	A or a	1C	F01C	1E	9E	1E61	1E41	1E01	1E00	1E61	1E41	1E01	1E00
61	S or s	1B	F01B	1F	9F	1F73	1F53	1F13	1F00	1F73	1F53	1F13	1F00
62	D or d	23	F023	20	A0	2064	2044	2004	2000	2064	2044	2004	2000
63	F or f	2B	F02B	21	A1	2166	2146	2106	2100	2166	2146	2106	2100
64	G or g	34	F034	22	A2	2267	2247	2207	2200	2267	2247	2207	2200
65	H or h	33	F033	23	A3	2368	2348	2308	2300	2368	2348	2308	2300
66	J or j	3B	F03B	24	A4	246A	244A	240A	2400	246A	244A	240A	2400
67	K or k	42	F042	25	A5	256B	254B	250B	2500	256B	254B	250B	2500
68	L or l	4B	F04B	26	A6	266C	264C	260C	2600	266C	264C	260C	2600
69	: or ;	4C	F04C	27	A7	273B	273A	----	----	273B	273A	----	2700
70	" or '	52	F052	28	A8	2827	2822	----	----	2827	2822	----	2800
71	Enter	5A	F05A	1C	9C	1C0D	1C0D	1C0A	----	1C0D	1C0D	1C0A	1C00
72	4	6B	F06B	4B	CB	4B00	4B34	7300	Note[6]	4B00	4B34	7300	Note[6]
73	5	73	F073	4C	CC	-----	4C35	---	Note[6]	4C00	4C35	8F00	Note[6]
74	6	74	F074	4D	CD	4D00	4D36	7400	Note[6]	4D00	4D36	7400	Note[6]

KEYBOARD SCAN CODES

Key #	Key Descript.	AT Mode Make Code	AT Mode Break Code	XT Mode Make Code	XT Mode Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
76	Left Shift	12	F012	2A	AA	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]
77	Z or z	1A	F01A	2C	AC	2C7A	2C5A	2C1A	2C00	2C7A	2C5A	2C1A	2C00
78	X or x	22	F022	2D	AD	2D78	2D58	2D18	2000	2D78	2D58	2D18	2000
79	C or c	21	F021	2E	AE	2E63	2E43	2E03	2E00	2E63	2E43	2E03	2E00
80	V or v	2A	F02A	2F	AF	2F76	2F56	2F16	2F00	2F76	2F56	2F16	2F00
81	B or b	32	F032	30	B0	3062	3042	3002	3000	3062	3042	3002	3000
82	N or n	31	F031	31	B1	316E	314E	310E	3100	316E	314E	310E	3100
83	M or m	3A	F03A	32	B2	326D	324D	320D	3200	326D	324D	320D	3200
84	< or ,	41	F041	33	B3	332C	333C	-----	-----	332C	333C	-----	3300
85	> or .	49	F049	34	B4	342E	343E	-----	-----	342E	343E	-----	3400
86	? or /	4A	F04A	35	B5	352F	353F	-----	-----	352F	353F	-----	3500
87	Right Shift	59	F059	36	B6	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]
88	Up Arrow	E075	E0F075	E02AE048	E0C8E0AA	4800	4800	-----	----	48E0	48E0	8DE0	9800
89	1 or End	69	F069	4F	CF	4F00	4F31	7500	Note[6]	4F00	4F31	7500	Note[6]
90	2	72	F072	50	D0	5000	5032	----	Note[6]	5000	5032	9100	Note[6]
91	3 or Pg Dn	7A	F07A	51	D1	5100	5133	7600	Note[6]	5100	5133	7600	Note[6]
92	Left Ctrl	14	F014	1D	9D	Note[9]	Note[9]	Note[9]	Note[9]	Note[9]	Note[9]	Note[9]	Note[9]
93	Left Alt	11	F011	38	B8	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]
94	Space	29	F029	39	B9	3920	3920	3920	3920	3920	3920	3920	3920

KEYBOARD SCAN CODES

Key #	Key Descript.	AT Mode Make Code	AT Mode Break Code	XT Mode Make Code	XT Mode Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
95	Right Alt	E011	E0F011	E038	E0B8	Note$_9^{10}$	Note$_9^{10}$	Note$_9^{10}$	Note$_9^{10}$	Note$_9^{10}$	Note$_9^{10}$	Note$_9^{10}$	Note$_9^{10}$
96	Right Ctrl	E014	E0F014	E0ID	E09D	Note^9	Note^9	Note^9	Note^9	Note^9	Note^9	Note^9	Note^9
97	Left Arrow	E06B	E0F06B	E02AE04B	E0CBE0AA	4B00	4B00	7300	-----	4BE0	4BE0	73E0	9B00
98	Down Arrow	E072	E0F072	E02AE050	E0D0E0AA	5000	5000	-----	-----	50E0	50E0	91E0	A000
99	Right Arrow	E074	E0F074	E024E04D	E0CDE0AA	4D00	4000	7400	----^{6}	4DE0	4DE0	74E0	9D00^6
100	0 or Ins	70	F070	52	D2	5200	5230	----	Note^6	5200	523H	9200	Note^6
101	. or Del	71	F071	53	D3	5300	532E	----	----	5300	532E	9300	-----
102	Enter	E05A	E0F05A	E01C	E09C	1C0D	1C0D	1C0A	----	E00D	E00D	E00A	A600

NOTES

Note1 —INT O5H is invoked and a screen dump is performed
Note2 —the scroll lock active bit is toggled
Note3 —the pause state is initiated
Note4 —INT 1BH is invoked
Note5 —the numlock active bit is toggled
Note6 —ALT num pad generates raw ascii code of typed number
Note7 —the caps lock active bit is toggled
Note8 —hold shift lock active until key is released
Note9 —hold control shift active until key is released
Note10—hold alternate shift active until key is released

5.0 PROTOCOL

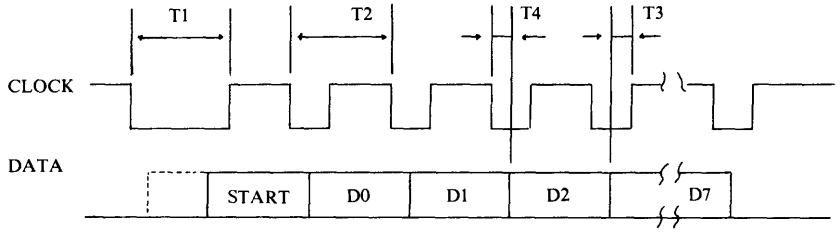
5.0.1 COMMUNICATION MODE 1 (PC/XT Mode)

The keyboard communicates with the host computer using a synchronous serial protocol at approximately 9600BPS. One start bit, eight data bits, no stop bit, and no parity are used to make up the nine bit data word. When no communications are in progress, the keyboard holds the data line low and the clock line high.

Before starting a transmission, the keyboard lowers the clock line as a Request To Send (RTS). The state of the data line is then checked. If the host system is holding the data line low, transmissions are disabled. The keyboard will retain the keycode for the pressed key in its buffer until the clock and data lines return to the idle state. The keyboard then resumes scanning the keyboard matrix until transmissions are enabled.

When transmissions are enabled, 100 to 250 microseconds after the keyboard drives the clock line low, the keyboard transmits its data in the previously described format. Data is valid during the time the clock line is high and for a minimum of 10 microseconds after the falling edge of the clock line. See Figure 2 for a timing diagram.

< KEYBOARD DATA OUTPUT-XT MODE >



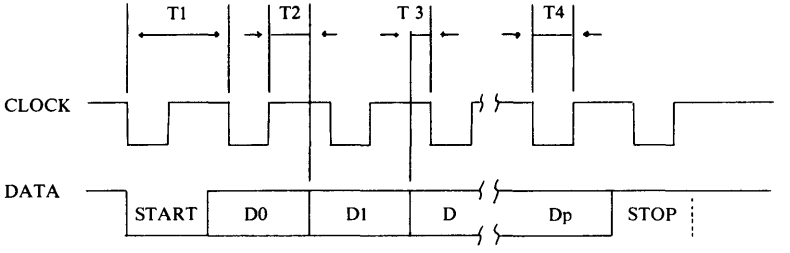
T1 ; 100 ~ 250μs (CHECKING TIME OF DATA OUTPUT READY OR PROHIBITION)
T2 ; 104μs ± 20%
T3 ; 10μs MIN.
T4 ; 10μs MIN.

FIGURE 2

5.0.2 COMMUNICATION MODE 2 (AT MODE)

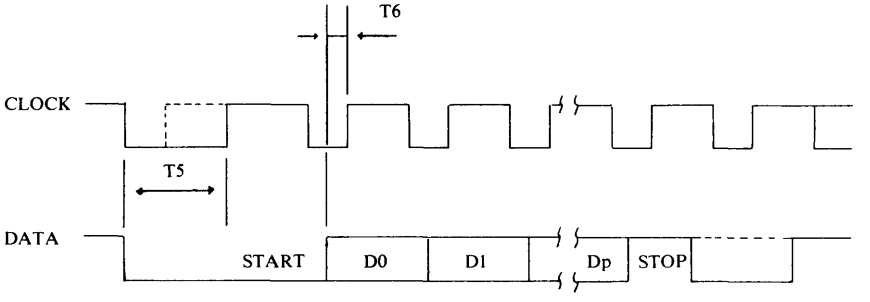
The keyboard communicates with the host computer using a synchronous serial protocol at approximately 9600BPS. One start bit, eight data bits, odd parity, and one stop bit form the eleven bit data word. This communication is bi-directional, with the keyboard clocking all data transfers. When no communications are in progress, the data and clock lines are high, indicating an idle state.

< KEYBOARD DATA OUTPUT-AT MODE > Figure 3A



T1 ; 104μs ±20%
T2 ; 20μs MIN.
T3 ; 20μs MIN.
T4 ; 35μs ±20%

< KEYBOARD DATA INPUT-AT MODE > Figure 3B



T5 ; 60μs MIN. (WAITING TIME FOR HOST DATA OUTPUT)
T6 ; 5μs MIN.

FIGURE 3

Before starting a transmission, the keyboard checks the status of the clock and data lines. Transmissions are disabled if the clock line is low and the code for the pressed key is held in the keyboard buffer until transmissions are enabled. If the clock line is high and the data line is low, the host system is sending a Request To Send (RTS), and the code for the pressed key is stored in the buffer.

When transmissions are enabled and no RTS is detected from the host system, both clock and data line will be high. The keyboard starts a transmission by sending a low start bit, followed by the rest of the data word. Data is valid 20 microseconds minimum prior to the falling edge of the clock. See Figure 3 for timing diagram.

During the transmission of a data word, the keyboard periodically checks the state of the clock line. If the clock line is low during these checks prior to the rising edge of the parity bit, a data collision occurs. When a data collision occurs, the keyboard stops transmitting, returns the code for the pressed key to the keyboard buffer, and prepares to respond to actions requested by the host system.

5.1 COMMANDS FROM THE KEYBOARD TO THE HOST SYSTEM

Keyboard Buffer Overrun — AT and XT Modes

This buffer can store up to sixteen codes for pressed keys. When this buffer is full and the seventeenth code is received, this code is replaced by an Overrun Code. The following chart shows the Overrun Codes for each mode.

XT Mode FF Hex
AT Mode 00 Hex

Codes received after this code are lost until the keyboard clears additional space in the keyboard buffer.

Self Test Passed — AA Hex AT and XT Modes

The keyboard issues this command upon successful completion of the keyboard self test. The self test consists of the following.

XT MODE

1. Memory is cleared.
2. Keyboard buffer is cleared.
3. ROM checksum is read and compared.
4. RAM is tested.
5. Self test completion code is output.
6. AA Hex is output to indicate successful self test.
7. FC Hex is output to indicate a defect in the self test.

AT MODE

1. ROM checksum is read and compared.
2. RAM is tested.
3. AA Hex is output to indicate successful self test.
4. FC Hex is output to indicate a defect in the self test.

This self test is initiated by the host system reset (Ctrl, Alt, Delete) or by Power-on Reset. Upon successful completion of the Self Test during Power-on Reset, the keyboard is set to XT mode if the keyboard detects a low level on the data line for more than 10 microseconds after 5 microseconds from the falling edge of the clock line. If this condition is not met, the keyboard is placed in the AT Mode, and Typematic Rate and Delay are set to the following defaults:

Typematic Rate 10.9 cps
Delay 500 milliseconds

ECHO — EE Hex AT and XT Modes

The Echo Command (EE Hex) is sent in response to an Echo Command from the host system instead of the normal Acknowledge (ACK) for diagnostic purposes.

Acknowledge — FA Hex AT Mode

The keyboard sends an Acknowledge (FA Hex) in response to a valid command from the host system, with the exceptions of the Resend and Echo commands.

Resend — FE Hex AT and XT Modes

The keyboard issues a Resend (FE Hex) in response to inputs which have parity errors, framing errors, or invalid data received from the host system.

KEYBOARD BUFFER OVERRUN — AT and XT Modes

When the 16-character keyboard buffer receives the 17th character, an overflow condition occurs. This condition is communicated to the host system by transmitting the Keyboard buffer Overrun (FF Hex for XT Mode, 00 Hex for AT Mode) to the host system.

5.2 COMMANDS FROM THE HOST SYSTEM TO THE KEYBOARD

Prior to sending commands to the keyboard, the host system must first check to see if the keyboard is sending data. If the keyboard is transmitting, and the data is past the parity bit, the host system must accept the data prior to initiating its own transmission.

If the keyboard's data has not yet reached the tenth clock pulse (Parity Bit), or is not transmitting data, the host system assumes control by lowering the clock line for a minimum of 60 microseconds, then releasing the clock line after clamping the data line low to indicate a start bit. The keyboard will respond with an RTS within 5 microseconds by clocking the start bit into the keyboard. The keyboard continues to clock data as shown in the timing diagram (Figure 3B). The host system must ensure that the data is valid prior to the rising edge and after the falling edge of the keyboard clock pulse.

After the parity bit, the host system should raise the data line to indicate a stop bit. The keyboard checks for a logical high stop bit, then clamps the data line low prior to clock in the stop bit. This signals the host system that the keyboard received the data correctly (Acknowledge). If the host system has not raised the data line to indicate a stop bit, a framing error results and the keyboard continues to clock data until the data line is raised by the host system. Upon receiving either a framing or parity error, the keyboard issues a RESEND to the host system.

All commands from the host system require a response from the keyboard. The keyboard will respond to these commands within 20 microseconds.

The following commands may be sent to the keyboard at any time, following the protocol described for the AT Mode. These commands are valid only in the AT Mode. During the reset command, the keyboard will not respond within 20 microseconds as described above.

RESET — FF Hex

Upon receiving this command, the keyboard transmits an Acknowledge to the host system. The keyboard then waits for the host system to accept the Acknowledge response. The host system will accept the Acknowledge by raising the clock and data lines for a minimum of 500 microseconds.

The keyboard then executes the self test routine similar to the Power-On Reset, and is placed in its default state.

RESEND — FE Hex

Upon receiving this command, the keyboard will transmit the last byte of data sent to the host system.

SET DEFAULT — F6 Hex

This command resets the keyboard to the Power-Up default state. The keyboard responds with an Acknowledge, clears the output buffer, sets the scanset to AT Mode, sets the default typematic rate and delay, and continues to scan the matrix.

DEFAULT DISABLE — F5 Hex

This command is similar to the Set Default command, except the keyboard stops scanning the matrix and waits for further instructions to be sent by the host system.

ENABLE — F4 Hex

Upon receipt of this command the keyboard responds with an Acknowledge, clears the output buffer, and starts scanning the matrix.

SET TYPEMATIC RATE/DELAY — F3 Hex

This command consists of one command byte and one parameter byte. The keyboard Acknowledges the command byte, stops scanning the matrix, and waits for the parameter byte. Upon receiving the parameter byte, the keyboard sends an Acknowledge, sets the typematic rate and delay as indicated in Table 2, and continues scanning the matrix.

If another command is received instead of the parameter byte, the set typematic rate/delay function ends with no change to the existing rate or delay parameters. The new command is processed and the keyboard continues scanning the matrix.

The parameter byte consists of an eight-bit word with bit 7 (most significant bit) always being set. Bits 0-4 set the typematic rate and bits 5-6 set the delay.

Example

1	0	1	0	1	0	1	1	Parameter Byte
7	6	5	4	3	2	1	0	Bit Number

The above example shows the default 10.9 cps typematic rate and 500 microsecond delay. Bits 0-4 (010111) correspond to the rate of 10.9 cps shown on Table 2 ii and bits 5-6 (01) correspond to the 500 microsecond delay shown in Table 2 i.

See Table 2 for Typematic Rate/Delay values other than the default settings.

i) Delay

Bit 6 5	Delay ms
0 0	250
0 1	500
1 0	750
1 0	1000

ii) Rate

Bit 4	3	2	1	0	Rate (CPS)
0	0	0	0	0	30.0
0	0	0	0	1	26.7
0	0	0	1	0	24.0
0	0	0	1	1	21.8
0	0	1	0	0	20.0
0	0	1	0	1	18.5
0	0	1	1	0	17.1
0	0	1	1	1	16.0
0	1	0	0	0	15.0
0	1	0	0	1	13.3
0	1	0	1	0	12.0
0	1	0	1	1	10.9
0	1	1	0	0	10.0
0	1	1	0	1	9.2
0	1	1	1	0	8.6
0	1	1	1	1	8.0

Bit 4	3	2	1	0	Rate (CPS)
1	0	0	0	0	7.5
1	0	0	0	1	6.7
1	0	0	1	0	6.0
1	0	0	1	1	5.5
1	0	1	0	0	5.0
1	0	1	0	1	4.6
1	0	1	1	0	4.3
1	0	1	1	1	4.0
1	1	0	0	0	3.7
1	1	0	0	1	3.3
1	1	0	1	0	3.0
1	1	0	1	1	2.7
1	1	1	0	0	2.5
1	1	1	0	1	2.3
1	1	1	1	0	2.1
1	1	1	1	1	2.0

TABLE 2

ECHO — FE Hex

This command is provided for diagnostic purposes. The keyboard shall respond with EE Hex, instead of Acknowledge, and continue scanning the matrix.

SET/RESET STATUS INDICATORS — ED Hex

This command consists of one command byte and one parameter byte. The keyboard Acknowledges the command byte, stops scanning the matrix, and waits for the parameter byte. Upon receiving the parameter byte, the keyboard sends an Acknowledge, sets the status indicators, and starts scanning the matrix.

If another command is received instead of the parameter byte, the keyboard disregards the Set/Reset Status Indicators command without changing the present status of the indicators, processes the new command, and starts scanning the matrix.

The parameter byte is an eight-bit word with bits 3-7 always set to low. Bit 0 is the Scroll Lock Indicator, bit 1 is the Num Lock Indicator, and bit 2 is the Caps Lock Indicator. A high in each individual bit indicates that Indicator is active and the indicator lamp should be on.

Example

0	0	0	0	0	0	1	0	PARAMETER BYTE
7	6	5	4	3	2	1	0	BIT NUMBER

The above example shows the power-on default of the Tandy 3000 NL. Bit 1 is high indicating Num Lock is active and the Num Lock indicator lamp is on.

READ KEYBOARD ID — F2 Hex

This command causes the keyboard to return two identification bytes AB83 Hex. The keyboard responds with an Acknowledge to the command and stops scanning the matrix. The keyboard then transmits the keyboard ID AB83 Hex and resumes scanning the matrix.

SET/READ SCAN SET — F0 Hex

This command is used to select one of three Scan Sets or to tell the host system which Scan Set is currently being used. This command consists of a command byte and a parameter byte. Upon receiving this command, the keyboard sends an Acknowledge to the host system and waits for the parameter byte. When the keyboard receives the parameter byte, it responds with an Acknowledge.

A parameter byte of 00 Hex will cause the keyboard to transmit the Hex value for the Scan Set currently in use. A parameter byte of 01 Hex selects the Scan Set 1 (XT Scan Codes), 02 Hex selects Scan Set 2 (Default AT Scan Codes), and 03 Hex selects Scan Set 3 (Special AT Scan Codes -- See Table 3 for Scan Codes and Default Key State Information). The keyboard resumes scanning the matrix.

TABLE 3

KEY DESCRIPTION	MAKE CODE	BREAK CODE	DEFAULT KEY STATE
Esc	08	F0 08	Make Only
F1	07	F0 07	Make Only
F2	0F	F0 0F	Make Only
F3	17	F0 17	Make Only
F4	1F	F0 1F	Make Only
F5	27	F0 27	Make Only
F6	2F	F0 2F	Make Only
F7	37	F0 37	Make Only
F8	3F	F0 3F	Make Only
F9	47	F0 47	Make Only
F10	4F	F0 4F	Make Only
F11	56	F0 56	Make Only
F12	5E	F0 5E	Make Only
Print Scrn	57	F0 57	Make Only
Scroll Lock	5F	F0 5F	Make Only
Pause or Break	62	F0 62	Make Only
`	0E	F0 0E	Typematic
1	16	F0 16	Typematic
2	1E	F0 1E	Typematic
3	26	F0 26	Typematic
4	25	F0 25	Typematic
5	2E	F0 2E	Typematic
6	36	F0 36	Typematic
7	3D	F0 3D	Typematic
8	3E	F0 3E	Typematic
9	46	F0 46	Typematic
0	45	F0 45	Typematic
-	4E	F0 4E	Typematic
=	55	F0 55	Typematic
Backspace	66	F0 66	Make Only
Insert cursor pad	67	F0 67	Make Only
Home cursor pad	6E	F0 6E	Make Only
Page Up cursor pad	6F	F0 6F	Make Only
Num Lock	76	F0 76	Make Only
/ number pad	77	F0 77	Make Only
* number pad	7E	F0 7E	Make Only
- number pad	84	F0 84	Make Only
Tab	0D	F0 0D	Typematic
q	15	F0 15	Typematic
w	1D	F0 1D	Typematic
e	24	F0 24	Typematic
r	2D	F0 2D	Typematic
t	2C	F0 2C	Typematic
y	35	F0 35	Typematic
u	3C	F0 3C	Typematic
i	43	F0 43	Typematic
o	44	F0 44	Typematic
p	4D	F0 4D	Typematic
[	54	F0 54	Typematic
]	5B	F0 5B	Typematic

\	5C	F0 5C	Typematic
Delete cursor pad	64	F0 64	Typematic
Home cursor pad	65	F0 65	Make Only
Page Up cursor pad	6D	F0 6D	Make Only
7 number pad	6C	F0 6C	Make Only
8 number pad	75	F0 75	Make Only
9 number pad	7D	F0 7D	Make Only
+ number pad	7C	F0 7C	Make Only
Caps Lock	14	F0 14	Make/Break
a	1C	F0 1C	Typematic
s	1B	F0 1B	Typematic
d	23	F0 23	Typematic
f	2B	F0 2B	Typematic
g	34	F0 34	Typematic
h	33	F0 33	Typematic
j	3B	F0 3B	Typematic
k	42	F0 42	Typematic
l	4B	F0 4B	Typematic
;	4C	F0 4C	Typematic
'	52	F0 52	Typematic
Enter	5A	F0 5A	Typematic
4 number pad	6B	F0 6B	Make Only
5 number pad	73	F0 73	Make Only
6 number pad	74	F0 74	Make Only
Left Shift	12	F0 12	Make/Break
z	1A	F0 1A	Typematic
x	22	F0 22	Typematic
c	21	F0 21	Typematic
v	2A	F0 2A	Typematic
b	32	F0 32	Typematic
n	31	F0 31	Typematic
m	3A	F0 3A	Typematic
,	41	F0 41	Typematic
.	49	F0 49	Typematic
Right Shift	59	F0 59	Make/Break
Up Arrow cursor pad	63	F0 63	Typematic
1 number pad	69	F0 69	Make Only
2 number pad	72	F0 72	Make Only
3 number pad	7A	F0 7A	Make Only
Enter number pad	79	F0 79	Make Only
Left Ctrl	11	F0 11	Make/Break
Left Alt	19	F0 19	Make/Break
Spacebar	29	F0 29	Typematic
Right Alt	39	F0 39	Make Only
Right Ctrl	58	F0 58	Make Only
Left Arrow cursor	61	F0 61	Typematic
Down Arrow	60	F0 60	Typematic
Right Arrow	6A	F0 6A	Typematic
Ins number pad	70	F0 70	Make Only
Del number pad	71	F0 71	Make Only

SET ALL KEYS — TYPEMATIC — F7 Hex

SET ALL KEYS — MAKE/BREAK — F8 Hex

SET ALL KEYS — MAKE ONLY — F9 Hex

SET ALL KEYS — TYPEMATIC/MAKE/BREAK — FA Hex

These commands affect Scan Set 3 only, but may be sent using any Scan Set. The keyboard responds with an Acknowledge, clears the output buffer, sets all keys to the function requested by the command, and continues scanning the matrix if it was previously enabled.

SET SINGLE KEY — TYPEMATIC — FB Hex

SET SINGLE KEY — MAKE/BREAK — FC Hex

SET SINGLE KEY — MAKE ONLY — FD Hex

These commands consist of a command byte and a parameter byte. The keyboard responds to the command byte with an Acknowledge and waits for the parameter byte. The parameter byte is the scan code from Scan Set 3 for the key to be changed. Upon receiving the parameter byte, the keyboard sets the selected key to the function selected by the command byte, and continues to scan the matrix if it was previously enabled. These commands affect only Scan Set 3 operation, but may be sent using any Scan Set.

5.3 KEY ROLLOVER

The keyboard incorporates N-Key Rollover in software to avoid loss of keystroke data during high speed entry. N-Key Rollover is defined as all keys pressed and released will be output in the proper sequence. However, when the keyboard detects more than four keys pressed during a scan of the matrix, the keyboard does not output the keycodes until one or more of the keys are released. If the released key was not properly detected as a pressed key, an error condition occurs and the keyboard issues an buffer overrun code to the host system.

5.4 AUTOREPEAT

The power-on default condition will cause the last key pressed to repeat at 10.9 characters-per-second after a 500 millisecond delay. This may be changed by the system when the keyboard is using the AT Communications Mode.

5.5 BUFFERING

The keyboard is capable of storing 16 scan codes in a first in/ first out (FIFO) circular buffer. When the buffer overflows, the last code is replaced by a Hex 00, in AT Mode and a Hex FF, in XT Mode.

5.6 STATUS INDICATORS

Three LED Status Indicators are provided: Num Lock, Caps Lock, and Scroll Lock.

These indicators are located in the keytop of each respective key. The keyboard will power up with all indicators OFF, except when the host system (such as the Tandy 3000 NL) sets them to ON.

6.0 ELECTRICAL REQUIREMENTS

The interface consists of two bi-directional lines, clock and data, which are controlled by 74LS125 equivalent buffers. The keyboard side is terminated by 2200 Ohm resistors. All voltage levels are TTL compatible and the keyboard drivers are capable of sinking 20 mA minimum including the current sourced by the pullup resistors on the keyboard.

6.1 CONNECTOR

The connector is a 5-pin DIN connector. Connections are shown in the following table.

Table 4

PIN #	SIGNAL
1	CLOCK
2	DATA
3	NO CONNECTION
4	LOGIC GROUND
5	+5 VOLTS DC

6.2 CHASSIS GROUND

Chassis ground is isolated from logic ground.

6.3 POWER REQUIREMENTS

The keyboard requires 5 Volts DC, +/-5%, at 500 milliamps (max).

7.0 ENVIRONMENTAL REQUIREMENTS

7.1 TEMPERATURE

OPERATING.....0 to 50 degrees C
NON-OPERATING.....-20 to 60 degrees C

7.2 RELATIVE HUMIDITY

20% to 90% non-condensing

7.3 SHOCK

Operating and non-operating.....10G 11 mS duration

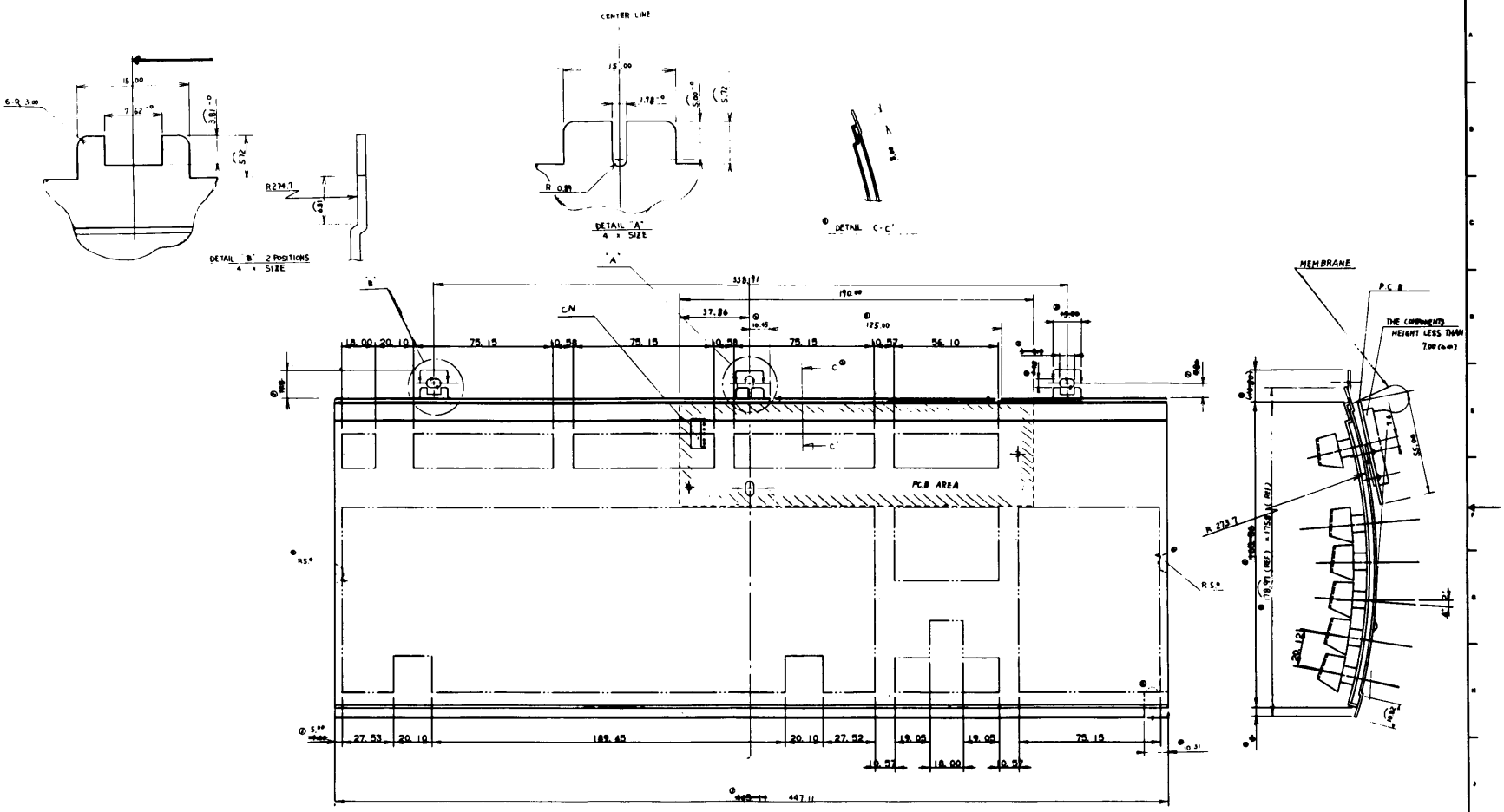
7.4 VIBRATION

Operating and non-operating.....0.3 mm amplitude 10 to 55 Hz

8.0 RELIABILITY

8.1 SWITCH LIFE

Switch life of the keyboard is a minimum of 20 million cycles.



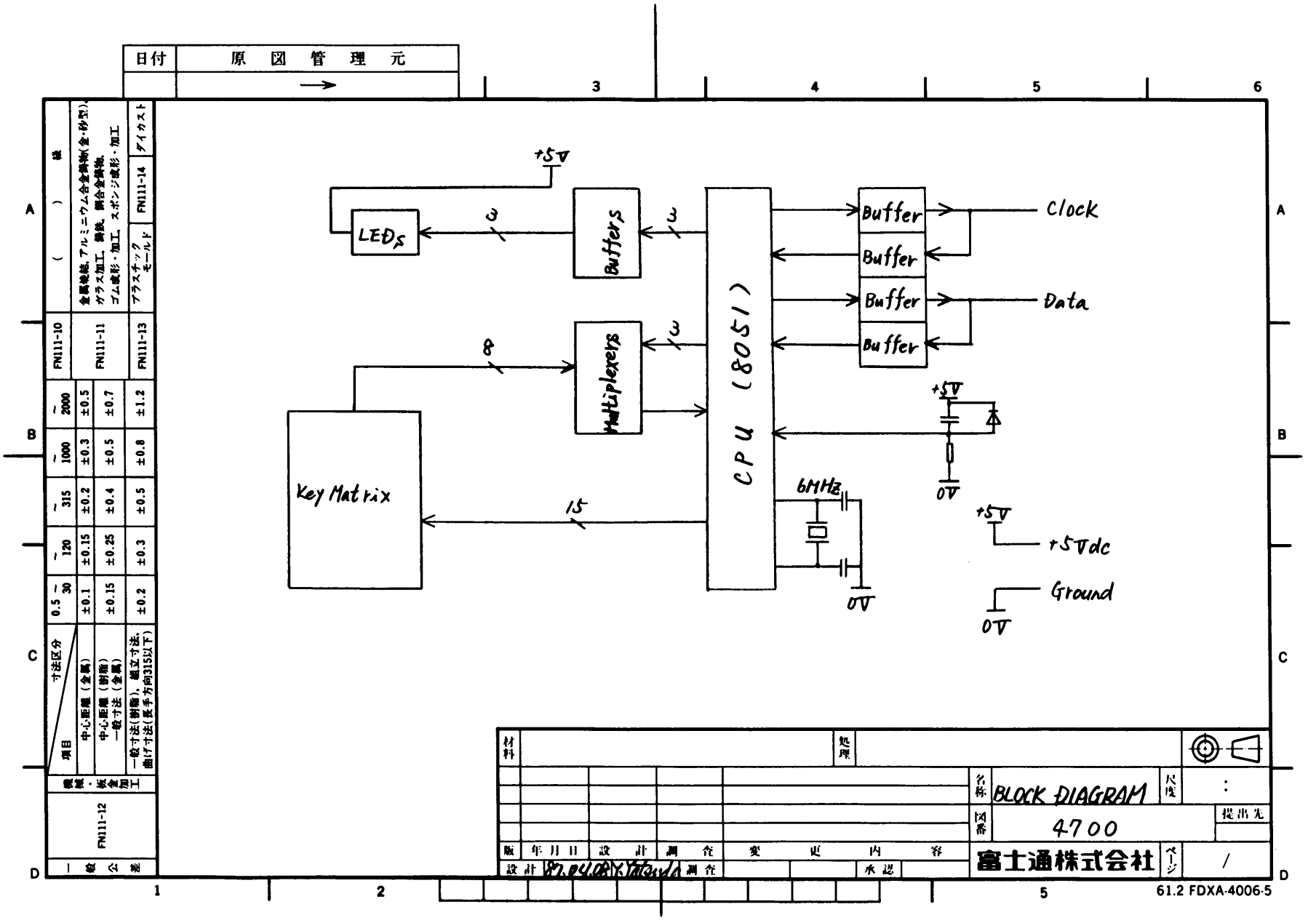
NOTE

1. TOLERANCE IS ± 0.5 mm UNLESS OTHERWISE SPECIFIED.
2. MEASUREMENTS WITH "⌒" MARK SHOW THE ARC.

KEYBOARD UNIT ASSY.

<PROPOSAL>

KEYBOARD UNIT ASSY	
N860-4703-U001	6
FUJITSU LIMITED	


日付
原 図 管 理 元
+5V
LEDs
8
Buffers
3
CPU (8051)
Buffer
Buffer
Buffer
Buffer
Clock
Data
8
Multiplexers
3
Key Matrix
15
6MHz
0V
+5V
0V
+5V
+5Vdc
Ground
0V
名称 BLOCK DIAGRAM
図番 4700
富士通株式会社
61.2 FDXA-4006-5

		Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
		1	2	3	4	5	6	7	8
X14	9	A00					A12		
X2	10			B00	B11				
X13	11	A01	C12'	B00'					
X6	12	B01	B02	B03	B04	B05	B06	B07	B08
X8	14	F00	F02	F03	F04	F05	F06	F07	F08
X10	15	E00	E01	E02	E03	E04	E05	E06	E07
X12	16	D00	D01	D02	D03	D04	D05	D06	D07
X5	17	C01	C02	C03	C04	C05	C06	C07	C08
X9	20	D10	F09	F10	F11	F12	F13	F15	F16
X11	21	E08	E09	E10	E11	E12	E13	D08	D09
X1	23	E15	E16	F14	C00	A09	E17	B20	E18
X3	24	D11	D12	D13	D17	D18	D19	E19	E20
X4	25	C09	C10	C11	C12	C17	C18	C19	D20
X7	26	B09	B10	A05	A17	A19	B17	B18	B19
X0	27	A14	A15	A16	B15	D14	D15	D16	E14

Vcc 18

L1 13 Caps

L3 19 Scroll

L2 22 Num

原図管理元

日付

版	年月日	設計	調査	変更内容
設計		調査		承認

名称 CIRCUIT SPECIFICATION

図番 N86C-4700-0001

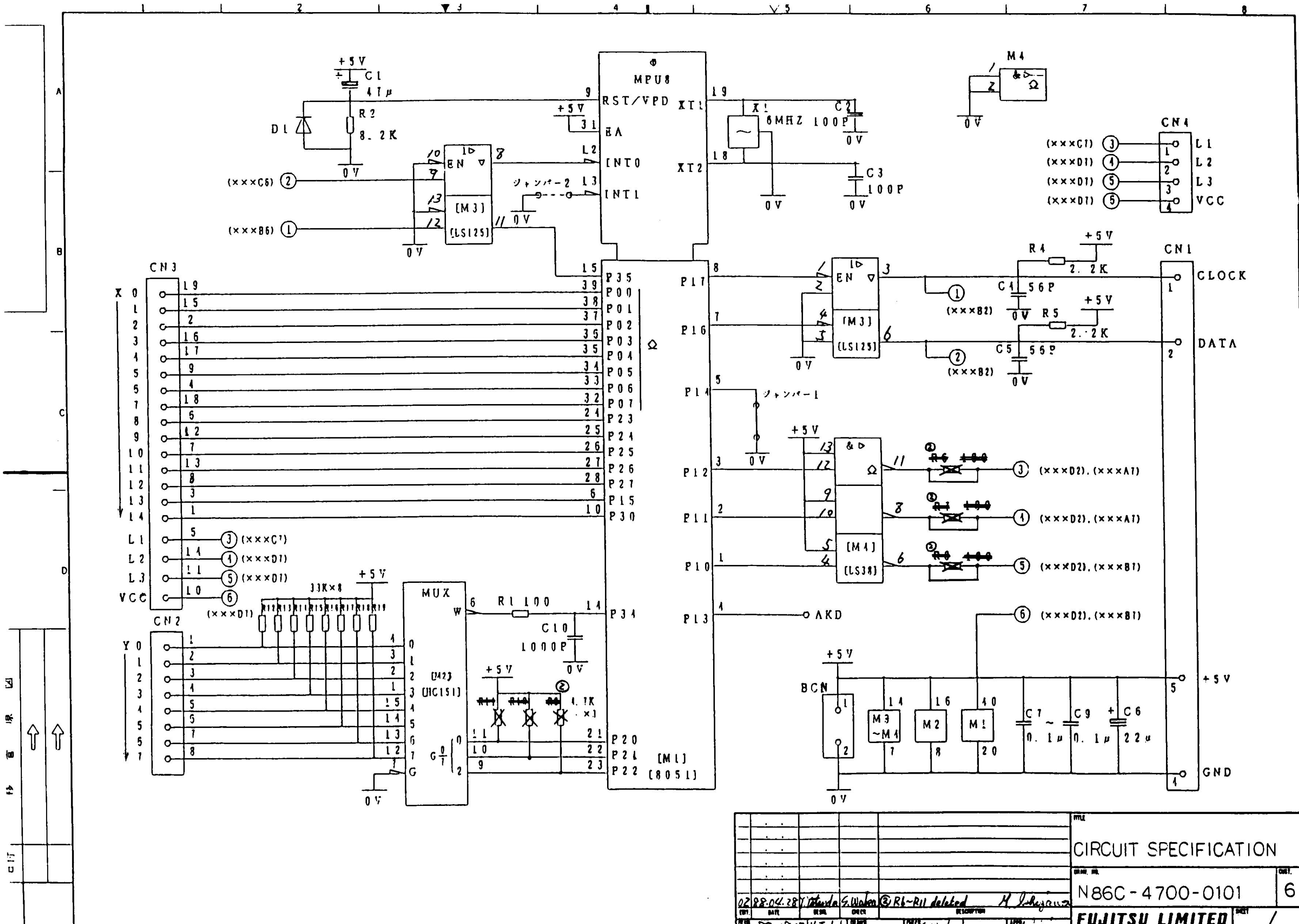
提出先 6

富士通株式会社

ページ /

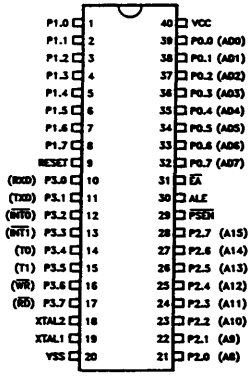
3

61.3. FDXA-4003-5



MPU8
RST/VPD
EA
INT0
INT1
XT1
XT2
X1 6MHZ
C1 47μ
R2 8.2K
D1
C2 100P
C3 100P
+5V
0V
M4
CN4
L1
L2
L3
VCC
CN1
CLOCK
DATA
R4 2.2K
R5 2.2K
C4 56P
C5 56P
[M3] [LS125]
[M4] [LS38]
CN3
CN2
MUX
[M2] [IC151]
R1 100
C10 1000P
33K×8
4.7K ×3
AKD
BCN
M3 ~M4
M2
M1
C7 0.1μ
C9 0.1μ
C6 22μ
GND
[M1] [8051]
ジャンパー1
ジャンパー2
CIRCUIT SPECIFICATION
N86C-4700-0101
6
FUJITSU LIMITED
R6~R11 deleted

Pin Connections



DOCUMENT CONTROL SECTION

DATE

TITLE CUSTOM IC PIN SIGNAL AND FUNCTION

FUJITSU LIMITED

1 / 3

61.3. FDXA-4902-5

PIN DESCRIPTION

V_{SS}
Circuit ground potential.

V_{CC}
+5V power supply during operation, programming and verification.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port.

It is also the multiplexed low-order address and data bus when using external memory. It is used for data input and output during programming and verification. Port 0 can sink/source two TTL loads.

Port 1
Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during programming and verification. Port 1 can sink/source one TTL load.

Port 2
Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order 8 bits of address when accessing external memory. It is used for the high-order address and the control signals during programming and verification. Port 2 can sink/source one TTL load.

Port 3
Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a special function must be programmed to a one (1) for that function to operate. Port 3 can sink/source one TTL load. The special functions are assigned to the pins of Port 3, as follows:

- RXD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous).
- TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous).
- $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0.
- $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1.
- T0 (P3.4). Input to counter 0.
- T1 (P3.5). Input to counter 1.
- $\overline{WR}$ (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory.
- $\overline{RD}$ (P3.7). The read control signal enables External Data Memory to Port 0.

RST/V_{PD}
A low to high transition on this pin (at approximately 3V) resets the 8051. If V_{PD} is held within its spec (approximately +5V), while V_{CC} drops below spec, V_{PD} will provide standby power to the RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}. A small internal resistor permits power-on reset using only a capacitor connected to V_{CC}.

ALE/$\overline{PROG}$
Provides Address Latch Enable output used for latching the address into external memory during normal operation. Receives the program pulse input during EPROM programming.

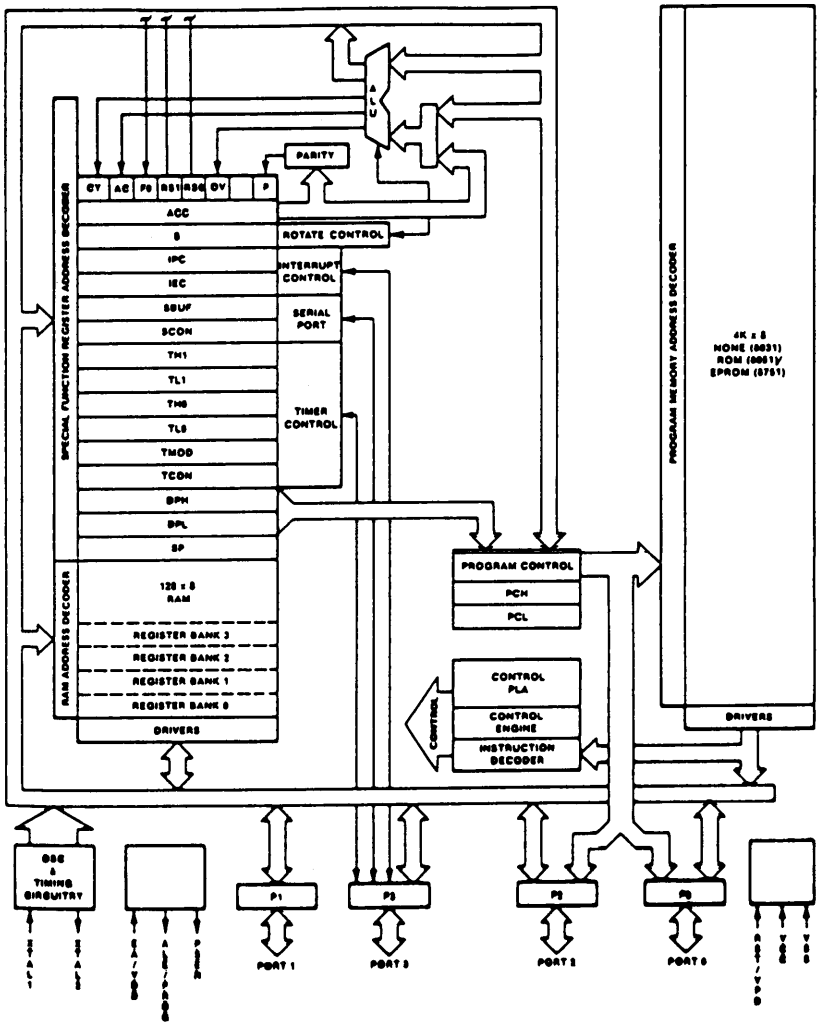
$\overline{PSEN}$
The Program Store Enable output is a control signal that enables the external Program Memory to the bus during normal fetch operations.

$\overline{EA}$/V_{DD}
When held at a TTL high level, the 8051 executes instructions from the internal ROM/EPROM when the PC is less than 4096. When held at a TTL low level, the 8051 fetches all instuctions from external Program Memory. The pin also receives the 21V EPROM programming supply voltage.

XTAL1
Input to the oscillator's high gain amplifier. A crystal or external source can be used.

XTAL2
Output from the oscillator's amplifier. Required when a crystal is used.

Block Diagram



DOCUMENT CONTROL SECTION

DATE

EDIT.	DATE	DESIG.	CHECK	DESCRIPTION
DESIG.			CHECK	APPR.

TITLE CUSTOM IC PIN SIGNAL AND FUNCTION

DRAW. NO.

CUST.

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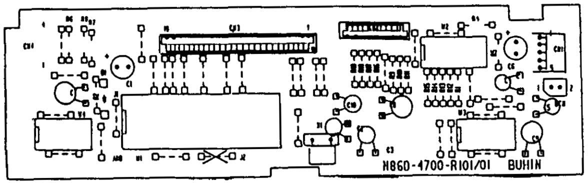
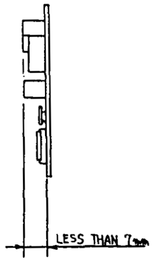
3 / 3

61.3. FDXA-4902-5

DATE	DOCUMENT CONTROL SECTION
	→





NOTE

1. CAPACITORS AND RESONATOR (X1) TO BE BENT AS ABOVE DRAWING AFTER MOUNTED.
   CAPACITOR (C6) TO BE NOT BENT.
2. CONNECTORS (CN1.CN2.CN3) TO BE NOT FLOATED.
3. JUMPER WIRE J2 TO BE NOT MOUNTED.
4. JUMPER WIRE IS 30 POSITIONS (CONTAIN J1)
5. COMPONENTS HEIGHT IS LESS THAN 7mm.

TITLE PCB ASSEMBLE

DRAW. NO. N860-4703-P101 /01

6

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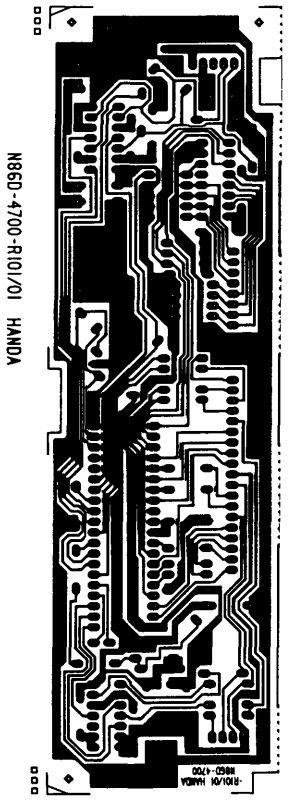
61.3. FDXA-4902-5



DOCUMENT CONTROL SECTION

DATE

					TITLE	P.C.B ARTWORK
					DRAW. NO.	N86D-4700-Q101/01
						CHT. 6
DSN.	DATE	RESP.	CHECK	DESCRIPTION		
RESP.	Jan. 18 '88	H. Ohashi	CHECK	S. Wada	APPR.	H. Kobayashi

FUJITSU LIMITED

61.3. FDXA-4902-5

Disk Drive

TEAC FD-55BR/FR/GR

MINI FLEXIBLE DISK DRIVE

MAINTENANCE MANUAL

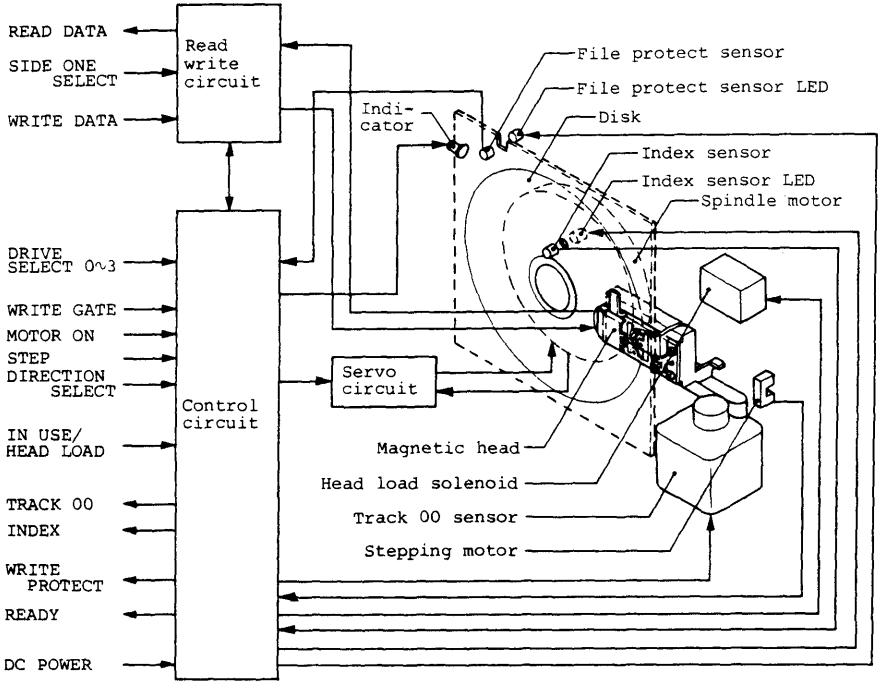
TABLE OF CONTENTS

SECTION 2

THEORY OF OPERATION

2-1. CONSTRUCTION AND FUNCTION

2-1-1. General Block Diagram



(Fig.201) General block diagram

2-1-2. Mechanical Section

Since a disk is flexible recording media made of mylar film and data interchangeability between disk and FDD is required, the mechanical section of the FDD uses precision parts and it is also assembled carefully and precisely. For this reason, only trained technicians can handle the internal mechanism. Never apply excessive impact nor drop the FDD down on the desk.
The mechanical section is constructed with frame, door mechanism, disk clamp mechanism, disk rotation mechanism, magnetic head and carriage, head load mechanism (or CSS mechanism), head seek mechanism, various detection mechanisms, etc.

(1) Frame

The main structure for mounting the various mechanisms and printed circuit boards. The frame is made of aluminum diecast to maintain the stability of the FDD in strength, precision, durability, and expansion coefficient.

(2) Door mechanism and disk clamp mechanism

The door mechanism is constructed with main parts of set arm which forms the structure for installing the disk on the spindle, other parts of front lever, clamp arm, etc. The set arm is attached to the rear of the frame with leaf spring and a collet, which forms the disk clamp mechanism, is attached on the tip of the set arm.
When a disk is inserted and the door (front lever) is closed, the collet is inserted into the center hole of the disk and the disk is clamped in the correct position along the outer circumference of the collet.

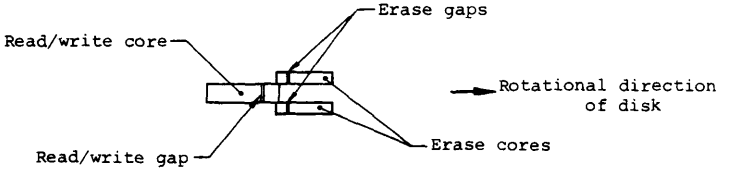
(3) Disk rotation mechanism

The disk rotation mechanism comprises DD motor Ass'y (spindle motor)

which includes spindle.

The DD motor is an outor-rotor type DC brushless motor which has the long life of 30,000 hours or more in continuous rotation. Rotational speed is 300rpm for B and F models or 360rpm for G model. It is maintained at a stable condition against load variations and environmental changes by a feedback signal from AC tachometer in the rotor. The collet and the spindle are combined precisely to maintain the center position correctly without damaging the center hole of a disk and so as to make the head be in contact with the disk at a correct position.

(4) Magnetic head and carriage



(Fig.202) External view of magnetic head core

The magnetic head assembly (head carriage Ass'y) of this FDD has two heads. One is for side 1 surface of the disk and the other for side 0 surface of the disk (down surface when the FDD is situated horizontally). Both of the side 0 and side 1 heads are supported by specially designed flexure. The two magnetic heads are mounted accross the disk on one head carriage, and their surfaces are designed for minimum disk wear and maximum read output. The head itself is a long life type for improved head wear.

The core of the head is constructed with read/write gap which is used for data write and data read operations and two erase gaps which are used to erase the edges of the recorded track immediately after the recording (tunnel erase). The head carriage Ass'y forms the most

important part of the FDD and it is specially assembled with high precision.

(5) Head load mechanism or CSS mechanism

The head load mechanism is used for models with head load solenoid and the CSS mechanism is used for CSS model without head load soelnoid.

The head load mechanism functions to make the head in contact with a disk only while a head load command is received so as to reduce wear of disk and head surfaces. This mechanism consists of head load solenoid, arm lifter, head protector, etc. When the solenoid is energized, the arm lifter goes down and the side 1 head attached to the upper arm of the head carriage is depressed against the side 1 surface of a disk with an appropriate pressure, and the disk is held between two heads. The side 0 surface of the head and the disk are set to nearly the same height and the depression of the side 1 head produces the stable contact between the heads and the disk.

The CSS mechanism consists of CSS cam and head protector. In the CSS model, the magnetic heads are always in contact with a disk as far as a disk is installed. In order to elongate the disk and head lives, it is required to make the disk rotate only during read or write operation. The CSS cam is designed to protect the contact of side 0 and side 1 heads directly when the front lever is closed without a disk.

For the purpose of protecting the head being caught and damaged by the head window edge at disk insertion or ejection, the head protector is also equipped to both of the head load and CSS mechanisms to lift up the disk jacket.

(6) Head seek mechanism

The head seek mechanism consists mainly of stepping motor with a capstan

(pooly), steel belt (band), and guide shafts. The head carriage is connected to the capstan of the stepping motor through the steel belt and is slided along the guide shafts.
The stepping motor rotates 2 steps (3.6°) in 48tpi model and 1 step (1.8°) in 96tpi models for one track space. To improve the continuity of head seek operation and precision of head positioning, hybrid type 4-phase stepping motor is driven in a unique manner which brought a success in reducing the heat radiation and to obtain a highly precise positioning.
The parallelism and the distance between the shafts and the center line of a disk, and shafts and capstan themselves are precisely machined. Also the thermal expansion of the frame, steel belt, carriage, etc. are taken into consideration in the process of design so that they are mutually offset with the expansion of the disk.

(7) Detection mechanisms

(a) File protect detection mechanism

This mechanism is constructed with an LED and a photo-transistor to detect the existence of the write enable notch of the disk jacket. When a disk with the notch covered is installed and the light pass for detection is disturbed, no write or erase current will be supplied to the read/write and erase heads and the recorded information on the disk is protected from an erroneous input of a write command.
The LED is mounted on the PCBA DD motor servo and the photo-transistor on the PCBA front OPT.

(b) Track 00 detection mechanism

This mechanism is constructed with a photo-interrupter for detecting the outermost track position (track 00) of the head carriage.
The photo-interrupter is mounted on the main PCBA (PCBA MFD control). Inside tracks from the track 00 on the disk are used. Even if an

erroneous step out command is input from the track 00 position, the command will be ignored by the internal circuit of the FDD.
If the head moves out from the track 00 by some reason such as impact during transportation, the head carriage strikes the frame (functions like a track 00 stopper) to protect the head from moving out of the returnable range at a next power on.

When step-in commands are input from the innermost track, the head moves toward inward and stops with an appropriate space left against the head window edge of the disk. In order to recalibrate the track from this position (returning operation to the track 00), it is required to input the step-out command with several additional steps to the maximum track number.

Caution: Sense timing of the track 00 position will change if you loosen a fixing screw of the main PCBA. This is because that the track 00 photo-interrupter is mounted on the PCBA. Be sure to readjust the track 00 sensor timing according to item 3-4-13.

(c) Index detection mechanism

LED and photo-transistor for detecting the index hole are located at the index window area of the disk jacket.
The LED is mounted on the PCBA DD motor servo (in the rotor of spindle motor) and the photo-transistor on the PCBA front OPT. The index hole will be detected along the rotation of the disk.

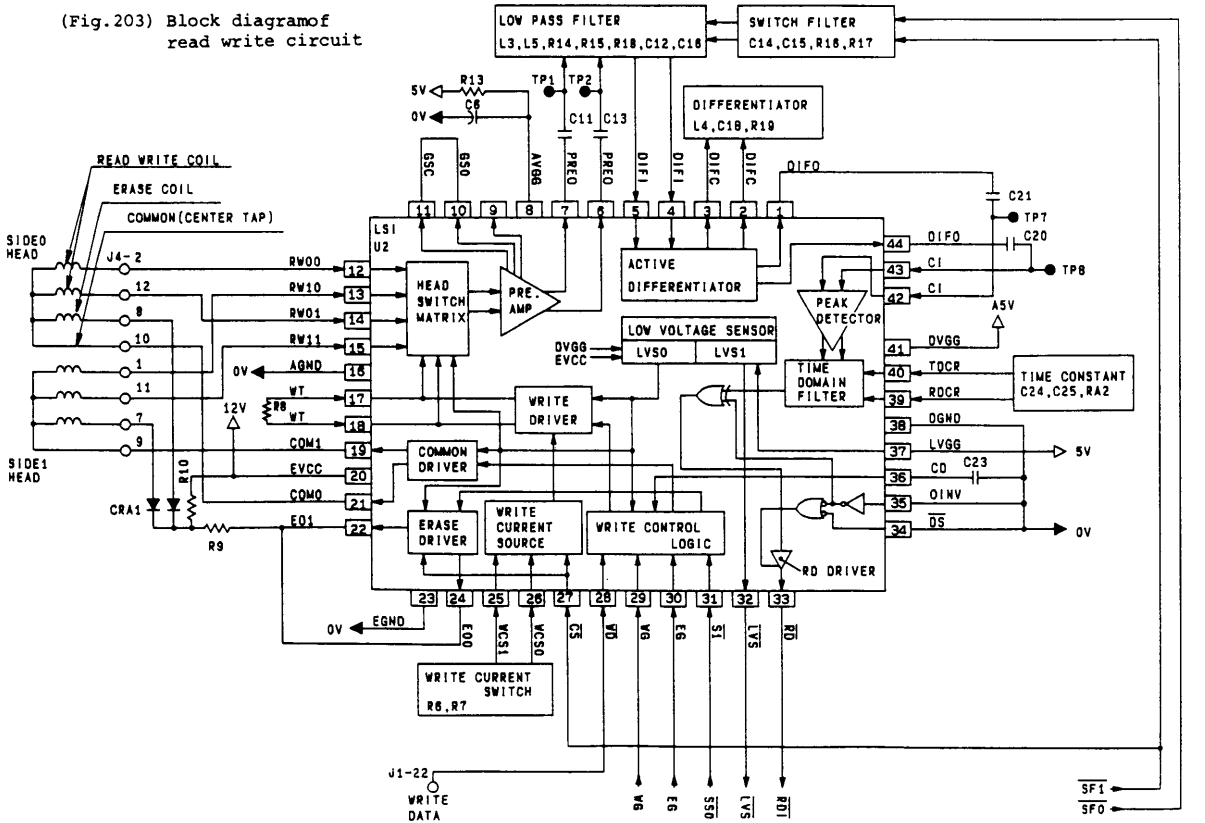
2-2. CIRCUIT DESCRIPTIONS

The electronics of the FDD is constructed with three sections which are read write circuit, control circuit, and servo circuit. Read write circuit and control circuit are mounted on the PCBA MFD control (main PCBA), and servo circuit is on the PCBA DD motor servo.

2-2-1. Read Write Circuit

The read write circuit is constructed with mode selector, read circuit, write circuit, low voltage sensor. They are mostly packed in a read write LSI (bipolar LSI, U2).
Fig.203 shows the block diagram.

(Fig.203) Block diagramof
read write circuit



2-2-1-1. Mode selector

Mode selector is constructed with the switch filter and write current switch.
Table 201 shows the switching condition of the read write circuit by the track switch signal ($\overline{SF0}$ and $\overline{SF1}$ signals in the schematic diagram) from the control circuit.

(1) Switch filter

Switch filter is used for eliminating the influence of saddle waveform (refer to Fig.204) at the outer tracks.
When the $\overline{SF0}$ and $\overline{SF1}$ are LOW level, the switch filter capacitors, C14 and C15 are activated to increase the capacity of the low pass filter capacitor, C16. This state is the on-state of the switch filter, and the cut-off frequency of the low pass filter is set to low.

(2) Write current switch

Write current switch is used only for 96tpi models. It is used for making the write current in outer tracks higher than in inner tracks to improve the over-write characteristics (write 2F after 1F write and measure the residual frequency components of 1F).

Write current is supplied to the write driver by write current source in the read write LSI, U2. The supplied value from this current source can be calculated from the following expression combining the external resistors R6 and R7.

Outer tracks: $Iw \approx \frac{13.2}{R6} + \frac{12.7}{R7}$ --- No.1

Inner trasks: $Iw \approx \frac{13.2}{R6}$ --- No.2

Erase current is calculated from the following expression. Erase current is not switched depending on the track position.

$$Ie \simeq \frac{10.8}{R9} \quad \text{--- No.3}$$

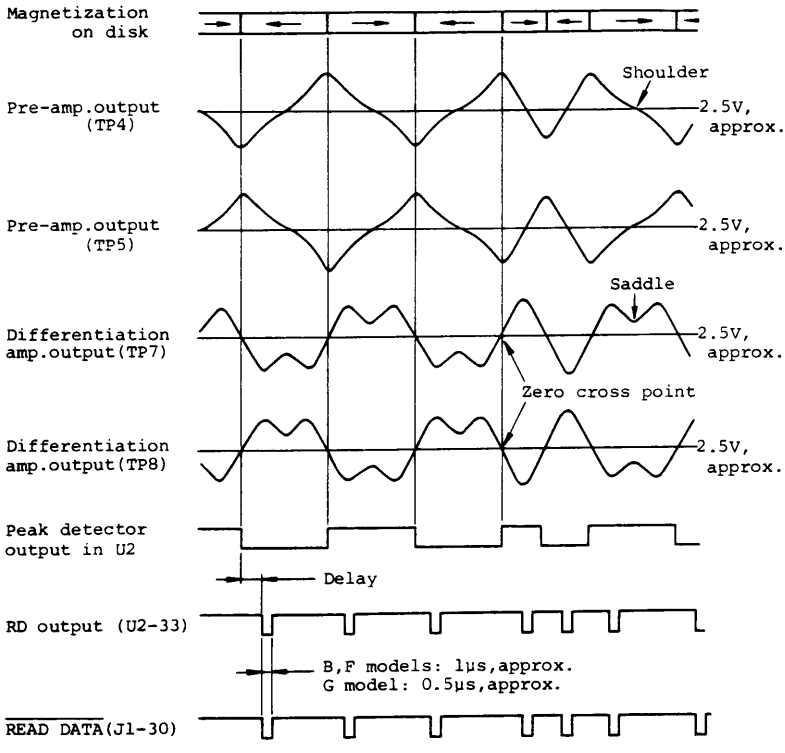
Switching item	Models and track position			
	B (48tpi)		F,G (96tpi)	
	Tr.00∿21	Tr.22∿39	Tr.00∿43	Tr.44∿79
$\overline{SF0}$, $\overline{SF1}$ signals	L	H	L	H
Switch filter	ON	OFF	ON	OFF
Write current sw. (Current exp.)	No.1	No.2	No.1	No.2
Erase driver (Current exp.)	Constant No.3	←	←	←

(Table 201) Switching function for read write circuit

2-2-1-2. Read circuit

The read circuit consists of head matrix switch, pre-amplifier, low pass filter, differentiation amplifier, peak detector, bi-directional edge detector, output driver, etc. Main circuits are enclosed in the read write LSI, U2.

The minute voltage induced in read operation by the read/write head is input to pre-amplifier via matrix switch for selecting side 0/1 heads. The pre-amplifier has three gain setting terminals, GS0, GS1 and GSC. In B and F models, GS0-GSC is shorted to obtain the gain of 115 times, approx., while GS1-GSC is shorted in G model to obtain the gain of 230 times, approx.
The pre-amp. output is supplied to the differentiation amplifier via the low pass filter and the switch filter to eliminate undesirable high frequency noises. The differentiation amplifier phase-shifts the peak position of the reproduced waveform to zero cross point, and at the same time, further amplifies the signal with the most appropriate equalization. The differentiated outputs are supplied to the peak detector constructed with a comparator after passing through the coupling capacitors, C20 and C21, and converted into a square wave. Then the edges of the square wave are detected by the bi-directional edge detector and they are output as the read data paulses from the FDD through the RD driver and the RD/INDEX gate in the control LSI, U1.



(Fig.204) Read amplifier and peak detector waveforms

2-2-1-3. Write circuit

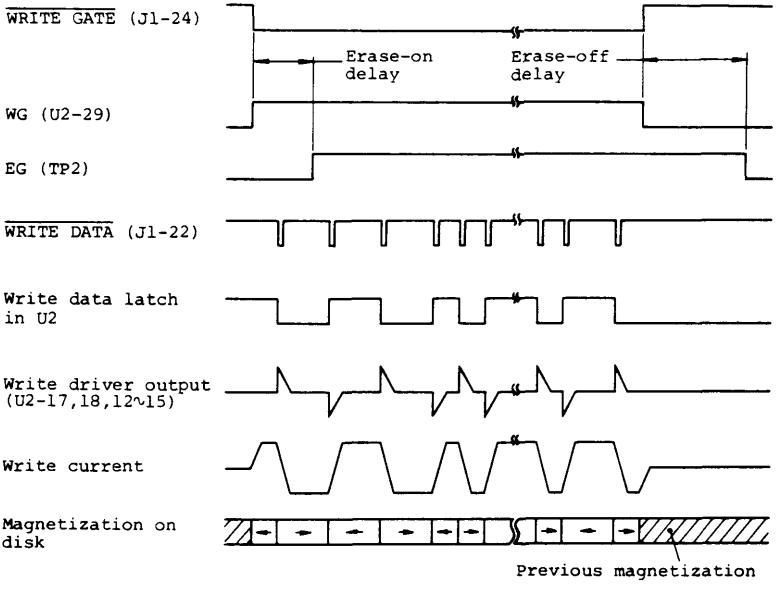
The write circuit consists of write control logic, write current source, write driver, erase driver, common driver, and etc. Most of the circuits are enclosed in the read write LSI, U2.
Common driver output terminals, COM0 and COM1 are connected to the common terminals (center taps) of the side 0 and side 1 heads, respectively. The outputs of the common driver are controlled by the SIDE ONE SELECT ($\overline{SI}$), write gate (WG), and erase gate (EG) signals supplied through the write control logic. When the COM0 or the COM1 is HIGH level (11.5V, approx.), the power to the read circuit is cut off in the read write LSI to inhibit the read operation.

Input signals			FDD operation	Output voltage (approx.)	
$\overline{SI}$	WG	EG		COM0	COM1
H	L	L	SIDE 0 read operation	2.7V	0V
H	H	-	SIDE 0 write operation	11.5V	0V
H	-	H	SIDE 0 write operation	11.5V	0V
L	L	L	SIDE 1 read operation	0V	2.7V
L	H	-	SIDE 1 write operation	0V	11.5V
L	-	H	SIDE 1 write operation	0V	11.5V

(Table 202) Common driver output

The EG signal supplied from the erase timer in the control circuit changes to HIGH or LOW level with an appropriate time delay against the WG signal (refer to Fig.205). Since the erase gaps locate about 0.85mm (B and F models) or 0.585mm (G model) backward from the read/write gap, it is necessary for the erase driver to delay the WG signal so that the written data is completely trimmed by the erase head (tunnel erase). The tunnel erase produces a guard band between the tracks preventing deterioration of the S/N ratio resulting from a off-track (positioning error). It also ensures disk interchangeability.
The WRITE DATA input pulse is latched by the write data latch in the

write control logic. And appropriate write current determined by the write current source is supplied to the read/write head with turning on and off the two write drivers alternately.

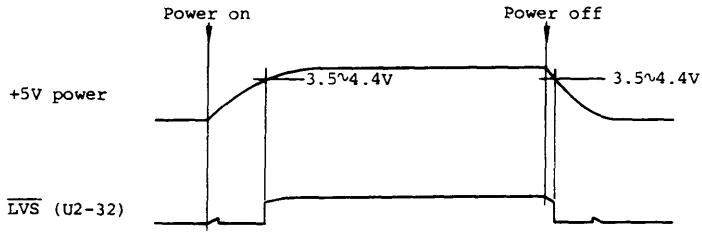


(Fig.205) Typical waveform of write circuit operation

2-2-1-4. Low voltage sensor

The low voltage sensor (LVS) is equipped to protect the FDD from erroneous operation due to the internal circuit construction of the FDD during unstable state of the power voltage such as at power on or off. Two sensors of LVS0 and LVS1 are equipped in the read write LSI, U2. LVS0 monitors the +5V voltage supplied to the internal circuit of the read write LSI. If the voltage is lower than 3.5V through 4.4V, it supplies signals to inhibit the operation of the common driver, write driver, erase driver, and write control logic in the LSI, which protect the disk from the erroneous write or erroneous erase during unstable state of the power voltage.

LVS1 is equipped to generate $\overline{LVS}$ signal to be supplied to the control circuit in item 2-2-2. As well as LVS0, it is activated in the range of 3.5V through 4.4V. The monitored voltage by the LVS1 is only +5V connected to the LVGG terminal (pin 37) of the read write LSI. While the $\overline{LVS}$ signal is LOW level, all the control circuits (mainly control LSI, U1) are reset.



(Fig.206) Typical waveform of low voltage sensor

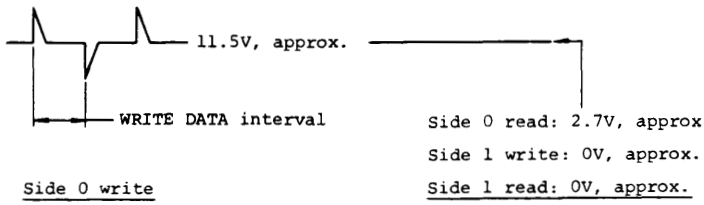
2-2-1-5. Function and operating waveform of read write LSI terminals

Following shows the function of the read write LSI, U2 and typical operating waveforms.

(1) Pre-amplifier

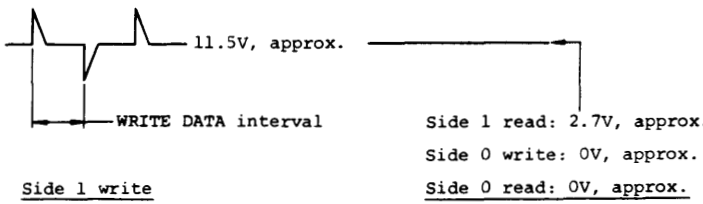
(a) RW00 (pin 12), RW01 (pin 14)

Terminals for side 0 head connection.



(b) RW01 (pin 13), RW11 (pin 15)

Terminals for side 1 head connection.



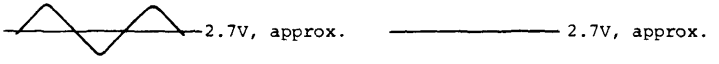
(c) GSC (pin 11), GS0 (pin 10), GS1 (pin 9)

Setting terminals of pre-amplifier gain.
If GSC-GS0 is shorted or connected with a capacitor, the differential voltage gain of the pre-amplifier is 115 times, approx.

If GSC-GSl is shorted or connected with a capacitor, it is increased to 230 times, approx.

(d) PREO (pin 7, pin 6)

Differential output terminals of the pre-amplifier. The phase of pin 6 and 7 are opposite each other. Refer to Fig.204.

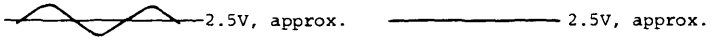


Read Write

(2) Differentiation amplifier

(a) DIFI (pin 5, pin 4)

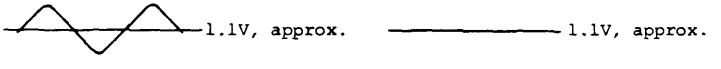
Differential input terminals to the differentiation amplifier. The phase of pin 5 and 4 are opposite each other.



Read Write

(b) DIFC (pin 3, pin 2)

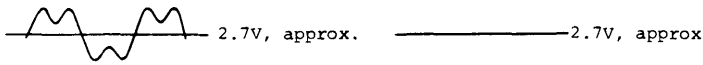
Time constant setting terminals of the differentiation amplifier. The phase of pin 3 and 2 are opposite each other.



Read Write

(c) DIFO (pin 1, pin 44)

Differential output terminals of the differentiation amplifier. The phase of pin 1 and 44 are opposite each other.



Read Write

(d) CI (pin 43, pin 43)

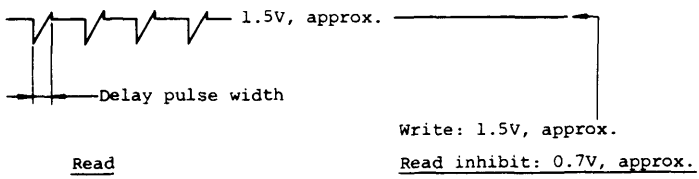
Differential input terminal of the comparator (peak detector). The phase of pin 43 and 42 are opposite each other.

Read Write

(3) Time domain filter

(a) TDCR (pin 40)

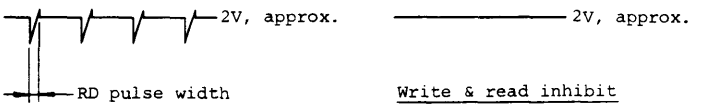
Pulse width setting terminal of the filter.



Read

(b) RDCR (pin 39)

Pulse width setting terminal for the RD output pulse.



Read

(4) Write circuit

(a) COM0 (pin 21), COM1 (pin 19)

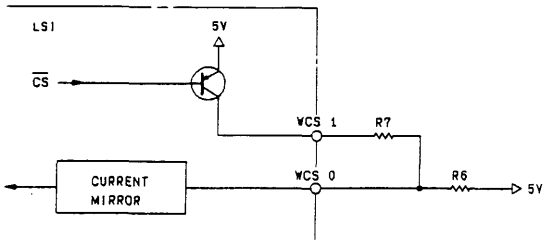
Output terminals of the common driver. Two terminals are equipped for the side 0 and side 1 heads respectively.
Refer to tables 202 and 203 as to the output voltage at each operating condition.

(b) E00 (pin 24), E01 (pin 22)

Output terminals of the erase driver which is constructed with open collector NPN transistors. Two terminals are equipped. While the EG input terminal is HIGH level, one of the drivers which is selected by the $\overline{CS}$ input terminal turns on (becomes LOW).
Refer to Table 203.

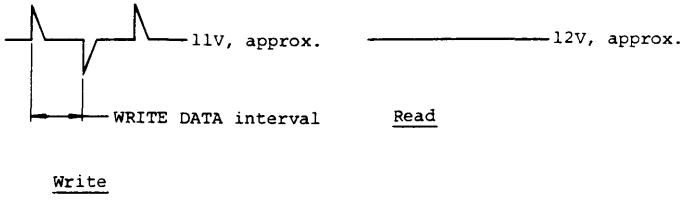
(c) WCS0 (pin 26), WCS1 (pin 25)

External resistor terminals for setting the write current. Following shows the circuit diagram of the terminal. By the pull up resistors for the WCS0 and WCS1, the write current is determined. The current is calculated by the expression in item 2-2-1-1 (2).



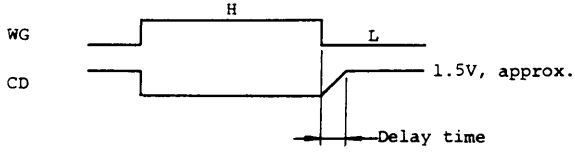
(d) WT (pin 17, pin 18)

External resistor terminals for the head termination in write operation. An appropriate value of resistor is connected externally not to occur the abnormal overshoot nor undershoot at write operation. These terminals are also used for the asymmetry adjustment at read operation.



(e) CD (pin 36)

In order to protect the head from undesirable magnetization, this terminal is used to set the delay time to keep the write current flow at a determined direction for 1 through 5μs, approx., after the completion of a write operation (WG turns off).



(f) $\overline{CS}$ (pin 27) --- Schmitt TTL input

Control input terminal having following two functions. Refer to Table 203.

i) ON/OFF control of write current setting terminal WCS1.
ii) Selection of erase driver output terminals EO0 and EO1.

(g) $\overline{WD}$ (pin 28) --- Schmitt TTL input

WRITE DATA input terminal from the host controller.

Write Read

(h) WG (pin 29), EG (pin 30) --- Schmitt TTL input

Control input terminals for write permit (WG) and erase permit (EG) from the control circuit in the FDD. Refer to Tables 202 and 203.

(5) Others

(a) $\overline{S1}$ (pin 31) --- Schmitt TTL input

Input terminal for controlling the side selection from the control circuit. The terminal functions as the selector for common driver outputs COM0/COM1 and for head switch matrix of RW00,01/RW 10,11 terminals. Refer to Table 203.

(b) $\overline{LVS}$ (pin 32) --- Open collector TTL output

$\overline{LVS}$ signal output terminal to the control circuit of the FDD. Refer to item 2-2-1-4.

(c) OINV (pin 35), $\overline{DS}$ (pin 34) --- TTL input

Control input terminal of RD output.

(d) $\overline{RD}$ (pin 33) --- Totempole TTL output

Read data pulse output terminal to the control circuit.
The output is controlled by OINV and $\overline{DS}$ input signals as shown in Table 203. In this FDD, both of the OINV and $\overline{DS}$ inputs are fixed to LOW level and negative pulses are output at this terminal. Refer to Fig.204.

(e) AGND (pin 16), EGND (pin 23), and DGND (pin 38)

0V power terminals mainly for the following circuits in the LSI.

AGND: Analog operation circuits such as pre-amplifier.
EGND: Erase driver.
DGND: Digital operation circuits such as write control logic.

(f) AVGG (pin 8), DVGG (pin 41), LVGG (pin 37)

+5V power terminals mainly for the following circuits in the LSI.

AVGG: Analog operation circuits such as pre-amplifier.
DVGG: Digital operation circuits such as write control logic.
LVGG: Low voltage sensor (LVS1)

(g) EVCC (pin 20)

+12V power terminal for common driver.

	Inputs						Outputs						Write
	WG	EG	$\overline{S1}$	$\overline{CS}$	$\overline{DS}$	OINV	$\overline{LVS}$	COM0	COM1	EO0	EO1	RD	current
Read	L	L	H	-	L	L	H	R	0	Z	Z	N	0
	L	L	L	-	L	L	H	0	R	Z	Z	N	0
	L	L	-	-	H	L	H			Z	Z	Z	0
	L	L	H	-	-	H	H	R	0	Z	Z	P	0
	L	L	L	-	-	H	H	0	R	Z	Z	P	0
Write/Erase	H	L	H	H	-	-	H	Hi	0	Z	Z	F	WCS 0
	L	H	H	H	-	-	H	Hi	0	0	Z	F	0
	H	H	H	H	-	-	H	Hi	0	0	Z	F	WCS 0
	H	L	L	H	-	-	H	0	Hi	Z	Z	F	WCS 0
	L	H	L	H	-	-	H	0	Hi	0	Z	F	0
	H	H	L	H	-	-	H	0	Hi	0	Z	F	WCS 0
	H	L	H	L	-	-	H	Hi	0	Z	Z	F	WCS 0+1
	L	H	H	L	-	-	H	Hi	0	Z	0	F	0
	H	H	H	L	-	-	H	Hi	0	Z	0	F	WCS 0+1
	H	L	L	L	-	-	H	0	Hi	Z	Z	F	WCS 0+1
	L	H	L	L	-	-	H	0	Hi	Z	0	F	0
	H	H	L	L	-	-	H	0	Hi	Z	0	F	WCS 0+1
LV	-	-	-	-	-	-	L	0	0	Z	Z	Z	0

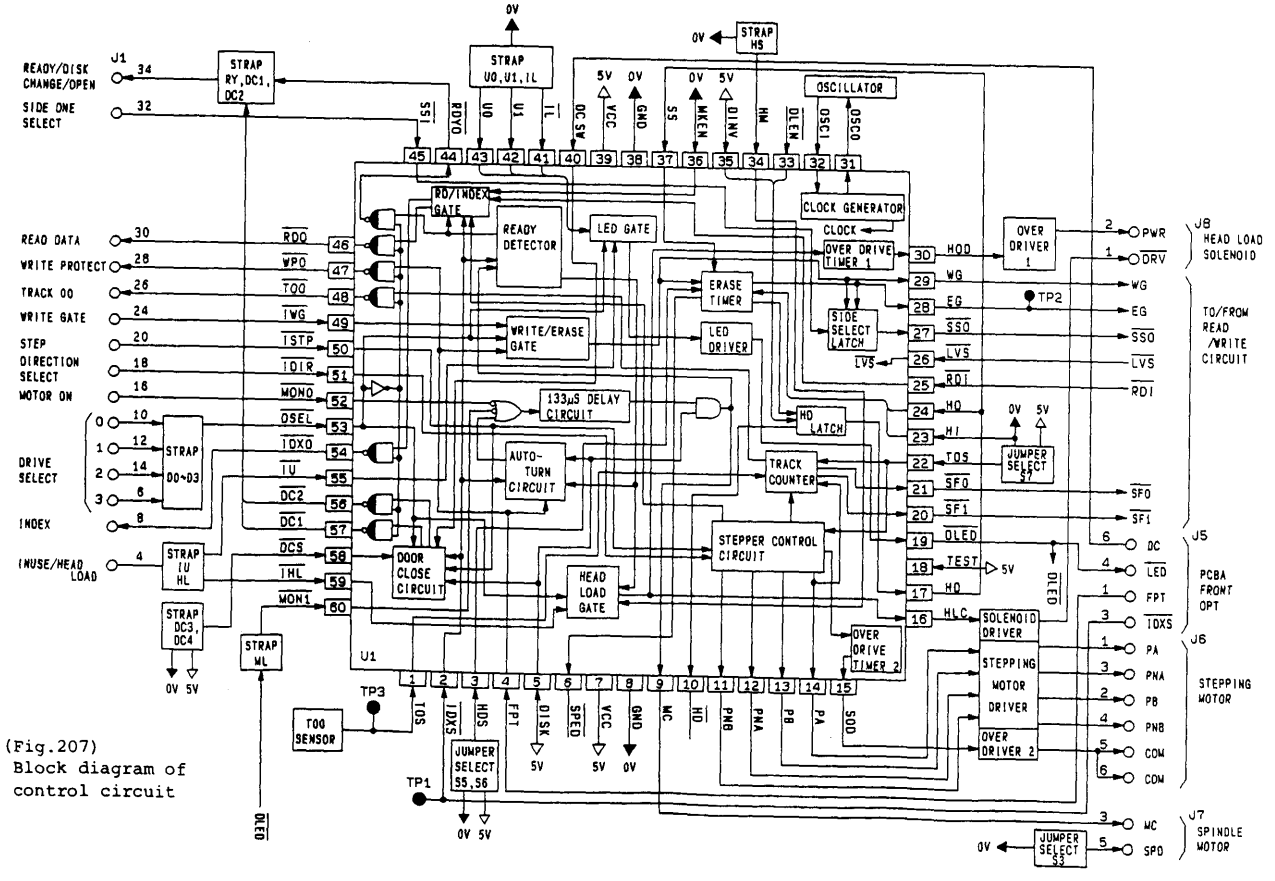
L: Logic level 0 (LOW)
H: Logic level 1 (HIGH)
Z: High impedance (OPEN)
Hi: COM voltage, 11.5V, approx.
R: COM voltage, 2.7V, approx.
P: Positive pulse
N: Negative pulse
F: FALSE (No pulse output)
LV: Low voltage

(Table 203) Read write LSI control table

2-2-2. Control Circuit

The control circuit consists of strap circuit, front LED control circuit, head load control circuit, write/erase control circuit, motor-on gate, ready detector, stepping motor control circuit, track counter, RD/INDEX gate, interface driver, etc.

Almost all the circuits except for strap circuit and stepping motor driver are enclosed in the control LSI (bipolar LSI, Ul).
Fig.207 shows the block diagram.



(Fig.207)
Block diagram of control circuit

2-2-2-1. Strap circuit

In order to select the various function by users, several strap posts are equipped. Refer to the Specification items 1-11 and 1-12 as to the details of strap function.
Some models have not strap posts. These models have soldered jumping wires instead of the strap posts, and the function is fixed. (Refer to the version table in the schematic diagram).

2-2-2-2. Front LED control circuit

The circuit consists of LED gate and LED driver. They are enclosed in the control LSI, U1.

DRIVE SELECT ($\overline{DSEL}$) and IN USE ($\overline{IU}$) signals via strap circuit are input to the LED gate. According to the function selected by U0/U1/IR straps. these input signals are gated to output as the $\overline{DLED}$ signal through the LED driver. While the $\overline{DLED}$ signal is LOW level, the front LED turns on.

Strap setting			U1 input			LED turn-on condition
U0	U1	IL	U0	U1	IL	($\overline{DLED}$: LOW)
OFF	ON	OFF	H	L	H	$\overline{IU}$(L) + $\overline{DSEL}$(L)
ON	OFF	OFF	L	H	H	$\overline{IU}$(L)
ON	ON	OFF	L	L	H	$\overline{IU}$(L) + $\overline{DSEL}$(L) * $\overline{RDYO}$(L)
OFF	ON	ON	H	L	L	IUL + $\overline{DSEL}$(L)
ON	OFF	ON	L	H	L	IUL
ON	ON	ON	L	L	L	IUL + $\overline{DSEL}$(L) * $\overline{RDYO}$(L)

Notes 1. $\overline{RDYO}$: Output signal from ready detector in U1. LOW in ready.
$\overline{IU}$: IN USE input signal LOW.
IUL: Internal signal of LSI. Latched signal of IN USE by leading edge of DRIVE SELECT.

2. $\overline{IU}$ and IUL conditions are effective only when the IU strap is on-state.

(Table 204) Front LED turn-on condition

2-2-2-3. Head load control circuit

The circuits consists of head load gate, overdrive timer 1, solenoid driver, and overdrive circuit 1.

(1) Head load gate

DRIVE SELECT ($\overline{DSEL}$) and HEAD LOAD ($\overline{IHL}$) signals via strap circuit are input to the head load gate in the control LSI, U1. According to the selected function designated by HL/HS straps, these input signals are gated to output as the HLC signal to the solenoid driver U3 (pin 3-14). While the HLC signal is HIGH level, the head load solenoid is activated.

Strap setting		U1 input		Head load solenoid turn-on condition (HLC: HIGH)
HL	HS	IHL	HM	
OFF	OFF	L	H	PRDY
OFF	ON	L	L	PRDY * $\overline{DSEL}$(L)
ON	ON	L/H	L	PRDY * $\overline{DSEL}$(L) * $\overline{IHL}$(L)

Notes PRDY: Ready + Pre-ready
Pre-ready: Internal signal of LSI. It goes to TRUE 50msec before the ready state. Refer to item 2-2-2-6.

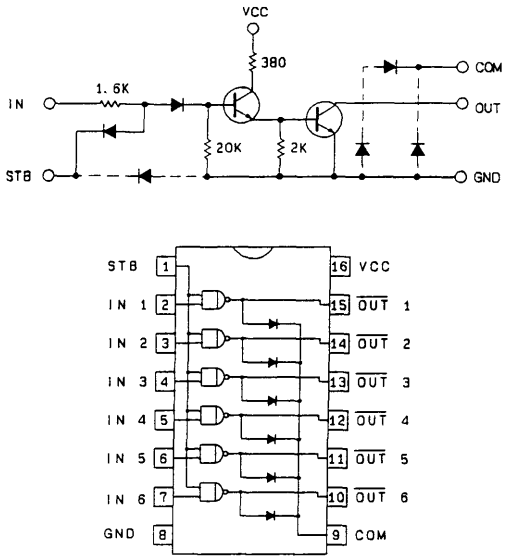
(Table 205) Head load solenoid turn-on condition

(2) Solenoid driver

The HLC signal from the control LSI is supplied to the driver IC, U3. Refer to Fig.208 as to the construction of U3.

(3) Overdrive timer 1

The HLC signal is also supplied to the overdrive timer 1 in the control LSI. The overdrive timer is constructed with a retriggerable counter.

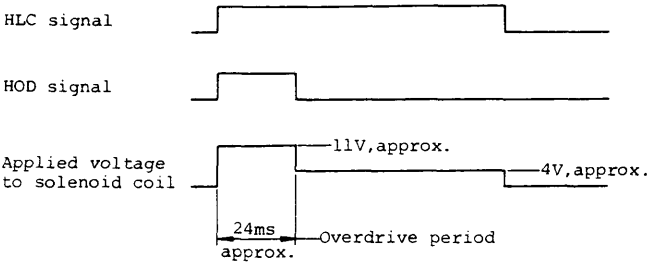


(Fig.208) Construction of driver IC, U3

For the initial 24msec of the solenoid activation, it maintains the HOD output at HIGH level.

(4) Overdrive circuit 1

The HOD output signal is supplied to the overdrive circuit 1 constructed by transistors Q2 (NPN) and Q1 (PNP) and it makes Q1 turn on while the HOD signal is HIGH level. +12V power is applied to the solenoid at that time to execute the drawing-in action of the solenoid securely.
After the overdrive period, the solenoid maintains its situation with +5V power through the diode CR1 to save the power.



(Fig.209) Overdrive timing of head load solenoid

2-2-2-4. Write/erase control circuit

The circuit consists of write/erase gate and erase timer. Most of the parts of the circuit are enclosed in the control LSI, U1.

(1) Write/erase gate

The gate judges whether new data can be written on an installed disk. If it can be, the circuit supplies the WG signal for the read write LSI and erase timer.
The WG signal goes to TRUE in the following condition.

$WG(H) = \overline{DSEL}(L) * \overline{IWG}(L) * FPT(L)$

Notes WG: Write operation at HIGH.
$\overline{DSEL}$: DRIVE SELECT input signal LOW.
$\overline{IWG}$: WRITE GATE input signal LOW.
FPT: File protect sensor output (FPT input of LSI) LOW.
The same as that the file protect sensor detects the write enable notch (light passing condition) of a disk which is equivalent to that the $\overline{WPO}$ (WRITE PROTECT) output signal is HIGH (write-enable condition).

(2) Erase timer

The circuit to make the WG signal delay from the write/erase gate as in Fig.205 to output the EG signal for the read write LSI. Refer to item 2-2-1-3.
Various delay time can be set by HDS, H0, H1, and SS input terminals of the control LSI. By these input terminals, the output of HD and $\overline{SPED}$ terminals are also set which executes the selection of the FDD function. The setting of this FDD, however, is fixed as shown in the following Table.

FDD model	Ul input				Ul output		Erase delay	
	HDS	H0	H1	SS	HD	$\overline{\text{SPED}}$	On-delay	Off-delay
B,F models (300rpm)	L	L	L	L	L	H	250∿267μs	916∿935μs
G model (360rpm)	H	H	L	H	H	L	208∿217μs	558∿567μs

Notes: 1. The figure in the above Table is the calculated value excluding the oscillator tolerance and propagation delay.

2. H0 and SS input terminals are connected to HD output. HD output state is determined by HDS input signals.

(Table 206) Erase delay control table

2-2-2-5. Motor-on gate

The circuit, receiving a spindle motor-on command from the host controller, supply the MC (motor control) signal to the spindle motor servo circuit. The circuit consists of OR-gate, 133μs delay circuit and auto-turn circuit which are enclosed in the control LSI, U1.

A motor-on command input to the $\overline{\text{MON0}}$ or $\overline{\text{MON1}}$ terminal is supplied to 133μs delay circuit via the OR-gate to be delayed for 133 ∿ 267μs. The delay circuit eliminates the noises mixed onto the interface line and protects the control circuit from erroneous operation.
The MC signal goes to TRUE in the following conditions.

MC(H)= ($\overline{\text{MON0}}$(L) + $\overline{\text{MON1}}$(L)) * 133μs delay * DISK(H)

Notes MC: Motor rotation at HIGH.
$\overline{\text{MON0}}$: MOTOR ON input signal LOW.
$\overline{\text{MON1}}$: $\overline{\text{DLED}}$ is low at ML strap is ON.
(Front bezel indicator is ON).
DISK: Fixed to TRUE (HIGH).

The auto-turn circuit makes the spindle motor rotate automatically at a disk insertion to improve the chucking accuracy. The circuit is set by an information of disk insertion from the file protect sensor, and is reset by a detection of ready state or by a detection of more than 8.7 seconds passing after the $\overline{\text{IDXS}}$ input terminal keeping TRUE (LOW). Even though the FDD goes to the ready state by a command from this circuit, the $\overline{\text{RDYO}}$ output signal in item 2-2-2-6 maintains FALSE (HIGH level).

2-2-2-6. Ready detector

Ready detector consists of 80% speed detector, internal ready latch, MON delay circuit which are enclosed in the control LSI, U1. In the block diagram, these circuits are shown as one block of ready detector.

The MC signal for controlling the spindle motor is input to the ready detector which enables the operation of all the above three circuits. As the motor speed increased, the 80% speed detector operates first, and then internal ready latch is set when the index ($\overline{IDXS}$) pulse interval becomes less than 250msec, approx. (i.e. disk speed reaches more than 80% of 300rpm).
On the other hand, the MON delay circuit generates MON delay 1 signal (443 ∿ 461msec delay) after the level change of the MC signal to TRUE (HIGH). When the outputs of the MON delay 1 and the internal ready latch are coincident with each other, FDD goes to the pre-ready state and then it reaches to the ready state after further 49 ∿ 51msec delay (MON delay 2). The sum of the delay time is 492 ∿ 512ms.

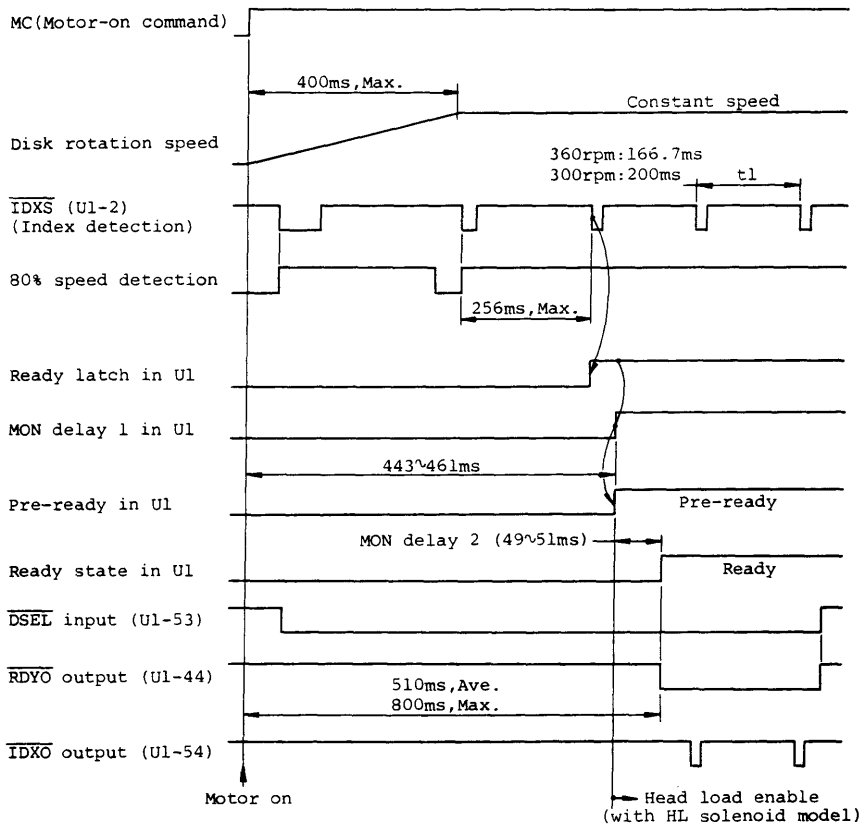
If $\overline{DSEL}$ input signal is TRUE after the FDD reaches to the ready state, the $\overline{RDYO}$ signal (which indicates that the FDD is in read/write ready state) is output from the FDD. Fig.210 shows the timing chart of the ready detector. The $\overline{RDYO}$ signal goes to TRUE (LOW) in the following condition.

$$\overline{RDYO}(L) = \underbrace{\{MC(H) * 80\%\ speed * MON\ delay\ 1\}}_{\text{Pre-ready}} * MON\ delay\ 2 * \overline{DSEL}(L)$$

Notes $\overline{RDYO}$: Ready at LOW.
MC: Motor rotates at HIGH.
80% speed: Disk rotational speed is more than 80%, approx. of 300rpm.
MON delay 1: Internal signal of LSI. 443 ∿ 461ms after an input of motor-on command.

MON delay 2: Internal signal of LSI. 49 ∿ 51msec after the pre-ready state.

$\overline{\text{DSEL}}$: DRIVE SELECT input signal LOW



Notes 300rpm: B and F models 360rpm: G model

(Fig.210) Ready detector waveforms

All the three circuits of ready detector are reset by the MC signal goint to FALSE (LOW level).

2-2-2-7. Stepping motor control circuit

Stepping motor control circuit consists of direction latch, internal step generator, shift register, phase drive selector, overdrive timer 2, motor driver, and overdrive circuit 2.
All the above circuits except for the motor driver and overdrive circuit 2 are enclosed in the control LSI, U1. In the block diagram, all the enclosed circuit in the control LSI except for the overdrive timer 2 are shown as one block of the stepper control circuit.

(1) Direction latch

At every input of the STEP ($\overline{\text{ISTP}}$) pulse from the host controller, the direction latch samples and holds the head seek direction designated by the DIRECTION SELECT ($\overline{\text{IDIR}}$) signal. The latched output is supplied to the bi-directional shift register and changes the activating order of the stepping motor coil as shown in Fig.211.

(2) Internal step generator

The circuit has following purposes.

(a) The circuit generates an internal step pulse 3msec later from the STEP ($\overline{\text{ISTP}}$) input pulse. This function is executed only when the signal level at the TDS terminal is LOW (48tpi mode) and the stepping motor rotates for two step space (3.6°) in response to one STEP pulse. When the TDS is HIGH (96tpi mode), the stepping motor rotates for one step space in response to one STEP pulse.

(b) The circuit generates internal step pulses for auto-recalibration at every 3msec. The auto-recalibration starts when the $\overline{\text{LVS}}$ signal from the read write LSI is changed from LOW to HIGH after power-on and it continues until the track 00 position is detected.
During the execution of the auto-recalibration, the FDD maintains

Not-ready state ($\overline{\text{RDYO}}$ output HIGH) and the STEP ($\overline{\text{ISTP}}$) pulse input from the host controller is ignored.

(3) Shift register and phase drive selector

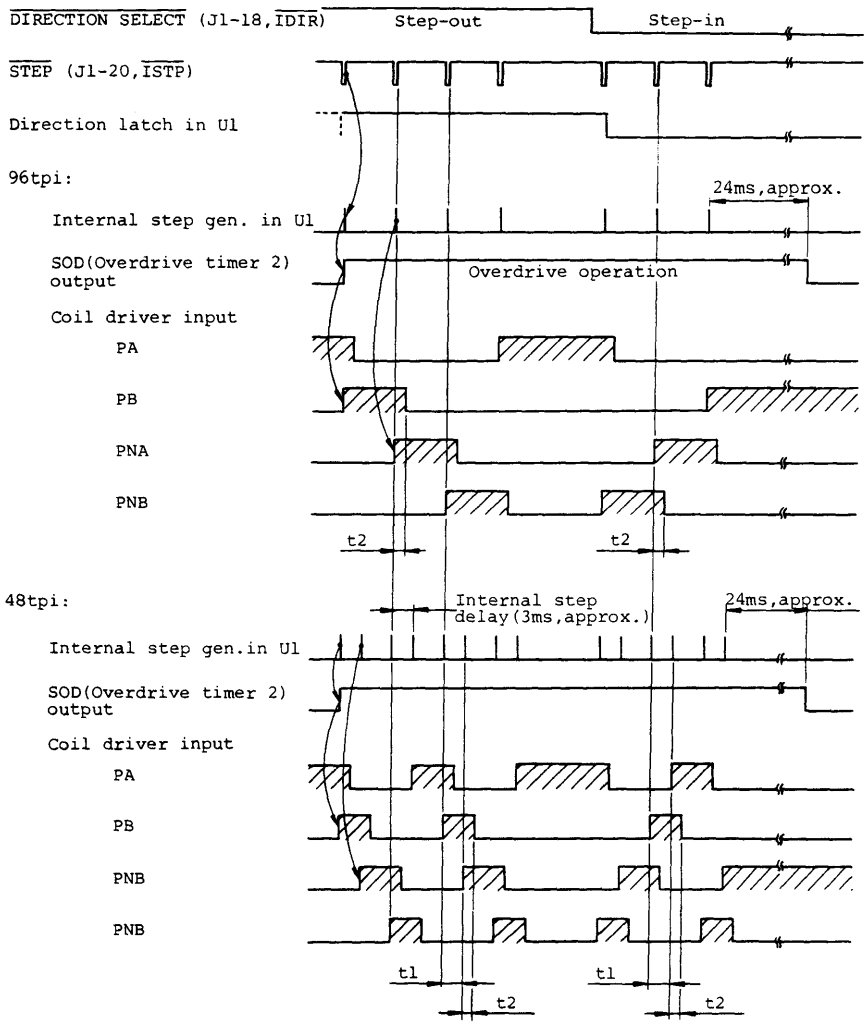
Step pulse and the output of the direction latch are supplied to the shift register and the phase drive selector to be converted to the appropriate timing signals for uni-polar 1-phase drive of the 4-phase stepping motor. These phase drive signals are output from the control LSI and supplied to the coil driver.
In order to improve the torque margin in the seek operation, partial 2-phase drive period is provided by the phase drive selector only in the initial stage when the drive phase is changed. Refer to Fig.211 for timing chart.

(4) Motor driver

Four outputs, PA, PB, PNA and PNB from the control LSI, U1 are input to the motor driver IC, U3. Refer to Fig.208 as to the construction of U3.

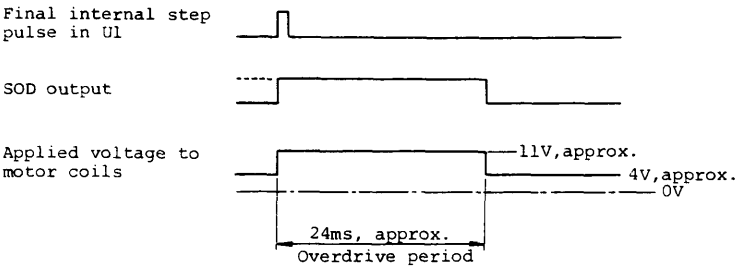
(5) Overdrive timer 2

External and internal step pulses are also supplied to the overdrive timer 2 in the LSI. The overdrive timer 2 is constructed with a retriggerable counter. During on-state of the timer (24msec, approx.), SOD output from the LSI goes to HIGH level. Refer to Fig.212.



t1: Internal step delay (3msec, approx.)
t2: Partial 2-phase activating period (0.6ms,approx.)

(Fig.211) Stepping motor control circuit waveform



(Fig.212) Stepping motor overdrive timing

(6) Overdrive circuit 2

The SOD signal is supplied to the overdrive circuit 2 constructed by U3 (pins 2-15) and PNP transistor Q3 and it makes Q3 turn on while the SOD signal is HIGH level. +12V power is applied to the stepping motor coils at that time to execute the seek and settling operations securely with high torque.

After the completion of the settling, only +5V power is supplied to the coils through the diode CR2 which minimize the power loss by supplying only the required torque for holding the stop position. By the above design, heat radiation is decreased to the minimum level and the power consumption of the stepping motor in seek stop is only 0.25W, approx.

2-2-2-8. Track counter

Track counter memorizes the track position and outputs track switch ($\overline{SF0}$, $\overline{SF1}$) signals for the read write circuit. It also outputs $\overline{T00}$ (TRACK 00) signal to the host controller. All the circuits are enclosed in the control LSI, U1.

The output signal from the track 00 sensor (TP3) is supplied to the T0S terminal of the LSI and is output as the $\overline{T00}$ signal through the gate and latch circuit in the track counter. The $\overline{T00}$ signal goes to TRUE in the following condition.

$\overline{T00}$(L)= T0S(H) * Step out * PA(H) * $\overline{DSEL}$(L)

Notes $\overline{T00}$: Track 00 detected at LOW.

T0S: Track 00 sensor output at TP3 (T0S input of LSI) is HIGH. Track 00 sensor detects the light disturbing wing of the head carriage (track 00 position).

Step out: Direction latch output is step-out direction.

PA: PA output from stepping motor control circuit is HIGH. Phase A coil of the motor is energized.

$\overline{DSEL}$: DRIVE SELECT input signal LOW.

When the $\overline{T00}$ signal goes to TRUE (LOW), the track counters constructed from up-down counters are reset. When a step-in operation is executed, the counter steps up and the $\overline{SF0/SF1}$ outputs change to HIGH at 44th track for 96tpi models (22th track for 48tpi model). Refer to item 2-2-1-1 as to the function of the $\overline{SF0}$ and $\overline{SF1}$ signals.

FDD models	TDS input terminal	$\overline{SF0}$ and $\overline{SF1}$ output signals
B (48tpi)	L	LOW at Tr.00∿21, HIGH at TR.22∿39
F,G (96tpi)	H	LOW at Tr.00∿43, HIGH at TR.44∿79

(Table 207) $\overline{SF0}$ and $\overline{SF1}$ output signals

2-2-2-9. RD/INDEX gate

READ DATA ($\overline{RDO}$) and INDEX ($\overline{IDXO}$) pulses are output to the host controller through the RD/INDEX gate which is enclosed in the control LSI, U1. The RD/INDEX gate changes its function according to the MKEN input level. In this FDD, the MKEN terminal is fixed to LOW level and the gate functions as follows.

$\overline{RDO}(L) = \overline{RDI}(L) * \overline{RDYO}(L) * \overline{DSEL}(L)$
$\overline{IDXO}(L) = \overline{IDXS}(L) * \overline{RDYO}(L) * \overline{DSEL}(L)$

Notes $\overline{RDO}$: Negative READ DATA pulse output to the host controller.
$\overline{RDI}$: Negative RD input from the read/write LSI.
$\overline{RDYO}$: $\overline{RDYO}$ output signal LOW. FDD is in ready state.
$\overline{DSEL}$: DRIVE SELECT input signal LOW.
$\overline{IDXO}$: Negative INDEX pulse output to the host controller.
$\overline{IDXS}$: Negative pulse input from the index sensor.

All the INDEX ($\overline{IDXO}$)output pulses are valid even if the first one by means of index latch circuit in the LSI in spite of the DRIVE SELECT input timing. For example, if the FDD is selected in the midst of an $\overline{IDXS}$ (index sensor output) pulse, the pulse will not be output to the host controller. The pulse will be output after one revolution of a disk.

2-2-2-10. Door-close circuit

Door-close circuit is optionally used in some special models with the door-close detection switch. The circuit is enclosed in the control LSI, U1 and it generates DOOR CLOSE or DRIVE STATUS signal using $\overline{DC1}/\overline{DC2}$ output terminals and DCS/DCSW input terminals of the LSI. Refer to the Specification and Schematic diagram as to the detailed condition including the DC1 ∿ DC4 straps.

In standard models without door-close switch, $\overline{DC1}$, $\overline{DC2}$, and DCSW terminals of the LSI are open and the door-close circuit is not utilized.

2-2-2-11. Other terminals and function of control LSI

Following explains other terminals and function of the control LSI, U1.

(1) OSC0/OSC1 terminals and clock generator

It supplies clocks for operation to all the circuits in the LSI by external ceramic oscillator.

(2) $\overline{\text{LVS}}$ input terminal

$\overline{\text{LVS}}$ signal input terminal from the read write LSI, U2.
When it is LOW, all the circuits in the control LSI are reset.

(3) $\overline{\text{SSI}}$ input and $\overline{\text{SSO}}$ output terminals

Terminals to select the disk side used.
The $\overline{\text{SSO}}$ output signal keeps LOW level while the $\overline{\text{SSI}}$ (SIDE ONE SELECT) input signal is LOW which makes the $\overline{\text{SI}}$ input of the read write LSI LOW to set the FDD to side 1 operating condition.

However, while the WG or EG output signal from the control LSI keeps HIGH level (write or erase operating condition), the $\overline{\text{SSO}}$ output signal does not change the state in spite of the $\overline{\text{SSI}}$ input signal and therefore, the change of side 0 $\rightleftarrows$ side 1 is not executed to complete the tunnel erase operation (refer to item 2-2-1-3). The side-change will be done after the WG and EG signals return to LOW (read state) by the side select latch in the control LSI.
The above delay operation is not executed only when the leading edge of the $\overline{\text{IDXO}}$ (INDEX) pulse is detected during the formatting of a disk, and the $\overline{\text{SSI}}$ input state is informed to the $\overline{\text{SSO}}$ output without significant delay time.

(4) DINV and DLEN input terminals

Terminals to select the designation method for high/normal density mode. These terminals are not used for this FDD and they are fixed to HIGH level.

(5) $\overline{\text{WPO}}$ output terminal

Terminal to output the WRITE PROTECT ($\overline{\text{WPO}}$) signal to the host controller. The $\overline{\text{WPO}}$ output goes to LOW when the FPT signal from the file protect sensor is LOW and when the DRIVE SELECT ($\overline{\text{DSEL}}$) input signal is TRUE (LOW).

(6) $\overline{\text{HD}}$ output terminal

Invert output terminal of the HD output. This terminal is not used for this FDD.

(7) TEST input terminal

This terminal is not used for this FDD.

(8) VCC and GND terminal

+5V and 0V power terminals.

2-2-3. Servo Circuit

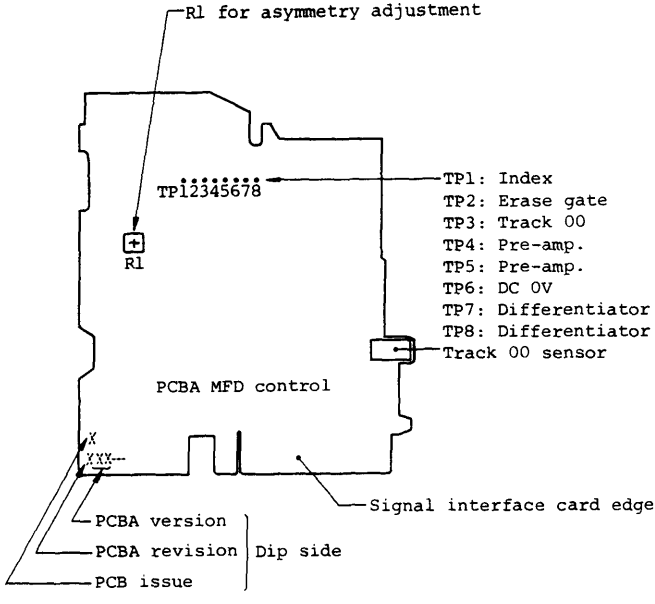
The DD motor Ass'y (spindle motor) of this FDD has two rotational speeds which are 300rpm for B and F models and 360rpm for G model. The speed is designated by $\overline{HSPD}$ input signal (J7-5) from the PCBA MFD control. When the $\overline{HSPD}$ is HIGH, the speed is 300rpm while it is 360rpm when the $\overline{HSPD}$ is LOW. Start/stop of the rotation is controlled by the MC signal supplied through the motor-on gate in the control LSI.

The servo circuit aims to maintain the rotational speed of the spindle motor at a determined constant speed, and the circuit is mounted on the PCBA assembled with the spindle motor.
The spindle motor is a long life DC brushless motor having 3-phase coils and bi-polar drive system. The coils are driven by the exclusive servo IC. Energization and magnetized direction of the coils are controlled by the signal from the hall elements mounted on the servo PCBA around the rotor so that they are changed corresponding to the designated rotational direction.
The rotational speed is maintained stably and precisely. The feedback signal from the frequency generator (FG) printed around the rotor is converted into the drive voltage (F-V conversion) by servo IC, and supplied to the drive coils through the phase compensation circuit

Several manufacturers' spindle motors are used in FD-55R series for the stable supply of the motor. Though these motors are the same in function and performance, they are different in external view.

2-3. FUNCTION OF TEST POINTS AND VARIABLE RESISTORS

Following shows the mounting position of the test points and variable resistors.



(Fig.213) Location of test points and variable resistors

2-3-1. Function of Test Points

Eight test points (one for DC 0V) are equipped on the PCBA MFD control for the check and adjustment of the waveforms of the FDD.

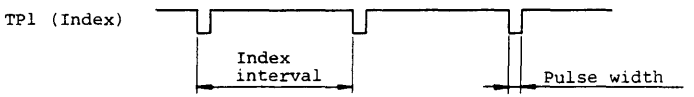
(1) TP1 (Index)

Test point to observe the output of the index sensor (photo-transistor). When the index hole is detected, negative going pulse is observed. The photo-transistor is mounted on the PCBA front OPT and the LED is mounted on the DD motor Ass'y (spindle motor).

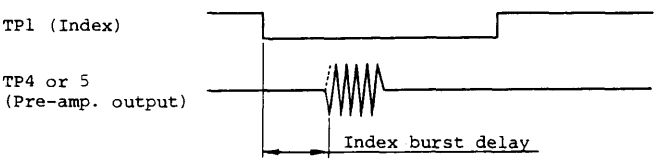
TP1 is used for the following purposes.

(a) Confirmation of the disk rotational speed.

(b) Rough confirmation and adjustment of the index burst detection timing. Burst timing is adjusted by the fixing screws of the PCBA front OPT. (Use INDEX interface signal for precise confirmation and adjustment).



(Fig.214) Typical waveform of TP1 (Speed observation)



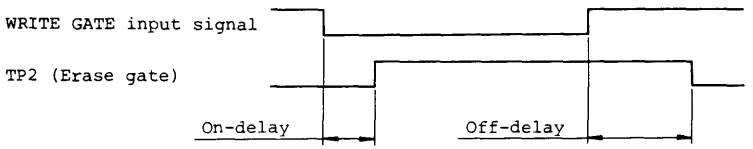
(Fig.215) Typical waveform of TP1
(Rough observation of burst timing)

Items	Models	
	B and F models	G model
Index interval	200 ± 3ms	166.7 ± 2.5ms
Pulse width	2 ∿ 5.5ms	1 ∿ 8ms
Index burst delay	200 ± 200μs	165 ± 165μs

(Table 208) Index timing

(2) TP2 (Erase gate)

Test point to observe the output of the erase gate.
When TP2 is HIGH level, erase current flows through the erase head.
This TP is used for the check of the required delay time of the erase gate signal against the WRITE GATE (WG) signal.



(Fig.216) Typical waveform of TP2

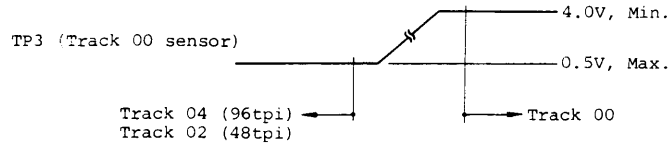
Delay	Models	
	B and F models	G model
On-delay	240 ∿ 290μs	200 ∿ 240μs
Off-delay	890 ∿ 990μs	530 ∿ 590μs

(Table 209) Erase gate delay

(3) TP3 (Track 00 sensor)

Test point to observe the output of the track 00 sensor (photo-interrupter).

The signal level at this TP is opposite in phase to that of the TRACK 00 ($\overline{T00}$) output signal. When the head is on track 00 or around track 00 position, TP3 goes to HIGH level.
The voltage of TP3 should be more than 4V at track 00 and less than 0.5V at track 04 (96tpi) or at track 02 (48tpi).



(Fig.217) Typical waveform of TP3

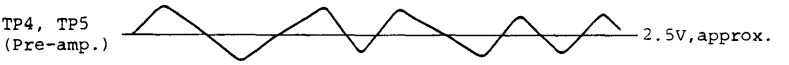
Notes: 1. The TRACK 00 output signal goes to TRUE (LOW level) only when the phase A (PA) coil of the stepping motor is energized and the direction latch is set to the step-out direction. Therefore, the level change timing of the TRACK 00 signal is not consistent with that of the TP3 signal.

2. Sense timing of the track 00 position will change if you loosen the fixing screws of the PCBA MFD control. This is because that the track 00 sensor is mounted on the PCBA. Be sure to readjust the track 00 sensor timing according to item 3-4-14.

(4) TP4, TP5 (Pre-amplifier)

Test point to observe the read pre-amplifier output signals.
The pre-amplifier has two outputs of the order of several dozen to several hundred mVp-p, and they differ in phase by 180° (opposite phase). Both outputs are observed at TP4 and TP5 respectively. For an accurate observation of the read waveforms, use two channels of an oscilloscope with one channel set to Invert mode and Add both channels. Use TP6 (0V) test point for the oscilloscope ground.

TP4 and TP5 are used for checking various characteristics of the read/write head and also for the check and adjustment of the head seek mechanism such as track alignment.

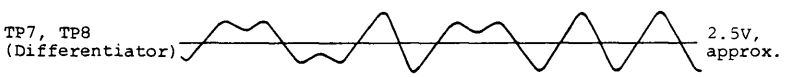


(Fig.218) Typical waveform of TP4 and TP5

(5) TP7, TP8 (Differentiation amplifier)

Test points to observe the differentiation amplifier output signals. Like the pre-amplifier, the differentiation amplifier also has two outputs of the order of several hundred mVp-p to several Vp-p which differ in phase by 180°. Both outputs are observed at TP7 and TP8 respectively.
For an accurate observation of the waveforms, use two channels of the oscilloscope with one channel set to Invert mode and Add both channels. Use TP6 (0V) test point for the oscilloscope ground.

TP7 and TP8 are used for checking the total operation of the read/write head and the read amplifier and for the check and adjustment of the head seek mechanism such as track alignment.



(Fig.219) Typical waveform of TP7 and TP8

(6) TP6 (0V)

It is used as the ground terminal for measurement equipment. Be sure

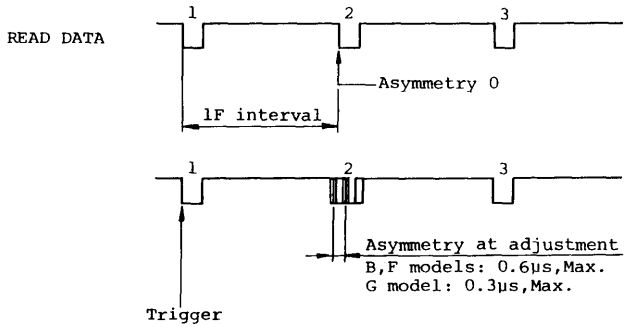
to use a small size clip to obtain a probe ground of the equipment.

2-3-2. Function of Variable Resistor

This item is applied only for a model with variable resistor on the PCBA MFD control.
The variable resistor is correctly adjusted before the shipment of the FDD and fundamentally it shall not be readjusted except for by a trained technician.

(1) R1 (for asymmetry adjustment)

Variable resistor for adjusting the asymmetry of the read data pulse. Write and read 1F data and observe the pulse intervals at the READ DATA output line. Then adjust the variable resistor so that the read data asymmetry takes the minimum value in Fig.220. Repeat each adjustment alternately for side 0 and side 1 heads to obtain the minimum asymmetry for both sides. Refer to item 3-4-9.



Note: When the READ DATA waveform is observed at the DOUT terminal of the SKA, positive going pulse is observed.

(Fig.220) Read data asymmetry

TEAC FD-55BR-521

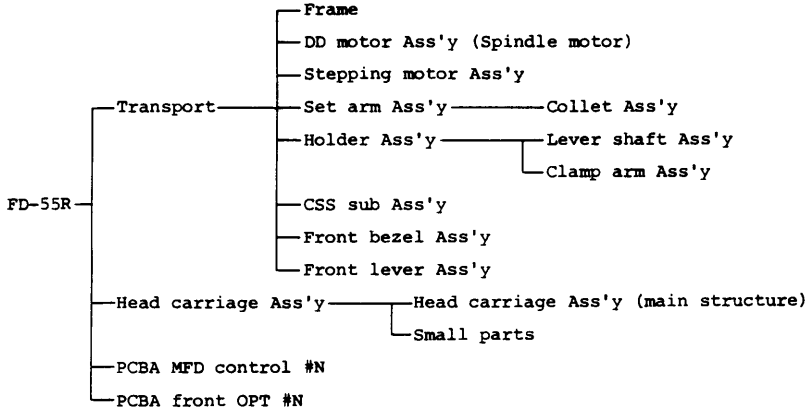
DRAWINGS & PARTS LIST

REV.A

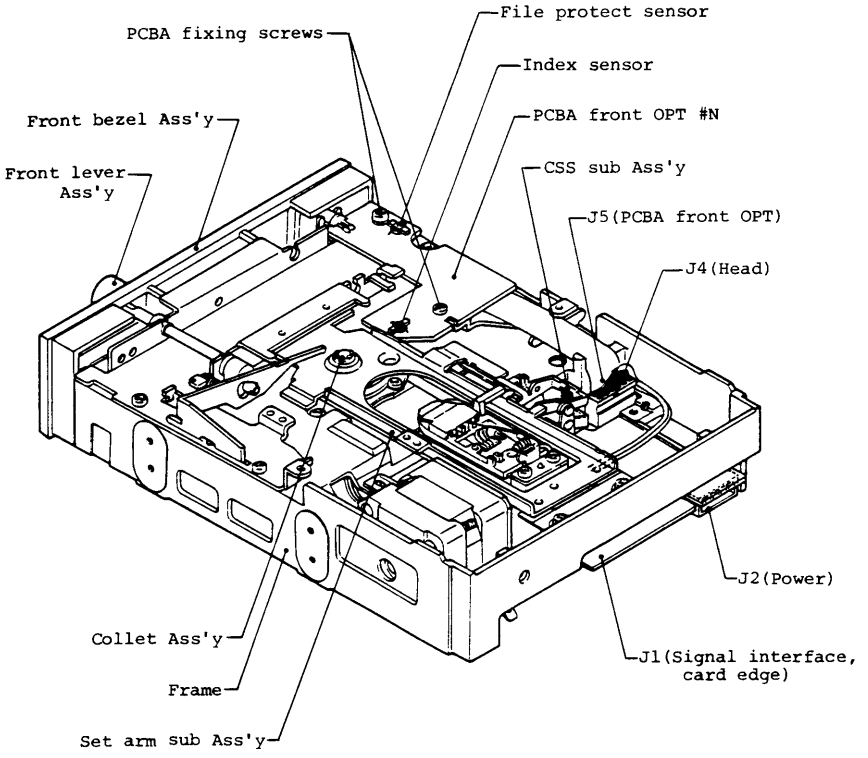
TABLE OF CONTENTS

4-1. CONFIGURATION

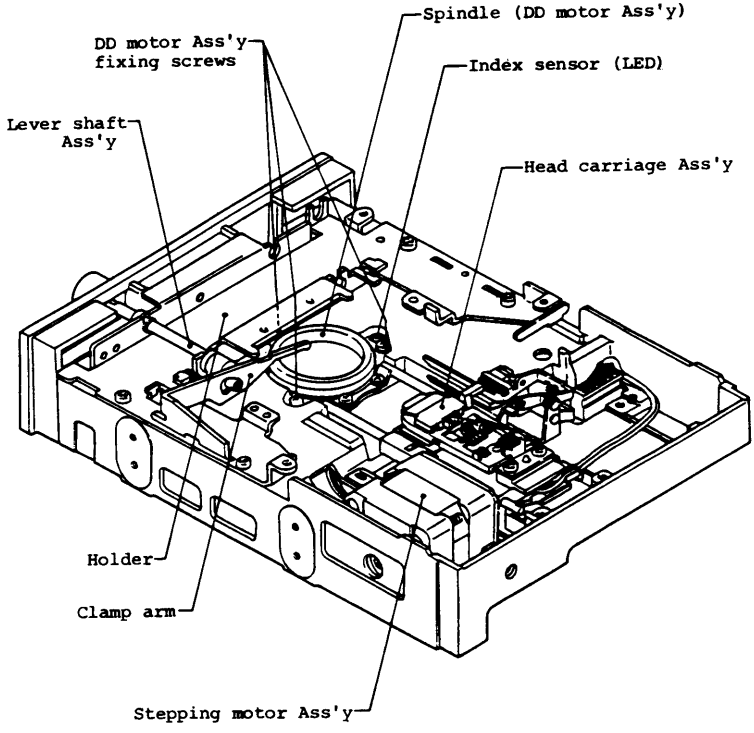
Following shows the configuration of the main parts of FD-55R series. (Refer to Fig.401 ∿ Fig.404). Refer to items 4-2 and 4-3 as to detailed break-down.



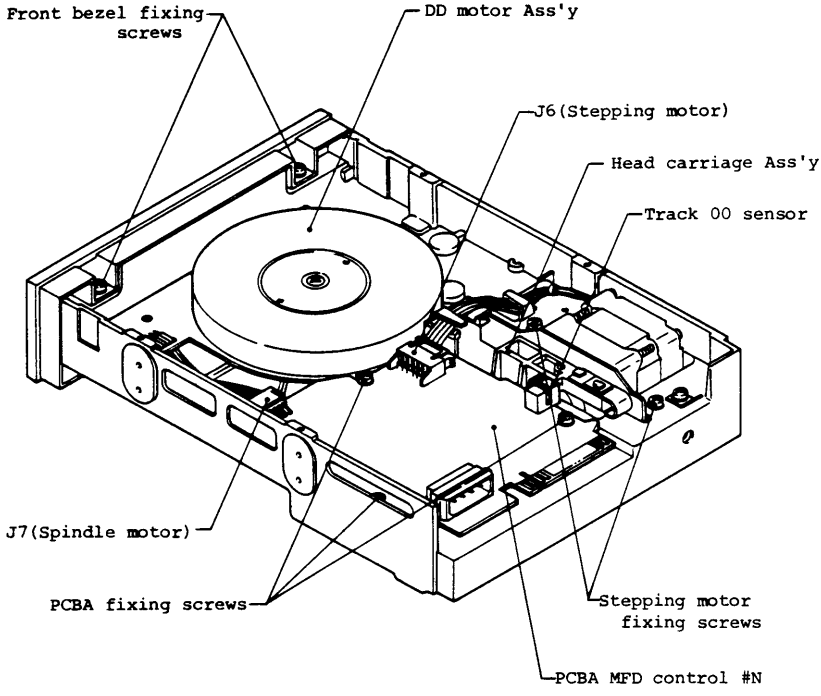
(Table 401) Main parts configuration of FD-55R series



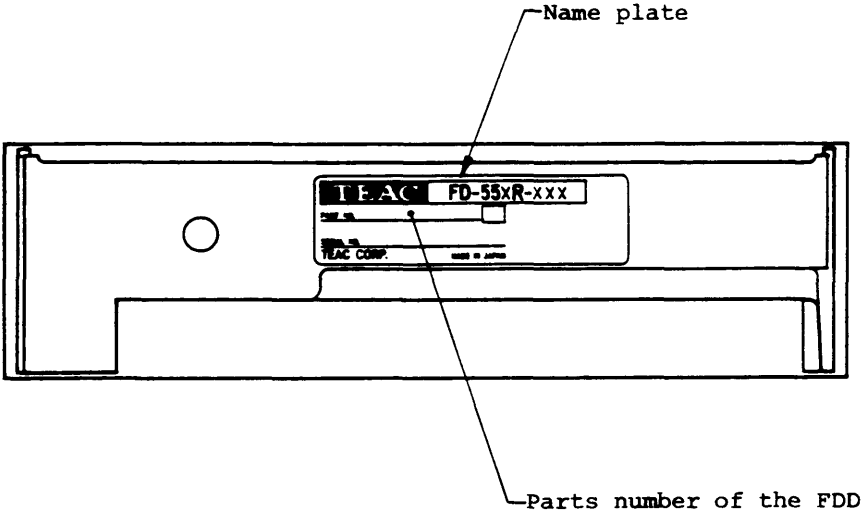
(Fig.401) External view (No.1)



(Fig.402) External view (No.2)



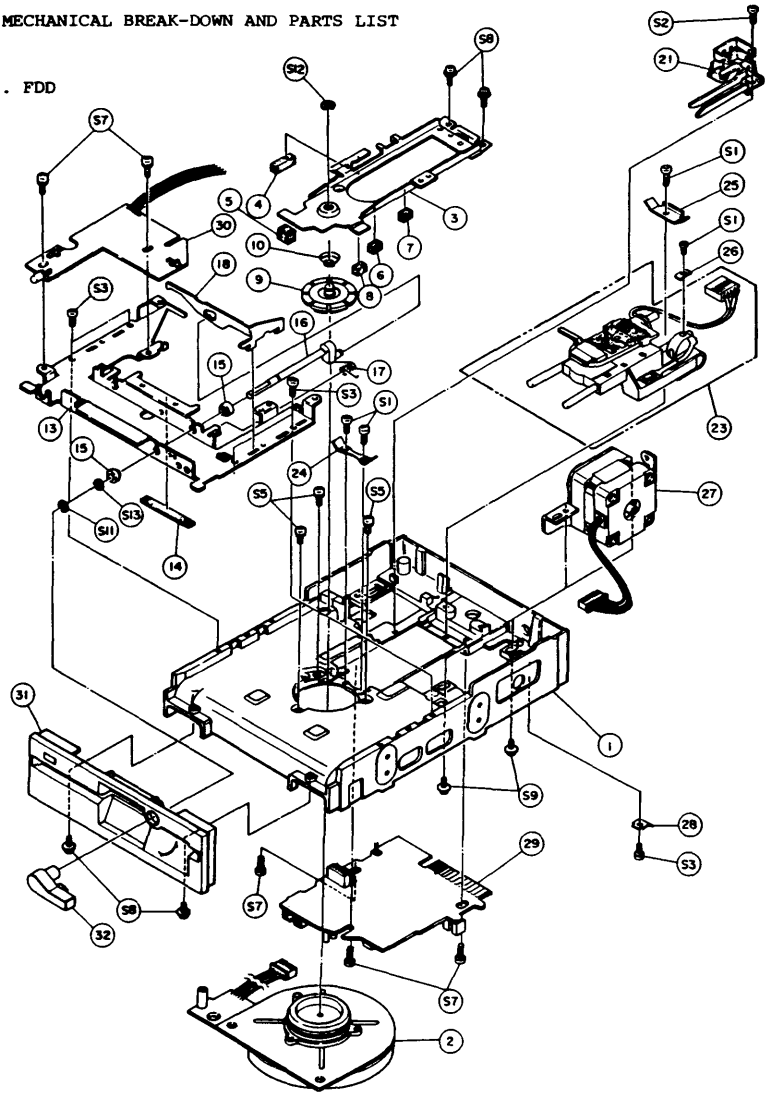
(Fig.403) External view (No.3)



(Fig.404) External view (No.4)

4-2. MECHANICAL BREAK-DOWN AND PARTS LIST

4-2-1. FDD



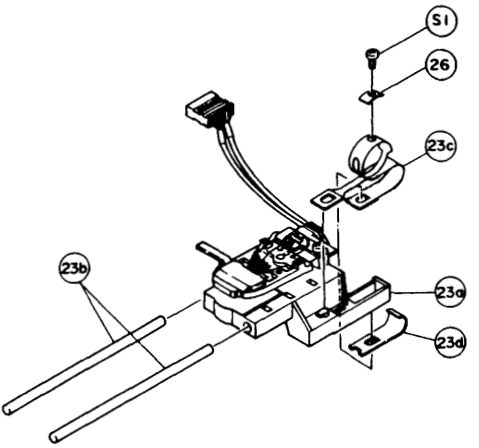
(Fig.405) Mechanical section break-down

Nos.	Parts Nos.	Parts name and ratings	Q'ty	Description
1	16153377 - 00	Frame	1	
2	14733730 - 70	DD motor Ass'y	1	
3	17967259 - 60	Set arm sub Ass'y	1	
4	16786997 - 03	Disk pad	1	
5	16787624 - 00	Pressure pad	1	
6	16787540 - 00	Touch pad	1	
7	16787076 - 06	Pad disk	1	For adjustment
8	16787944 - 00	Pad	1	For adjustment
9	17967272 - 00	Collet Ass'y	1	
10	16385299 - 00	Pressure spring B	1	
13	16803479 - 00	Holder	1	
14	16787501 - 00	Holder cushion	1	
15	16787500 - 00	Bush	2	
16	17967258 - 00	Lever shaft Ass'y	1	
17	16389068 - 00	Lever spring	1	
18	16786856 - 50	Clamp arm	1	
21	17967309 - 00	CSS Sub Ass'y	1	
23	17967603 - 00	Head carriage Ass'y BR	1	
24	16392009 - 00	Spring guide A	1	
25	16392045 - 00	Spring guide B	1	
26	16496492 - 00	Plate washer	1	
27	14769070 - 80	Stepping motor Ass'y	1	
	14769070 - 60	Stepping motor Ass'y	1	Second source
29	15532097 - 02	PCBA MFD control #N	1	
30	15532091 - 00	PCBA front OPT #N	1	
31	17967267 - 68	Front bezel Ass'y	1	
32	17967261 - 68	Front lever Ass'y	1	

(Table 402) Parts list of the FDD

Note: Head carriage Ass'y can be broken-down to the parts level shown in Table 402-C. However, order the maintenance parts as an parts number in Table 402 including small parts. This is because that the head carriage and two guide shafts are supplied in a pair for the matched hole combination. Two guide shafts are placed into the carriage holes at the shipment and the shafts are selected for each hole. Be sure not to ignore the combiantion when you use them.

SPARE PAGE



Nos.	Parts Nos.	Parts name	Q'ty	Description
23a	17987584 - 00	Head carriage Ass'y (Main structure)	1	
23b	16766577 - XX	Guide shaft	2	
23c	16792349 - 00	Steel belt	1	
23d	16392054 - 00	Belt spring	1	
23e	10902256 - 00	Shipping box	1	

(Table 402-C) Parts list of head carriage Ass'y BR

4-2-2. Screws and Washers

Nos.	Parts Nos.	Parts name and ratings	Description
S 1	16400304	Screw,pan 3*4 S ZMC	
S 2	16400305	Screw,pan 3*5 S ZMC	
S 3	16400306	Screw,pan 3*6 S ZMC	
S 5	16470308	Screw,pan,sems 3*8 S ZMC	
S 7	16498899	Screw,pan,flat 3*6 S ZMC	
S 8	16475308	Screw,pan,flat 3*8 S ZMC	
S 9	16499237-00	Screw,pan,three pieces 3*8 S ZMC	
S 11	16351140	E-ring 3J	
S 12	16351160	E-ring 4J	
S 13	16496060-00	Mylar washer 0.1T*4.1*8	For adjustment
	16496061-00	Mylar washer 0.2T*4.1*8	For adjustment
	16496061-01	Mylar washer 0.25T*4.1*8	For adjustment
	16496618-00	Nylon washer 0.3T*4.1*8	For adjustment
	16496062-00	Mylar washer 0.35T*4.1*8	For adjustment
	16496818-01	Nylon washer 0.4T*4.1*8	For adjustment

(Table 403) Parts list of screws & washers

4-3. PCBA PARTS LIST

Following shows the parts list of PCBAs.

Notes for Table:

1. "REV" (PCBA Revision No.) in the Description column indicates that the parts has been revised in the past. The revision number is indicated on the PCB in one or two alphabets following the PCBA version number. The earlier the character in the alphabets is, the older the revision of the assembly.

2. The newest assembly parts have "∿" mark after the "REV". Parts with old revision number are used only in that revision.

3. In Tables having plural PCBA versions, parts with PCBA version in the Description column are exclusive parts for the version, while parts without PCBA version are common parts.

4-3-1. PCBA MFD Control #N (P/N 15532097-02)

Nos.	Parts Nos.	Parts name and ratings	Description
U 1	13442777-01	IC IR4N09A	
U 2	13442429-00	IC BA6581CK	
U 3	13428129	Transistor array M54534P	
Q 3	13421244	Transistor 2SA881Q, R	
PQ 1	13419352	Photo-interrupter GP1S55	
	13419323	Photo-interrupter TLP809	Second source
CR 2	13411388	Diode 1SS138	
CR 3	13040377	Jumper wire JPW-01	
CR 4	13040377	Jumper wire JPW-01	
CR 5	13040377	Jumper wire JPW-01	
CRA1	13411398	Diode pair (K) 1SS233F	
	13411409	Diode pair (K) MC921	Second source
RA 1	13498981	Resistor array 8-1K ohms J	
RA 2	13498286-00	Resistor array T-9268	

(Table 404) PCBA MFD control #N parts list (1/5)

Nos.	Parts Nos.	Parts name and ratings	Description
RA 3	13499186-00	Resistor array T-9186	
R 3	11186183	Resistor RD 1/5W 18K ohms J	
R 5	11186183	Resistor RD 1/5W 18K ohms J	
R 6	11982968	Resistor RN 1/4W 2.80K ohms F	
R 8	11186222	Resistor RD 1/5W 2.2K ohms J	
R 9	11050121	Resistor RN 1W 120 ohms J	
	11985065	Resistor RN 1W 120 ohms J	Second source
R 10	11186223	Resistor RD 1/5W 22K ohms J	
R 12	11186472	Resistor RD 1/5W 4.7K ohms J	
R 13	11186159	Resistor RD 1/5W 1.5 ohms J	
R 14	11186151	Resistor RD 1/5W 150 ohms J	
R 15	11186151	Resistor RD 1/5W 150 ohms J	
R 16	11186223	Resistor RD 1/5W 22K ohms J	
R 17	11186223	Resistor RD 1/5W 22K ohms J	
R 18	11186391	Resistor RD 1/5W 390 ohms J	
R 19	11982848	Resistor RN 1/4W 165 ohms F	
R 20	11186222	Resistor RD 1/5W 2.2K ohms J	
R 21	11170101	Resistor RD 1/2W 100 ohms J	
R 22	11170101	Resistor RD 1/2W 100 ohms J	
R 23	11186563	Resistor RD 1/5W 56K ohms J	

(Table 404) PCBA MFD control #N parts list (2/5)

Nos.	Parts Nos.	Parts name and ratings	Description
R 25	13040377	Jumper wire JPW-01	
C 2	12907080	Capacitor CE 25V 33μF M	
C 4	12907078	Capacitor CE 10V 100μF M	
C 5	12907113	Capacitor CC 25V 0.022μF Z	
C 6	12907053	Capacitor CE 10V 22μF M	
C 7	12907113	Capacitor CC 25V 0.022μF Z	
C 9	12907096	Capacitor CC 50V 470PF J	
C 10	12907096	Capacitor CC 50V 470PF J	
C 11	12907648	Capacitor CC 12V 0.1μF M	
C 12	12907104	Capacitor CC 16V 2200PF K	
C 13	12907648	Capacitor CC 12V 0.1μF M	
C 14	12907104	Capacitor CC 16V 2200PF K	
C 15	12907104	Capacitor CC 16V 2200PF K	
C 16	12467222	Capacitor CQ 50V 2200PF G	
C 18	12467152	Capacitor CQ 50V 1500PF G	
C 19	12907061	Capacitor CE 50V 0.22μF M	
C 20	12907113	Capacitor CC 25V 0.022μF Z	
C 21	12907113	Capacitor CC 25V 0.022μF Z	

(Table 404) PCBA MFD control #N parts list (3/5)

Nos.	Parts Nos.	Parts name and ratings	Description
C 22	12907113	Capacitor CC 25V 0.022μF Z	
C 23	12907091	Capacitor CC 50V 180PF J	
C 24	12907088	Capacitor CC 50V 100PF J	
C 25	12467101	Capacitor CQ 50V 100PF G	
C 28	12906659	Capacitor CE 50V 6.8μF V	
C 29	12906659	Capacitor CE 50V 6.8μF V	
C 30	12907113	Capacitor CC 25V 0.022μF Z	
C 31	12907113	Capacitor CC 25V 0.022μF Z	
C 32	12907113	Capacitor CC 25V 0.022μF Z	
L 1	11984508	Resistor 0 ohm	
L 2	11984508	Resistor 0 ohm	
L 3	14723692	Coil chalk 330μH J	
L 4	14723692	Coil chalk 330μH J	
L 5	14723692	Coil chalk 330μH J	
Y 1	13295084-00	Ceramic oscillator KBR-480	
J 2	13121916	Connector 4P	
J 4	13121235	Connector W12P polarizing	
J 5	13123219	Connector 5P	

(Table 404) PCBA MFD control #N parts list (4/5)

Nos.	Parts Nos.	Parts name and ratings	Description
J 6	13121191	Connector 6P	
J 7	13123257	Connector 5P	
U1	11984508	Resistor 0 ohm	
D0, D1	13189406	4-Post pins	Unreplaceable
ML, RY	13189406	4-Post pins	
IU	11984508	Resistor 0 ohm	
TP1~TP8	13189406	8-Post pins	Unreplaceable
	13122427	Short bar	(For shorting the straps)

(Table 404) PCBA MFD control #N parts list (5/5)

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4-3-2. PCBA Front OPT #N (P/N 15532091-00)

Nos.	Parts Nos.	Parts name and ratings	Description
PQ51	13419060	Phot transistor	
PQ52	13419060	Phot transistor	
LED51	13419261-00	Lead-formed LED GL-5HD5	RED
R51	11186151	Resistor RD 1/5W 150 ohms J	
	13040460	Jumper wire 5 lines 77mm	
	16787503-00	Index holder	(For PQ51)
	16787502-00	Sensor holder	(For PQ52)

(Table 405) PCBA Front OPT #N parts list

4-4. PARTS LOCATION AND SCHEMATIC DIAGRAMS

Notes:

1. One of three types (Type S, K, and G) of DD motor Ass'y are used for the FDD. These three types have compatibility with no relation to revision number.

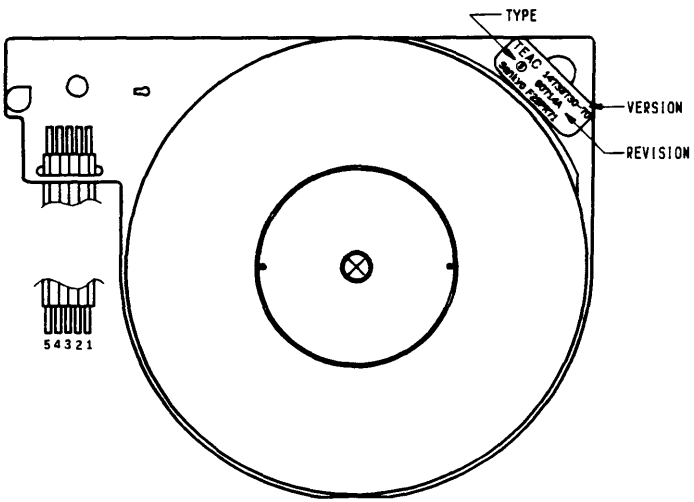
2. For Schematic diagram, parts with an asterisk (*) are different in each PCBA version. Refer to VERSION TABLE.
   If the parts with an asterisk (*) are not listed in the corresponding column of the VERSION TABLE, it means that they are not used in that PCBA version.

3. Resistor (R) and resistor array (RA) values are in Ohms, 1/8W or larger, ±5%(J), unless otherwise specified.

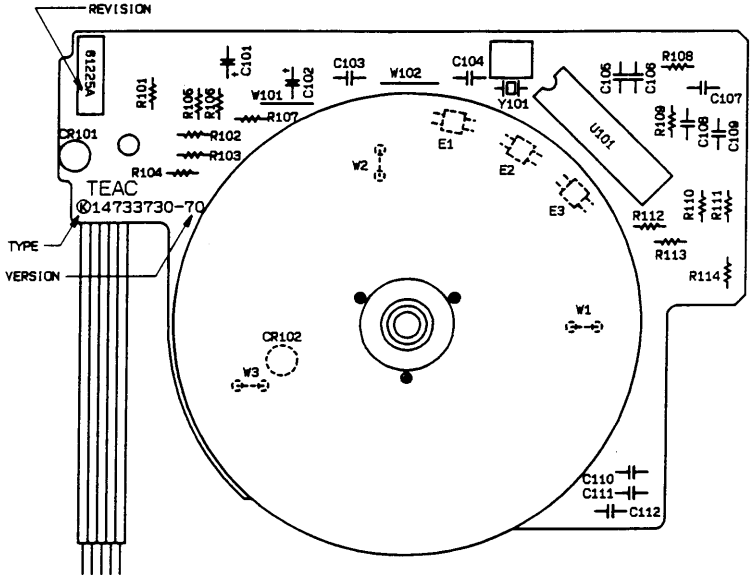
4. Capacitor (C) values are in Microfarads, 50V or higher, ±10%(K), unless otherwise specified.

5. Tolerance symbols for R, RA, and C are:
   F: ±1% G: ±2% J: ±5% K: ±10%
   V: +20-10% M: ±20% Z: +80-20%

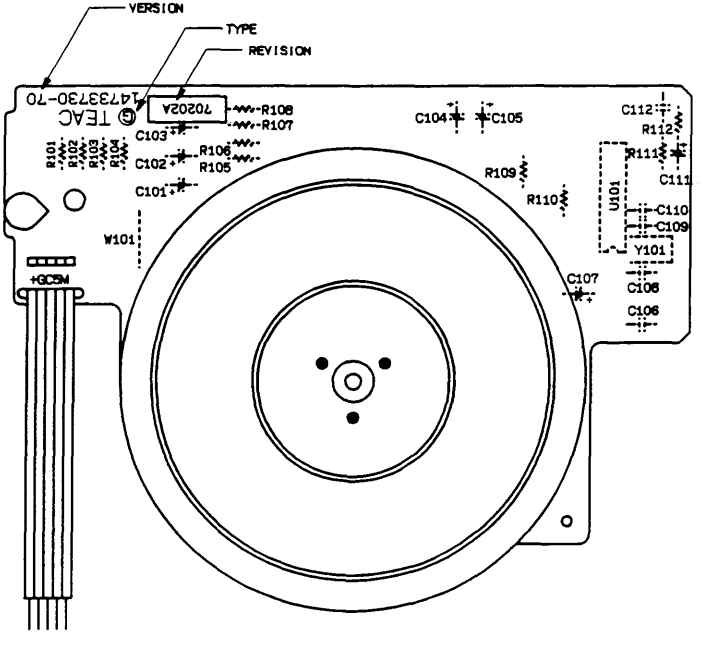
PCBA DD MOTOR SERVO, PARTS LOCATION (Type S)



PCBA DD MOTOR SERVO, PARTS LOCATION (Type K)



PCBA DD MOTOR SERVO, PARTS LOCATION (Type G)



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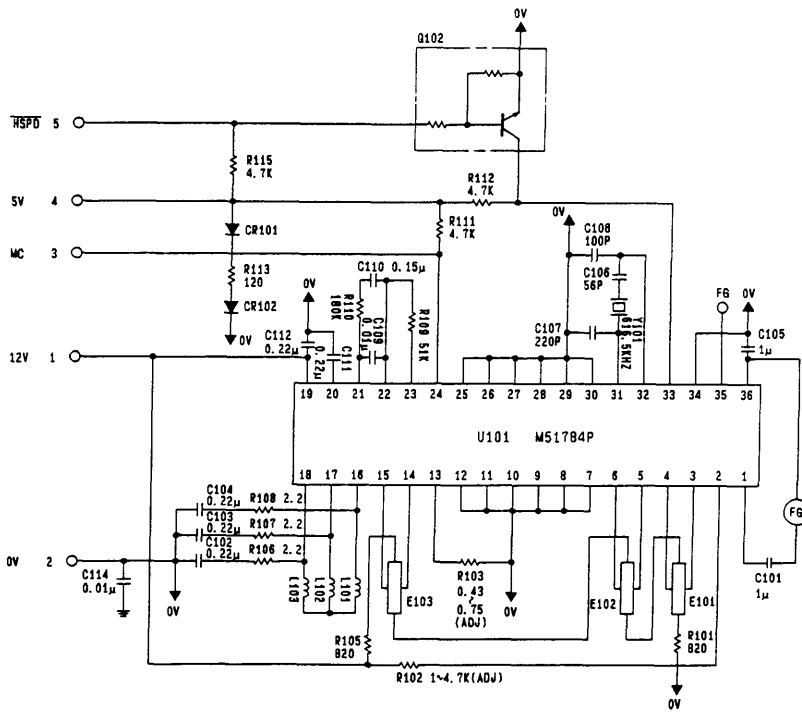
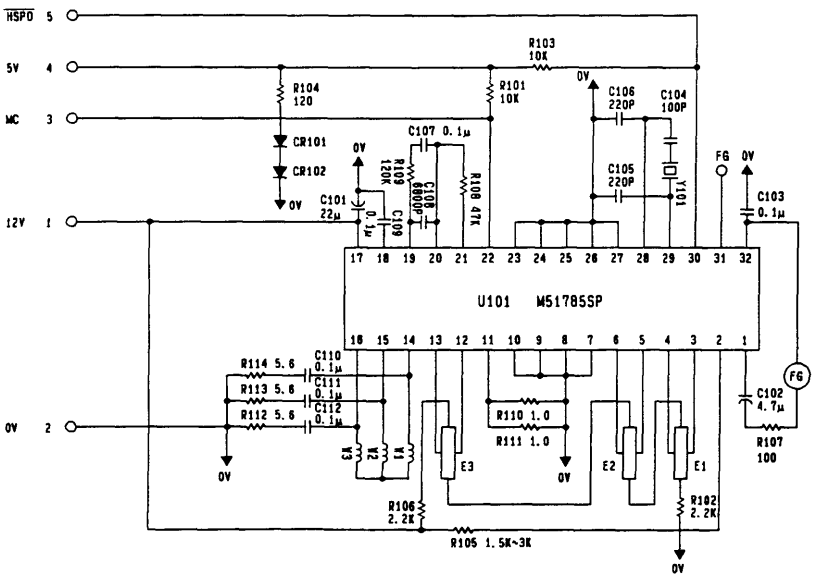
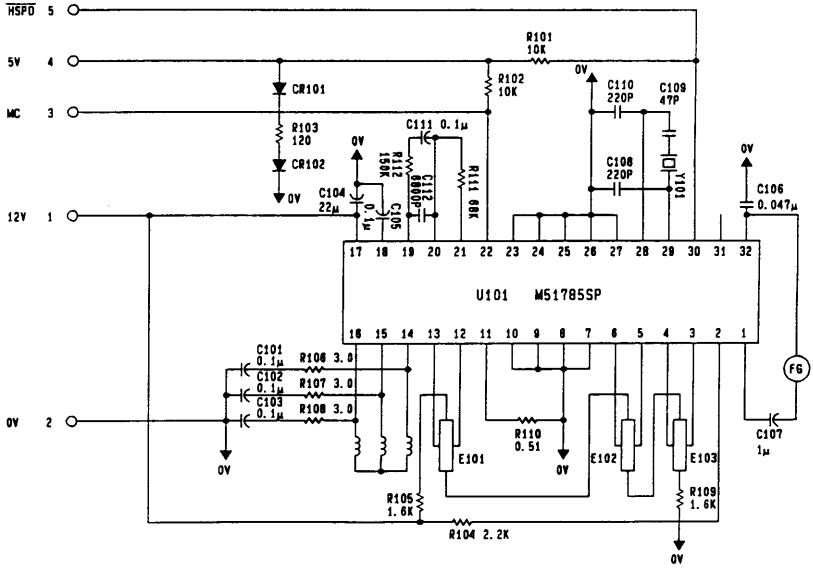
PCBA DD MOTOR SERVO, SCHEMATIC (Type S)



PCBA DD MOTOR SERVO, SCHEMATIC (Type K)



PCBA DD MOTOR SERVO, SCHEMATIC (Type G)



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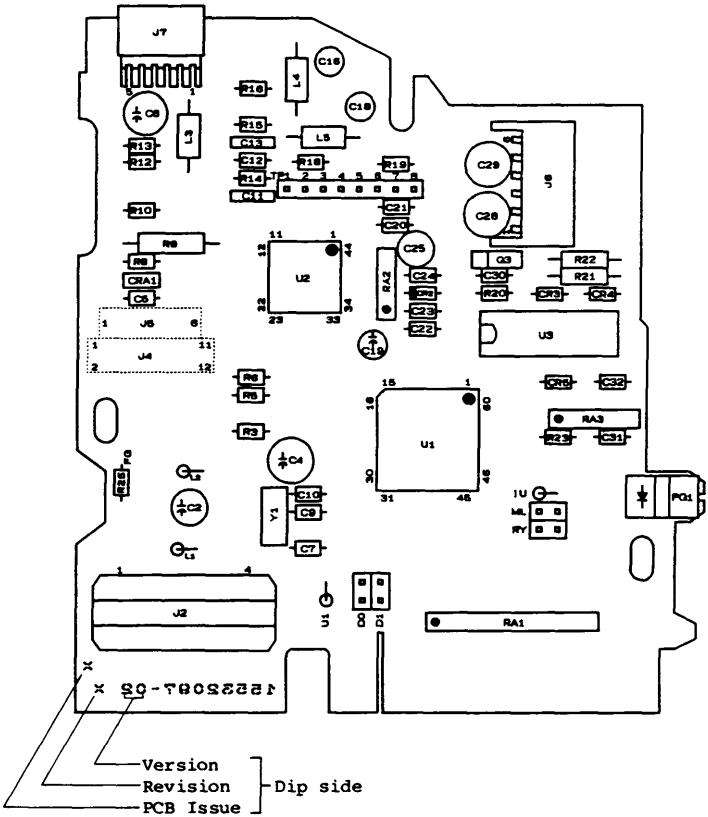
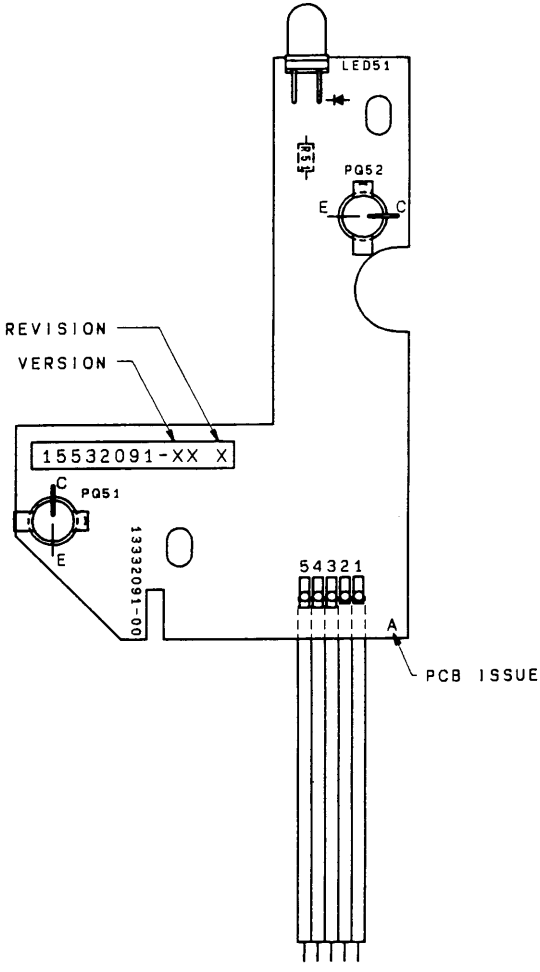
PCBA MFD CONTROL #N, PARTS LOCATION



PCBA FRONT OPT #N, PARTS LOCATION



SECTION 3

MAINTENANCE

3-1. GENERAL

3-1-1. Periodic Maintenance

The FDD is designed to be free from periodic maintenance for 5 years such as replacement of parts, grease-up, etc. when it is operated at a normal operation duty.
However, cleaning of the magnetic head is recommended using a cleaning disk since it may be effective to improve the reliability of data.
If some of the parts in the FDD are operated at a specially heavy duty, or if the FDD is operated over 5 years, it is recommended to replace the wear parts according to Table in item 4-5. Replacement of parts should be executed according to item 3-5 referring to precautions in item 3-2.

Periodic maintenance items	Recommended cycle	Required time
Cleaning of magnetic head	Refer to item 3-3.	5 minutes
Replacement of wear parts	Refer to items 4-5 and 3-5.	

(Table 3101) Periodic maintenance items

3-1-2. Check and Adjustment

Table 3102 shows all of the check and adjustment items. These items do not require periodic maintenance. Check and adjustment should be done when required during replacement of the maintenance parts or during trouble shooting referring to items 3-2 and 3-4.
The numbered procedure in Table 3102 shows a typical procedure of the general check and adjustment all over the FDD. After the mechanical items of steps 1 ∿ 4, electric performance items of steps 5 ∿ 15 should be done.

Steps	Check and adjustment items	Required time	Referred items
1	Adjustment of set arm position	3 minutes	3-4-1
2	Check and adjustment of holder position	5 minutes	3-4-2
3	Check and adjustment of arm lifter (Model with head load solenoid)	5 minutes	3-4-3
4	Check of CSS Ass'y (CSS model)	3 minutes	3-4-4
5	Check of file protect sensor	3 minutes	3-4-5
6	Check of disk rotational speed	3 minutes	3-4-6
7	Check of erase gate delay	3 minutes	3-4-7
8	Check of head touch	3 minutes	3-4-8
9	Check of asymmetry	3 minutes	3-4-9
10	Check of read level	3 minutes	3-4-10
11	Check of resolution	3 minutes	3-4-11
12	Check and adjustment of track alignment	10 minutes	3-4-12
13	Check and adjustment of track 00 sensor	5 minutes	3-4-13
14	Check of track 00 stopper	3 minutes	3-4-14
15	Check and adjustment of index burst timing	5 minutes	3-4-15

(Table 3102) Check and adjustment items

3-1-3. Maintenance Jigs and Tools

The following are the jigs and tools required for adequate maintenance of the FDD.

3-1-3-1. Equipments

(A) When conventional Simulator KA (abbreviated to SKA) is used:

(1) SKA

SKA model	Applied FDD model
SKA-A~F	FD-55BR/FR
SKA-G (or SKA-GFII, G mode)	FD-55GR

(Table 3103) Conventional SKA model and applied FDD

Notes: 1. All SKAs are generally called as SKA in the following explanation unless otherwise designated.
2. SKAs in Table 3103 can be used also for all the conventional FD-55 series.

(2) Accessories for SKA

SKA needs the following accessories for operating the FD-55R series. The following accessories are common for all the 55R series except for special models.

(a) SKA/FDD interface cable #0, P/N 15922337-00
(b) Check cable #5, P/N 15922611-00
Check cable #5 includes SKA/FDD power cable.

(3) Oscilloscope (two channels)

(4) DC power supply

(a) Commercially available DC power supply or any of the following TEAC power unit can be used.
TEAC power unit: PS-II, PS3, or PS3-MINI

(b) Minimum required current for SKA operation.
+12V: 0.2A (for SKA) + α(for FDD)
+5V: 1.2A (for SKA) + α(for FDD)

(c) Required accessory: PS/SKA power cable

(5) Thermometer and hygrometer

(B) When Simulator KA3 (abbreviated to SKA3) is used:

Notes: 1. Conventional SKAs and SKA3 are generally called as SKA in the following explanation unless otherwise designated.

2. SKA3 basically functions like as a conventional SKA and it is improved in many points when compared.
Also the SKA3 can be applied to all FDD models including 3.5" FDDs supplied from TEAC by replacing a small cartridge for each FDD model.

(1) SKA3

The following Issue and Version shall be used for SKA3 itself and installed ROM.

(a) SKA3 hardware: Issue E or later
(b) ROM installed: Version V1.06 or later

Note: Issue and Version are shown on bottom plate of the SKA3.

(2) Accessories for SKA3

SKA3 needs the following accessories for operating the FD-55R series.

(a) Cartridge

Cartridge is constructed with small printed circuit board to select a function parameter of the SKA3 matching with a tested FDD. It shall be attached to rear side of the SKA3 before operation.
Table 3104 shows the selection of the cartridge.

(b) SKA/FDD interface cable #0, P/N 15922337-00
(c) SKA/FDD power cable, P/N 15922336-00
(d) Check cable #8, P/N 15922670-00

Name of cartridge	P/N	Applied model
PCBA cartridge #1, FD-55V AB	15532077-10	FD-55BR
PCBA cartridge #1, FD-55V EF	15532077-11	FD-55FR
PCBA cartridge #1, FD-55V G	15532077-12	FD-55GR

(Table 3104) Selection of SKA3 cartridge

(3) Oscilloscope (two channels)

(4) DC power supply

(a) Commercially available DC power supply or TEAC power unit (PS3 or PS3-MIN) can be used.

Note: TEAC power unit, PS-II cannot be applied for the SKA3 as a rule, because of small current capacity. If it is temporarily used, connect PSB output of the PS-II to the PSB input of the SKA3 and set the FD PWR switch to the PSB side.

(b) Minimum required current for SKA3 operation

+12V: 0.25A (for SKA3) + α(for FDD)
+5V: 2.0A (for SKA3) + α(for FDD)

(c) Required accessory: PS/SKA power cable.

(5) Thermometer and hygrometer

(C) When an SKA is not used:

(1) FDD controller and DC power supply (user's system)

(2) Oscilloscope (two channels)

(3) Frequency counter

(4) Digital voltmeter

(5) Thermometer and hygrometer

3-1-3-2. Tools, jigs, and disks

(1) Tools

(a) Cross-point screwdriver, M2.6 and M3
(b) Common screwdriver, small size
(c) Hexagon wrench key, 1.5mm
(d) A pair of tweezers
(e) Round nose pliers
(f) Cutting pliers
(g) Cutter knife
(h) Solder and soldering iron
(i) Scale, small size

(2) Special jigs

(a) Max. media jig for adjustment (Jig.C, P/N 17890746-00)
(b) Max. media jig for check (Jig E, P/N 17890746-02)
(c) Alignment adjustment jig (P/N 17851100-00)

(3) Disks

(a) Work disk (commercially available disk)

i) For Normal density (FD-55BR/FR)
ii) For High density (FD-55GR)

(b) Double sided cleaning disk (commercially available, dry type)

(c) Level disk

i) For Normal density (FD-55BR/FR), P/N 14900015-00
ii) For High density (FD-55GR), P/N 14900015-01

Note: Commercially available disks may be used if there is no doubt.

(b) Alignment disk

i) For double sided, 48tpi (FD-55BR), P/N 14900016-21
ii) For double sided, 96tpi (FD-55FR), P/N 14900016-24
iii) For High density, double sided, 96tpi (FD-55GR), P/N 14900016-25

(4) Other articles used during maintenance

(a) Absolute alcohol (Ethanol)
(b) Cottom swab or gauze
(c) Locking paint (Three Bond, 1401B)
(d) Screws and washers (Refer to Table 403 in Parts List).
(e) Oil (Kanto Chemicals Co., FLOIL 946P, TEAC P/N 10854022)
(f) Grease (Kyodo Yushi, Co., Multemp P2B, TEAC P/N 10857031)

3-2. PRECAUTIONS

3-2-1. Torque Applied to Screws and Locking Paint

(1) The following torque should be applied to screws, unless otherwise specified.

Size of screws	Application	Torque
M3	For general usage	6Kg.cm
M3	Installation of steel belt and PCBA front OPT	4.5Kg.cm

(Table 3201) Torque applied to screws

(2) Apply fresh locking paint to the following designated points after tightening or adjusting the screw.

(a) Installation screws of stepping motor: M3, 2 points
(b) Adjustment screw of arm lifter
(Only for models with head load solenoid): M3 setscrew
(c) Steel belt and carriage: 4 points, refer to item 3-5-1.

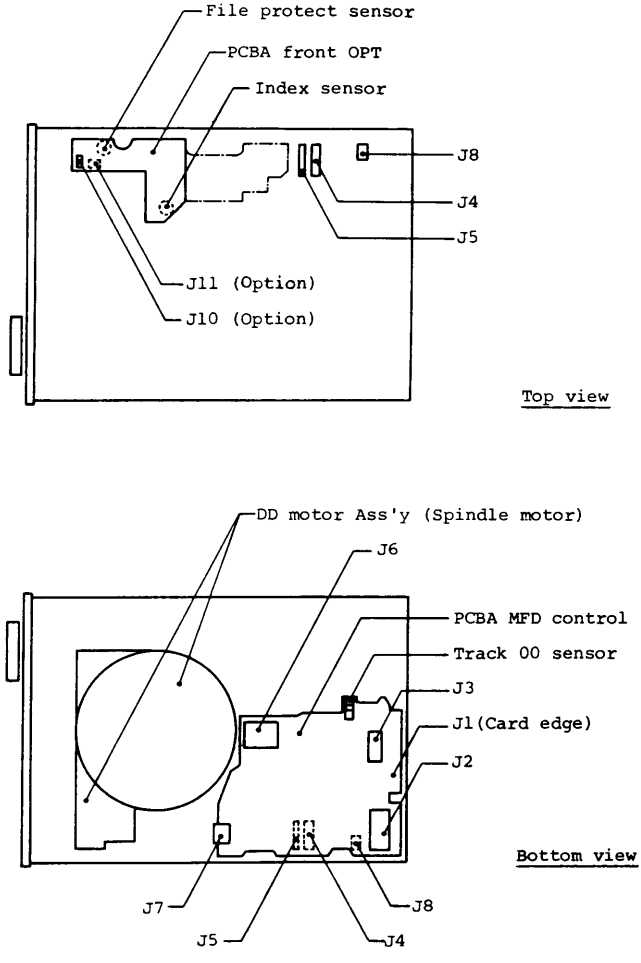
Note: Before applying a drop of locking paint, be sure to remove old locking paint on the screw and around it.

3-2-2. Handling of Connectors

3-2-2-1. Location of connectors

The following connectors are used in the FDD. Fig.3201 shows the location.

(a) J1: Interface connector
(b) J2: Power connector
(c) J3: IC socket for terminator network (only for full strap models)
(d) J4: Head connector
(e) J5: PCBA front OPT connector
(f) J6: Stepping motor connector
(g) J7: Spindle motor (DD motor Ass'y) connector
(h) J8: Head load solenoid (only for models with HL solenoid)
(i) J10: (Option, 1/1 size front bezel indicator connector)
(j) J11: (Option, Door close Ass'y or Door lock solenoid Ass'y connector)



(Fig.3201) Types of connectors

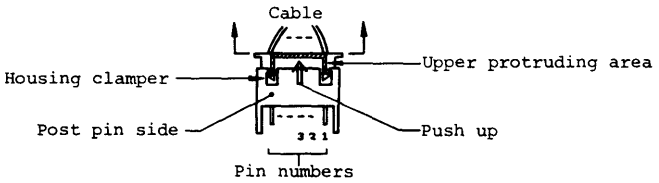
3-2-2-2. Connection and disconnection of the connectors

Be sure to turn the power off before connecting and disconnecting the connectors. Connection or disconnection should be done straightly and correctly without applying excessive force to the cables and the post pins.

3-2-2-3. Precautions for white connectors, J6 and J11

(1) Disconnection of the connector

As shown in Fig.3202, carefully push up the edges of the upper protruding area of the connector little by little with the finger nails or with a screwdriver.



(Fig.3202) Disconnection of J6 or J11

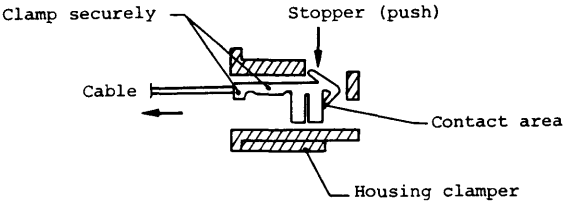
(2) Connection of the connector

Push the connector into the post pin on the PCBA with the housing clamper up.

(3) Removal of the pin (for reference)

Refer to Fig.3203.
Depressing the stopper of the pin lightly with a narrow object such as a pair of tweezers, pull the cable in the direction indicated by

the arrow mark.



(Fig.3203) Sectional view of J6 and J11

(4) Insertion of the pin (for reference)

Before insertion, check the following three points.

(a) Confirm that the sheath and the core of the cable are securely clamped.
(b) Confirm that the stopper is lifted as in Fig.3203 and it inhibits accidental removal.
(c) No tarnish or contamination adheres on the contact area of the pin or the PCB side post pin. If there is, remove it.

Contact failure may happen if any of these three points is not satisfied.
When you insert the pin, it shall be so inserted that the stopper faces the opening side of the housing.
After the insertion, check the connection by pulling the cable lightly.

3-2-2-4. Precautions for black connectors, J4 and J8

(1) Disconnection of the connector

Pull out slowly holding the housing with the fingers or a round nose

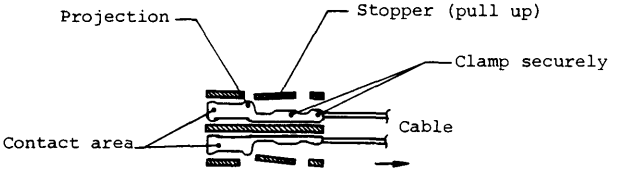
pliers. Be sure not to apply tension to the fine cable of J4 (head connector).

(2) Connection of the connector

Make the polarizing key position of the housing correspond with the lack of the post pin, and push the housing carefully with the fingers.

(3) Removal of the pin

Lifting up the stopper of the housing with a narrow object such as cutter knife, pull the cable with a pair of tweezers in the direction indicated by the arrow mark. Refer to Fig.3204.



(Fig.3204) Sectional view of black connectors

(4) Insertion of the pin

Before insertion, check the pins according to item 3-2-2-3 (4). When you insert the pin, it shall be so inserted that the projection side faces the stopper of the housing. After the insertion, pull the cable with a pair of tweezers softly in order to confirm whether it is securely connected.

3-2-2-5. Precautions for flat cable connector, J5 and J7

(1) J5 (PCBA front OPT connector)

(a) Disconnection of the connector

After disconnecting the adjacent connector, J4 according to item 3-2-2-4, pick up the flat cable with fingers and draw it out slowly.

(b) Connection of the connector

i) Confirm that the core wires of the tip of the flat cable are straight in parallel.

ii) Hold the flat cable with your right fingers and fit the core wires in line against the J5 receptacle on the soldered side of the PCBA MFD control.

iii) Guiding the cable with a tip of your left finger and push the cable into the receptacle securely.

iv) Confirm visually that the cores are not bent nor jut out.

(2) J7 (Spindle motor connector)

(a) Disconnection of the connector

i) Lift up the flat cable from the frame surface by fingers or by a pair of tweezers.

ii) Depressing the tip of the J7 housing (front bezel side) against the rear end of the FDD with your thumb and draw out the flat cable straightly. Be careful not to press the rotor of the spindle motor or electric parts on the PCBA.

(b) Connection of the connector

i) Confirm that the core wires of the tip of the flat cable are

straight in parallel.

ii) Hold the flat cable with fingers or with a pair of tweezers and fit the core wires in line against the J7 receptacle.

iii) Push the cable into the receptacle securely not to be bended nor folded.

iv) Depress the center area of the flat cable against the frame.

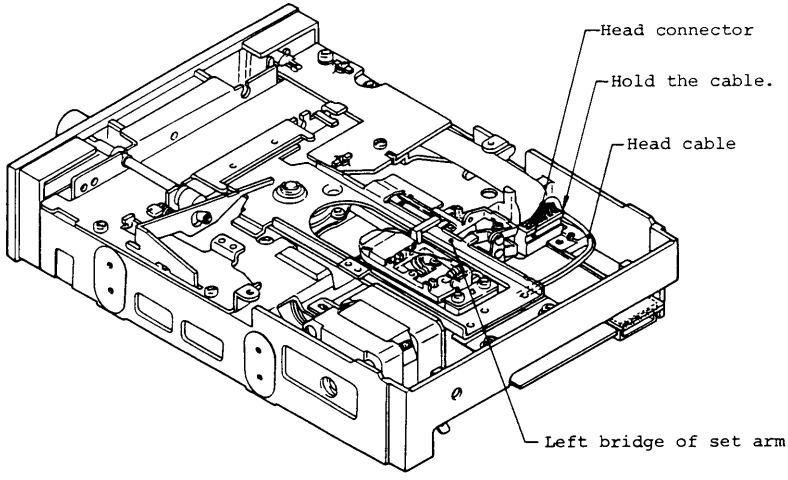
v) Confirm visually that the core wires are not bent nor jut out.

3-2-3. Head Cable Treatment

Head cable shall be arranged correctly so that the head carriage can move on the guide shafts smoothly.
When the FDD has head load solenoid Ass'y, remove the Ass'y referring to item 3-5-5 before the following steps.

(1) Pass the head cable under the left bridge of the set arm.

(2) Hold the head cable between the head connector and the frame so that the cable has appropriate space margin against the mechanical parts when the head carriage is set to the innermost track (front end of the moving area) and track 00 (rear end of the moving area). The head cable should run at a balanced position of moving area.



(Fig.3205) Head cable arrangement

3-2-4. Initial Setting of SKA

Following initial settings are required for operating an SKA. These settings are applied to all the SKA models unless otherwise specified.

3-2-4-1. Cable connection and setting of power supply voltage

(A) Convertional SKA (SKA-A∿F, SKA-G, SKA-GFII)

(1) Set the output voltage of DC power supply to +12V and +5V, approx.

(2) Turn the DC power off and connect the power cable to the PSA (SKA PWR) connector of the SKA.

(3) Set the FD PWR switch of the SKA to the OFF position.

(4) Connect the SKA/FDD interface cable. Pay attention to identification mark (▽) of the connector so that it locates at pin 1 side.

(5) Connect the FD PWR OUTPUT of the SKA and J2 of the FDD with the power line of the check cable #5.

(6) Connect the black connector (8P) of the check cable #5 to TP1 ∿ TP8 of the FDD. Be sure to connect so that the green wire comes to TP8 side.

(7) Connect the white connector with shielded wire of the check cable #5 to terminals 6 ∿ 9, G of the SKA. The shielded wires come to terminals 6 and 7 side of the SKA.

(8) Connect the white connector without shielded wire of the check cable #5 to terminals 1 ∿ 5 of the SKA. Green wire comes to terminal 1 of the SKA.

(9) Turn the DC power on. Set the FD PWR switch of the SKA to the PSA side.

(10) Key in "CB". (+5V VOLTAGE)

(11) Adjust the DC power voltage so that the DATA indicator of the SKA, XX.XX (V) indicates a value within the range of 5.00 ± 0.1V.

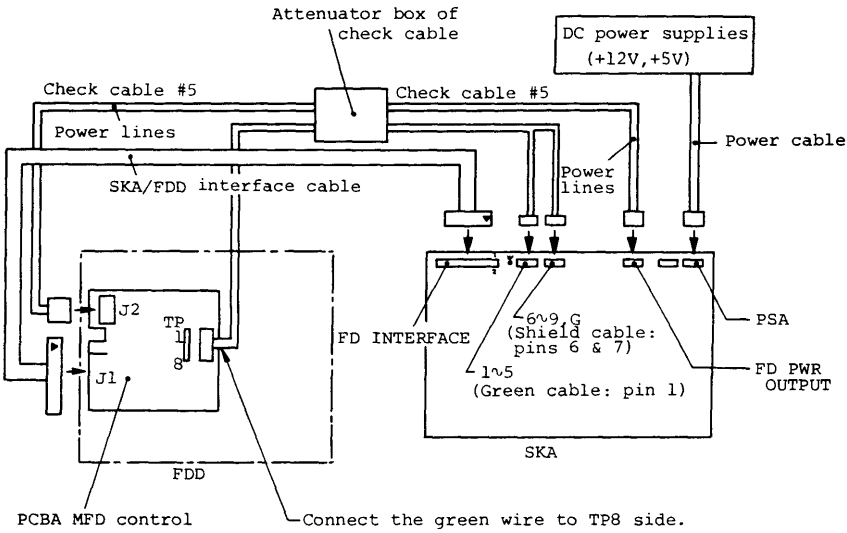
(12) Key in "F". (STEP)

(13) Key in "CC". (+12V VOLTAGE)

(14) Adjust the DC power voltage so that the DATA indicator, XX.XX (V) indicates a value within the range of 12.00 ± 0.24V.

(15) Key in "F". (STOP)

Note: The above items (1), (2), (7), (8), (10) ∿ (15) may be omitted for replacement or temporary power off of the FDD.
In this case, remain the DC power on for the SKA and control the FDD power by the FD PWR switch.



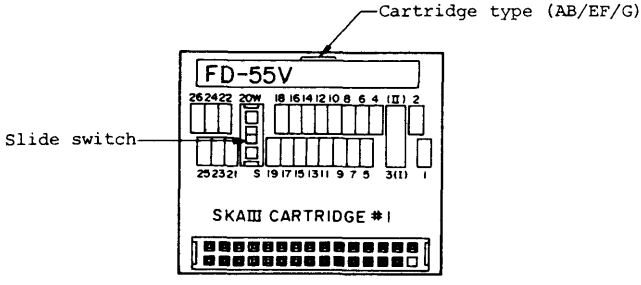
(Fig.3206) Connection of conventional SKA

(B) SKA3

(1) Attach an appropriate cartridge to the SKA3 referring to Table 3104. Pay attention to identification mark (▽) of the cartridge connector so that it matches with the mark of the SKA3.

(2) Set the slide switch mounted on the cartridge for FD-55BR or 55FR to "W" (upper) side. This means double sided operation by single SKA3 command.

Note: Cartridge for FD-55GR has no slide switch and "20" position of the cartridge is fixed to "W" side.



(Fig.3207) Cartridge setting for FD-55BR and FR

(3) Set the output voltage of DC power supply to +12V and +5V, approx.

(4) Turn the DC power off and connect the power cable to the PSA (SKA PWR) connector of the SKA3.

(5) Set the FD PWR switch of the SKA3 to the OFF position.

(6) Connect the SKA/FDD interface cable. Pay attention to identification mark (▽) of the connector so that it locates at pin 1 side.

(7) Connect the FD PWR OUTPUT of the SKA3 and J2 of the FDD with the SKA/FDD

power cable.

(8) Connect the black connector (8P) of the check cable to TP1 ∿ TP8 of the FDD. Be sure to connect so that the green wire comes to TP8 side.

(9) Connect the white connector with shielded wire of the check cable to terminals 6 ∿ 9, G of the SKA3. The shielded wires come to terminals 6 and 7 side of the SKA3.

(10) Connect the white connector without shielded wire of the check cable to terminals 1 ∿ 5 of the SKA3. Green wire comes to terminal 1 of the SKA3.

(11) Turn the DC power on and push the RESET switch at the rear side of the SKA3. The contents of the cartridge parameter are read into the SKA3.

Note: Be sure to push the RESET switch when a cartridge is changed or a slide switch is reset.

(12) Set the FD PWR switch of the SKA3 to the PSA side.

(13) Key in "CB". (+5V VOLTAGE)

(14) Adjust the DC power voltage so that the DATA 0 indicator of the SKA3, XX.XX (V) indicates a value within the range of 5.00 ± 0.1V.
Data 1 indicator shows current consumption XXXX (mA) at that time.

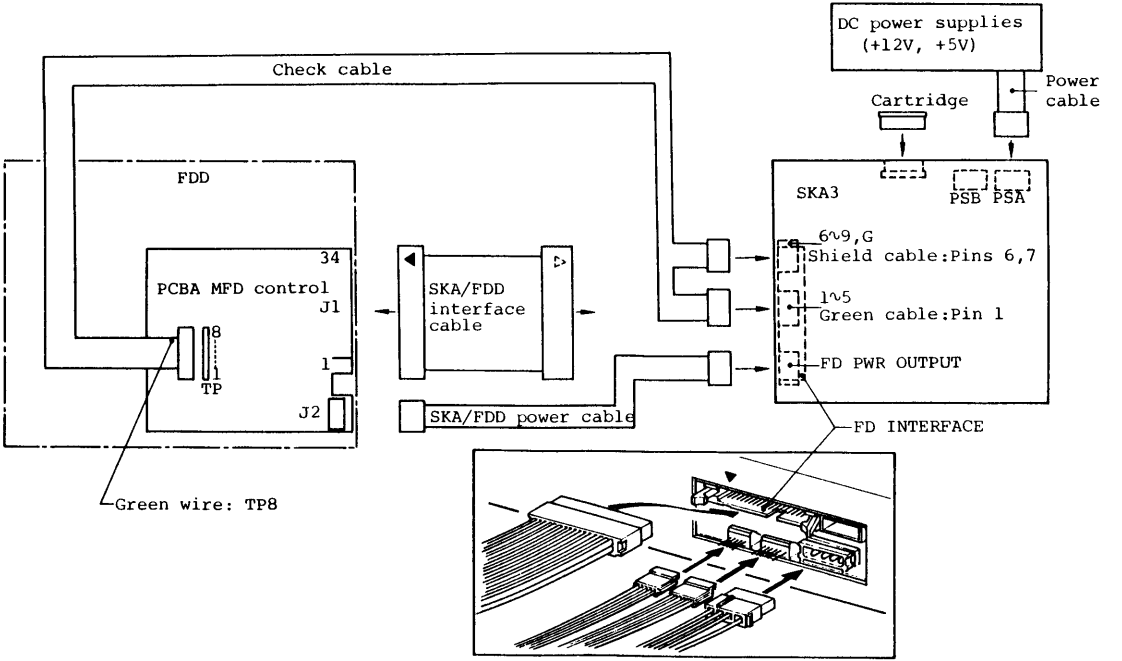
(15) Key in "F". (STOP)

(16) Key in "CC". (+12V VOLTAGE)

(17) Adjust the DC power voltage so that the DATA 0 indicator, XX.XX (V) indicates a value within the range of 12.00 ± 0.24V.
DATA 1 indicator shows current consumption XXXX (mA) at that time.

(18) Key in "F". (STOP)

Note: The above items (1) ∿ (4), (9) ∿ (11), (13) ∿ (17) may be omitted for replacement or temporary power off of the FDD. In this case, remain the DC power on for the SKA3 and control the FDD power by the FD PWR switch.



(Fig.3208) Connection of SKA3

3-2-4-2. Setting or confirmation of the maximum track number

This item is not required for SKA3 except for special testing because the maximum track number is pre-set to the cartridge. The following shows the confirmation or changing method for reference.

For a conventional SKA, set the maximum track number according to the following instructions before the check and the adjustment of the FDD. The setting will be maintained until the main DC power (SKA PWR) is turned off or until the RESET switch of the SKA is depressed. Since the FD PWR switch is independent of this setting, it is convenient to maintain the main DC power on for the successive operations.
The initial setting of the following is not required, if the maximum track number is the same as the initial value of the SKA.

(1) Key in "CF". (SET TMAX)

(2) The maximum track number set at that time is indicated with the latter two digits of the DATA (DATA 0 for SKA3) indicator, XXXX (track).

Note: If there is no change in the maximum track number in item (2), depress "F" key.

(3) Key in new maximum track number used for the FDD in two digits of decimal notation.

e.g. 48tpi (FD-55BR): CF 39 (for 40 cylinders)
96tpi (FD-55FR): CF 79 (for 80 cylinders)
96tpi, high density (FD-55GR): CF 76 (for 77 cylinders)

Note: If 80 cylinders are used in FD-55GR, key in "CF 79" also for the SKA. Key in "CF F", if it is the same as the initial value of the SKA.

3-2-4-3. Setting or confirmation of step rate and settling time

This item is not required for SKA3 except for 4msec seek model of FD-55BR because the step rate (STEP pulse interval) and the settling time of the FDD are pre-set to the cartridge. The following shows the comfirmation or changing method for reference.
For 4msec seek model of FD-55BR or for a conventional SKA, set the step rate and the settling time according to the following instruction before check and adjustment of the FDD.
The setting will be maintained until the main DC power (SKA PWR) is turned off or until the RESET switch of the SKA is depressed. The initial setting of the following is not required, if the step rate and the settling time are the same as the initial values of the SKA.

(1) Key in "DB". (SET STEP RATE)

(2) Step rate set at that time is indicated by 0.1msec scale on the DATA (DATA 0 for SKA3) indicator, XXX.X (ms).

e.g. DATA indicator "XX60" means 6.0msec.

(3) Key in a new step rate down to one decimal place (unit:msec).

Note: If there is no change in step rate in item (2), omit item (3) and forward to item (4).

(4) Key in "F". (Completion of step rate setting).

(5) Settling time at that time is indicated by 0.1msec scale on the DATA (DATA 1 for SKA3) indicator, XXX.X (ms).

e.g. DATA indicator "X150" means 15.0msec.

(6) Key in new settling time down to one decimal place (unit: msec).

Note: If there is no change in settling time in item (5), omit item (6) and depress "F" key to complete the operation.

(7) Depress "F" key. (STOP -- Completion of settling time setting).

e.g. 48tpi, 6msec seek model
(Step rate 6msec, Settling time 15msec): DB 60 F 150 F
48tpi, 4msec seek model
(Step rate 4msec, Settling time 10msec): DB 40 F 100 F
96tpi, 3msec seek model
(Step rate 3msec, Settling time 15msec): DB 30 F 150 F

3-2-4-4. Level disk calibration

Setting of the following calibration value is required for accurate measurement before the check of the read level or the resolution. Use a level disk with a calibration value (100% center) written on the label. The setting will be maintained until the main DC power (SKA PWR) is turned off or until the RESET switch of the SKA is depressed.

If the calibration value is the same as the initial value (100%) of the SKA, the initial setting of the following is not required. Also the setting in this item is not required when the level disk is not used (i.e., when it is substituted with a commercially available disk and no accurate measurement is required).

(A) Conventional SKA

(1) Innermost track read level

(a) Key in "D0". (CALIBRATION READ LEVEL)

(b) Calibration value set at that time is indicated in the latter three digits of the DATA indicator, XXXX (%).

(c) Key in a new calibration value written on the level disk label (three digits, Max.).

Notes: 1. If the side is changed for a double sided FDD, new calibration value shall be keyed in.
The side is changed alternately by a depression of "4" key.
If the side 1 is selected, SIDE 1 indicator of the SKA turns on.
Confirm the used side by the indication of the SIDE 1 indicator at the input of a new calibration value.
2. If there is no calibration change in item (b), omit item (c).

(d) Depress "F" key. (STOP)

(2) Innermost track resolution

(a) Key in "D1". (CALIBRATION RESOLUTION)

(b) The same as in item (1)-(b) ∿ (d).

e.g. READ LEVEL 103%, RESOLUTION 96%: D0 103 F, D1 96 F

(B) SKA3

(1) Innermost track read level

(a) Key in "D0". (CALIBRATION READ LEVEL)

(b) Side 0 calibration value set at that time is indicated in the latter three digits of the DATA 0 indicator, XXXX (%).

(c) Key in a new calibration value of side 0 written on the level disk label (three digits, Max.).

(d) Key in "F". (Completion of side 0 calibration setting)

(e) Side 1 calibration value set at that time is indicated in the latter three digits of the DATA 1 indicator, XXXX (%).

(f) Key in a new calibration value of side 1 written on the level disk label (three digits, Max.).

Note: If there is no calibration change, omit items (c) and (f).

(g) Depress "F" key. (Completion of side 1 calibration setting).

(2) Innermost track resolution

(a) Key in "D1". (CALIBRATION RESOLUTION)

(b) The same as in item (1) - (b) ∿ (g).

e.g. Double sided FDD, SIDE 0 READ LEVEL 103%, SIDE 1 READ LEVEL 95%
SIDE 0 RESOLUTION 96%, SIDE 1 RESOLUTION 98%:
D0 103 F 95 F, D1 96 F 98 F

3-2-4-5. Alignment disk calibration

Setting of the following calibration value is required for accurate measurement before the check and adjustment of the track alignment. Use a correctly calibrated (0% center) alignment disk with a calibration value written on the label. The setting will be maintained until the main DC power (SKA PWR) is turned off or until the RESET switch of the SKA is depressed.
If the calibration value is the same as the initial value (0%) of the SKA, the initial setting of the following is not required.

(A) Conventional SKA

(1) SIDE 0 alignment

(a) Key in "E0". (CALIBRATION SIDE 0 ALIGNMENT)

(b) Calibration value set at that time is indicated in the latter two digits of the DATA indicator, XXXX (%), and the polarity is indicated in the initial digit. If a "0" is indicated, the polarity is positive.

Polarity indication: plus +, minus -

(c) Key in a polarity and a new calibration value (two digits, Max.) written on the alignment disk label.

Designation of polarity: Depress "B" key only for minus designation. (No designation is reauired for plus).

Note: If there is no change in the calibration value in item (b), omit item (c).

(d) Depress "F" key. (STOP)

(2) Side 1 alignment

(a) Key in "E1". (CALIBRATION SIDE 1 ALIGNMENT)

(b) The same as in item (1)-(b) ∿ (d).

(3) Index burst timing

(a) Key in "E5". (CALIBRATION INDEX TIMING)

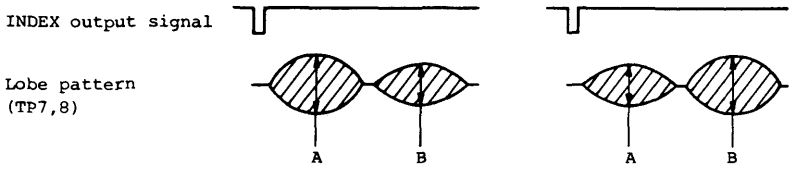
(b) Calibration value set at that time is indicated in the latter three digits of the DATA indicator, XXXX (μs), and the polarity is indicated in the initial digit. Refer to item (1)-(b).
If a "0" is indicated, the polarity is positive.

(c) Key in a polarity and a new calibration value (three digits, Max.) of side 0 written on the alignment disk label. Refer to item (1)-(c) as to the polarity designation.

Notes: 1. If the side is changed by key "4" for a double sided FDD, new calibration value for side 1 shall be keyed in. Refer to item 3-2-4-4, Note 1.
2. If there is no change in the calibration value in item (b), omit item (c).

(d) Depress "F" key. (STOP)

e.g. Double sided FDD, SIDE 0 ALIGNMENT +3%, SIDE 1 ALIGNMENT -5%,
INDEX TIMING -25μs:
E0 3 F, E1 B5 F, E5 B25 F

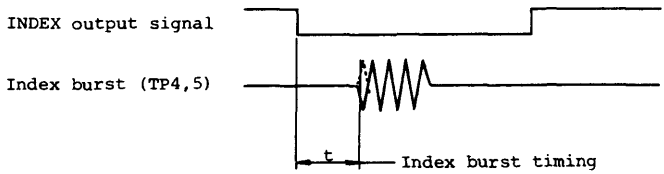


Notes: 1. The lobe pattern ratio is calibrated in the SKA according to the following expression.

$$\text{Lobe pattern ratio after calibration} = \frac{\text{A-B}}{\text{Larger one of A \& B}} \times 100 - \text{Calibration value (\%)}$$

2. If a calculated value with the above expression is positive, the polarity is plus, while the polarity is minus when a value is negative.

(Fig.3209) Calibration of alignment lobe pattern



Notes: 1. The index timing is calibrated in the SKA according to the following expression.

Calibrated timing = t - Calibration value (μs)

2. If a calculated value with the above expression is positive, the polarity is plus, while the polarity is minus when a value is negative.

(Fig.3210) Calibration of index burst timing

(B) SKA3

(1) Alignment

(a) Key in "E0". (CALIBRATION SIDE 0 ALIGNMENT)

(b) Side 0 calibration value set at that time is indicated in the latter two digits of the DATA 0 indicator, XXXX (%), and the polarity is indicated in the initial digit. If a "0" is indicated, the polarity is positive.

Polarity indication: plus +, minus -

(c) Key in a polarity and a new calibration value (two digits, Max.) of side 0 written on the alignment disk label.

Designation of polarity: Depress "B" key only for minus designation. (No designation is required for plus).

(d) Depress "F" key. (Completion of side 0 calibration setting)

(e) Side 1 calibration value set at that time is indicated in the latter two digits of the DATA 1 indicator, XXXX (%), and the polarity is indicated in the initial digit.

(f) Key in a polarity and a new calibration value (two digits, Max.) of side 1 written on the alignment disk label. Refer to item (c) as to the polarity designation.

Note: If there is no change in the calibration value, omit items (c) and (f).

(g) Depress "F" key. (Completion of side 1 calibration setting)

(2) Index burst timing

(a) Key in "E5". (CALIBRATION INDEX TIMING)

(b) Side 0 calibration value set at that time is indicated in the latter three digits of the DATA 0 indicator, XXXX (μs), and the polarity is indicated in the initial digit. Refer to item (1)-(b).
If a "0" is indicated, the polarity is positive.

(c) Key in a polarity and a new calibration value (three digits, Max.) of side 0 written on the alignment disk label. Refer to item (1)-(c) as to the polarity designation.

(d) Depress "F" key. (Completion of side 0 calibration setting)

(e) Side 1 calibration value set at that time is indicated in the latter three digits of the DATA 1 indicator, XXXX (μs), and the polarity is indicated in the initial digit.

(f) Key in a polarity and a new calibration value (three digits, Max.) of side 1 written on the alignment disk label. Refer to item (1)-(c) as to the polarity designation.

Note: If there is no change in the calibration value, omit items (c) and (f).

(g) Depress "F" key. (Completion of side 1 calibration setting)

e.g. Double sided FDD, SIDE 0 ALIGNMENT +3%, SIDE 1 ALIGNMENT -5%
SIDE 0 INDEX TIMING -40μs, SIDE 1 INDEX TIMING 20μs:
E0 3 F B5 F, E5 B40 F 20 F

3-2-4-6. Humidity setting

For the check and adjustment of the track alignment using an alignment disk, set the environmental relative humidity to the SKA in order to execute the accurate measurement.
This setting is important when the relative humidity is considerably different from 50% at 96tpi FDD.
The initial setting of the following is not required if the relative humidity is the same as the initial value (50%) of the SKA.

(1) Key in "F2". (CALIBRATION RH ALIGNMENT)

(2) The relative humidity set at that time is indicated in the latter two digits of the DATA (DATA 0 for SKA3) indicator, XXXX (%).

(3) Key in a new relative humidity (%) of the measurement environment (two digits, Max.)

e.g. Relative humidity 58%: E2 58

3-2-4-7. Gain setting

This item is applied only for conventional SKAs. Operator need not feel concern about this setting for the SKA3.

(1) Track alignment of 96tpi (FD-55FR/GR):

Key in "DD" to confirm that the H GAIN indicator is on.

(2) Track alignment of 48tpi (FD-55BR), and other items:

Confirm that H GAIN indicator is off. If it is on, depress "DD" key again to turn it off.

3-2-4-8. Setting of FDD straps and SKA special key

(1) Setting of FDD straps

It is required to confirm before the operation that the straps (short bars) on the PCBA MFD control are at the appropriate position for the system to be used in the check and adjustment.
For the purpose of simplyfying the explanation, it is recommended to set the following straps on when you use an SKA. However, if you can set the straps correctly referring to Specification, Schematic Diagrams, and Operation Manual, you need not to follow this recommendation.

Strap setting: Set the D0 and FG straps to on-state as a general rule. The other straps may be set as they were unless otherwise designated.
For a model with head load solenoid, set the HS strap to on-state and the HL strap should be off.

Notes: 1. If the strap position of the FDD is changed from the initial setting at the system installation, be sure to change it back to the initial position after maintenance.
2. When D1 strap is on, drive select is executed by key "1" of the SKA. Similarly D2 corresponds to key "2" and D3 to key "3". These keys of D0 ∿ D3 can also release the drive select condition by depressing the same key again.

(2) Setting of SKA special key

The signal level of the interface connector pin No.4 (IN USE/HEAD LOAD) changes alternately between TRUE and FALSE by depressing "A" (IN USE) key of the SKA. When it is TRUE, "A" indicator turns on. Refer to the Specification as to the function of the signal and its relation to the straps.

(3) Signal of interface connector pin No.34

While the output signal of interface connector pin No.34 (READY, OPEN, or other optional signals) is TRUE (LOW level), "RDY" indicator of the SKA turns on.
Refer to the Specification as to the function of the signal and its relation to the straps.

3-2-5. Others

(1) Total error test

In the check and adjustment in item 3-4, read/write error test is not included. After the adjustment or the replacement of the maintenance parts, it is recommended to perform a data error test by connecting the FDD to the user's system or the TEAC simulator KB. The window margin test is the most recommended item.

(2) Terminator

When you check each FDD with a maintenance system such as an SKA, it is necessary to put the terminator network into the IC socket J3 on the PCBA MFD control. The terminator shall be returned to the initial condition after completion of the maintenance.

For the fixed type terminator without IC socket (soldered on PCB), above instruction is not applied.

(3) Connection of probe ground

Connect the probe ground of the equipment as follows:

(a) For observation of test points (TP) 4, 5 (Pre-amplifier) and TPs 7, 8 (Differentiation amplifier):
Connect the probe ground to TP6 (0V) on the PCBA MFD control.

(b) For observation of the other test points and FDD circuits:
Connect the probe ground to TP6 (0V) on the PCBA MFD control, or GND (0V) terminal of the system power supply unit, or the GND terminal of the SKA. The frame of the FDD may be also used when the FG strap is on-state.

(c) For observation of SKA test points:

Connect the probe ground to the following terminal.

i) Conventional SKA: GND terminal of the SKA

ii) SKA3, PRE and DIF terminals: TP1 (GND) of the SKA3
Other terminals: TP4 (GND) of the SKA3

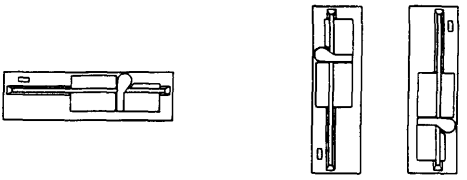
Note: When you use the SKA, almost all the checks including the read amp. output level at TPs of the FDD will be done automatically through the check cable and FDD interface cable.
Also these signals can be observed by an oscilloscope using the test points on an SKA.

(4) Head load of CSS model

For a CSS model (without head load solenoid), the FDD is always in head load condition as far as a disk is inserted and the front lever is closed.

(5) Orientation of the FDD

Position the FDD as shown in Fig.3211 unless otherwise specified.



Horizontal setting Vertical setting

(Fig.3211) General orientation of FDD during maintenance

(6) Maintenance environment

Maintenance of the FDD should be done on a clean bench at room temperature and humidity. It is recommended to execute the check and adjustment of the track alignment after leaving the FDD for at least 2 hours at room temperature and humidity. The magnetic head, disk, steel belt, etc. might suffer from dust and dirt if the maintenance is not undertaken in a clean environment.

(7) Disk

There are two sectoring types in normal density disks which are soft sectored disk and hard sectored disk. Use soft sectored disks when an SKA is used.
For the check and adjustment of high density FDD (FD-55GR), appropriate high density (HD) disk is required.

3-3. PREVENTIVE MAINTENANCE

3-3-1. Cleaning of Magnetic Head by Cleaning Disk

When you use the FDD in dusty environment, it is recommended to clean the magnetic head surface periodically (e.g. once a month) with a commercially available cleaning disk.
For a typical usage under typical environmental condition, the cleaning cycle is enough at every three months.

(A) Equipment

(1) Dry type cleaning disk
(2) SKA or user's system

(B-1) Cleaning procedure (General method)

(1) Install an appropriate cleaning disk and start the spindle motor.

Notes: 1. Do not use a damaged cleaning disk.
2. Be sure to use a double sided cleaning disk. Side 0 (lower side) and side 1 (upper side) heads will be cleaned at the same time.

(2) Execute head loading and clean the head at a suitable track position for 10 ∿ 30 seconds, approx. In order to avoid the concentration on a specific track, it is a good way to make the head move between track 00 and the innermost track during cleaning operation.

Note: The most appropriate cleaning time is different for each type of cleaning disk used.
Excessively long cleaning time is not effective but has possibility to accelerate the head wear.

(3) Remove the cleaning disk.

(B-2) Cleaning procedure (SKA method)

(1) Connect an SKA referring to item 3-2-4 and set the FD PWR switch to the PSA side.

(2) Execute drive select by key "0". (DS0 indicator turns on).

(3) Key in "C0" and confirm that the TRACK indicator of the SKA becomes "00". (RECALIBRATE)

(4) Install an appropriate cleaning disk. See item (B-1), "Notes".

(5) Start the spindle motor by key "5". (MON indicator turns on).

(6) Key in "C6". (SEEK TEST)

(7) After 10 ∿ 30 seconds, depress "F" key.

(8) Eject the cleaning disk.

3-4. CHECK AND ADJUSTMENT

3-4-1. Adjustment of Set Arm Position

(A) Equipment

(1) Cross point screwdriver, M3

(B) Adjustment procedure

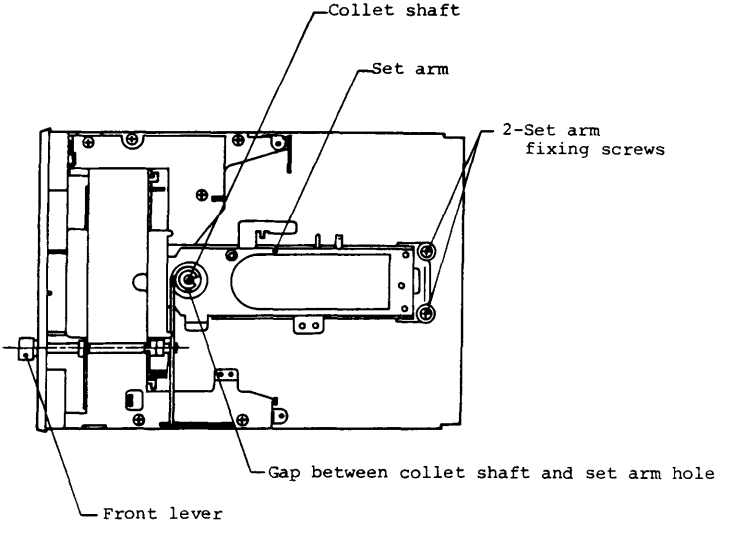
(1) Loosen two fixing screws of the set arm (see Fig.3401) so that the set arm can be moved manually without getting out of place.

(2) Close the set arm by turning the front lever.

(3) In this condition (item (2)), adjust the set arm so that the visial gap between the collet shaft and the set arm hole becomes even.

(4) Tighten the installing screws of the set arm with the specified torque.

(5) Open and close the set arm by turning the front lever and confirm that it does so smoothly.



(Fig.3401) Adjustment of set arm position

3-4-2. Check and Adjustment of Holder Position

This item is applied for a standard model without optional disk eject mechanism.

(A) Equipment

(1) Cross point screwdriver, M3
(2) MAX media jigs C and E

(B) Check and adjustment procedure

(1) Insert the MAX media jig E from open side until it strikes the frame stopper. Refer to Fig.3402.

(2) When closing the front lever at the stop side of the MAX media jig E, confirm that the wing of the front lever disturbs the rotation and that the lever cannot be closed.

(3) When turning the MAX media jig E over to insert it for pass side, and closing the front lever, confirm that the lever can be closed.

(4) If the item (2) or (3) is not satisfied, adjust the holder position according to the following procedure.

(a) Loosen four fixing screws (see Fig.3403) of the holder so that the holder can be moved manually without going out of place.

(b) Install the MAX media jig C from open side to set it to be in contact with the frame stopper.

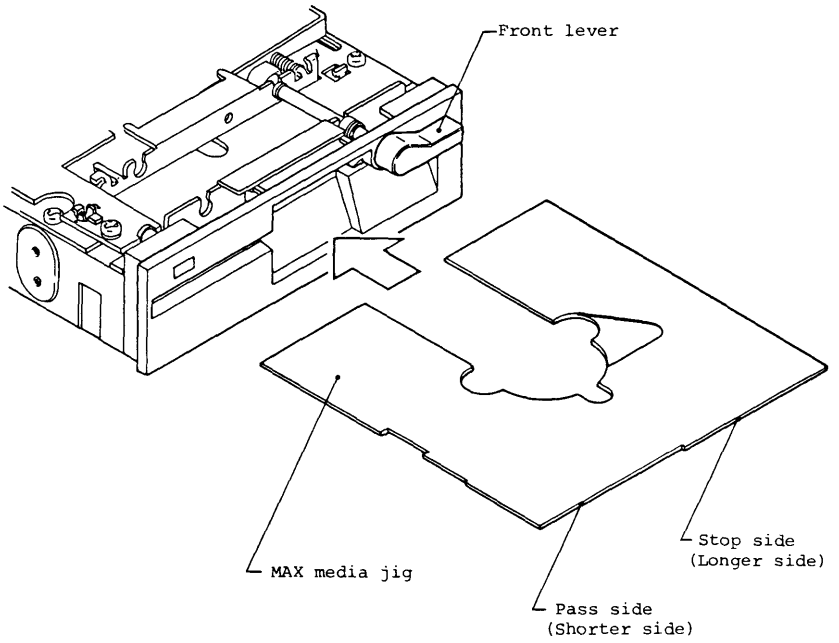
(c) Turn the front lever to close position. Loosen the fixing screws of the holder again to make the holder move toward the arrow indicated direction in Fig.3403, then depress the wing area of the front lever against the MAX media jig C. Refer to Fig.3404.

(d) Tighten the four fixing screws of the holder with specified torque.

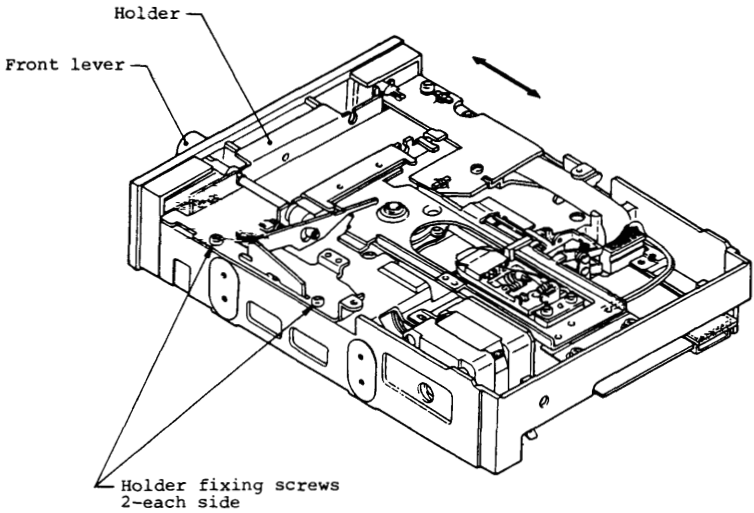
(e) Confirm items (1) through (3).

(f) Check for the file protect sensor according to item 3-4-5.

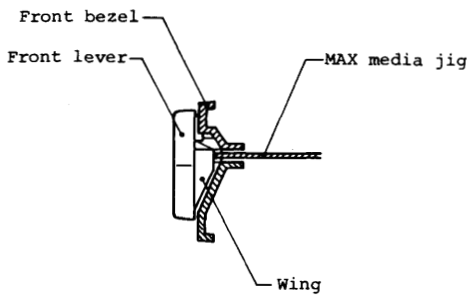
(g) Check and adjust the index burst timing according to item 3-4-15.



(Fig.3402) Insertion of MAX media jig



(Fig.3403) Adjustment of holder position 1



(Fig.3404) Adjustment of holder position 2

3-4-3. Check and Adjustment of Arm Lifter

This item is applied only for a double sided model with head load solenoid Ass'y.

(A) Equipment

(1) Common screwdriver, small size
(2) Work disk
(3) SKA or user's system
(4) Oscilloscope
(5) Locking paint

(B-1) Check and adjustment procedure (General method)

(1) Use two channels of oscilloscope. Connect the 1st channel to the head load command signal and the 2nd channel to TP7 or TP8 on the PCBA MFD control. Triggering should be done by the head load command.

Oscilloscope range, The 1st channel: DC mode, 2V, 20msec
The 2nd channel: AC mode, 0.5 ∿ 1V, 20msec

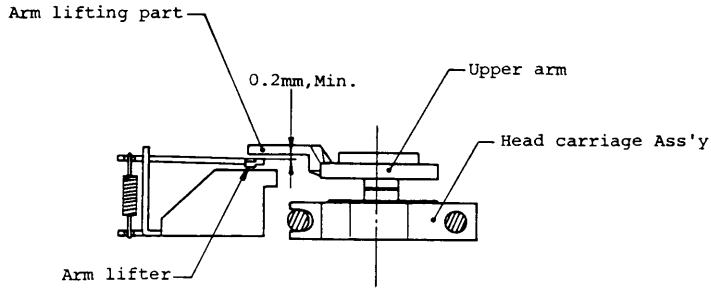
Note: For the purpose of check and adjustment in this item, it is not proper to execute the head loading by the MOTOR ON signal. Use either of the DRIVE SELECT signal or the IN USE/HEAD LOAD signal. Refer to item 3-2-4-8 (1) or the Specification item 1-12.

(2) Install a work disk and start the spindle motor.

(3) Set the head to track 00.

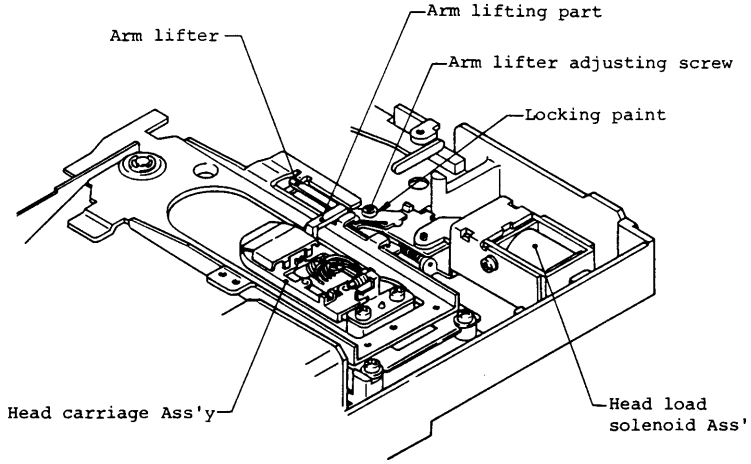
(4) Select the side 1 head.

(5) Execute the head loading.



Note: Viewed from front bezel side.

(Fig.3405) Gap of arm lifter



(Fig.3406) Adjustment of arm lifter

(6) Confirm that the gap between the upper arm and the arm lifter is larger than 0.2mm. Refer to Fig.3405.

(7) Execute 2F write operation (WRITE DATA frequency of 250KHz for FD-55BR /FR and 500KHz for FD-55GR) for one rotation of the disk.

(8) Unload the head.

(9) Repeat the head loading and unloading alternately (tapping operation) and observe the waveform of TP7 or TP8 by the oscilloscope.

(10) Set the oscilloscope trigger to the positive mode and observe the read waveform at TP7 or TP8 after the input of an unload command.

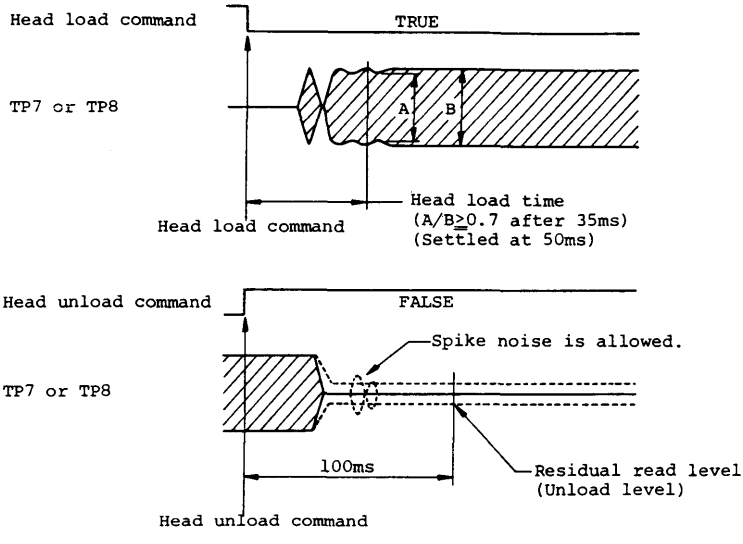
(11) Confirm that there is no unload level (excludes very small one) at 100msec after the unload command as shown by dotted line in Fig.3407.

Note: This item shall be executed when the side 1 head is selected. If the side 1 head is lifted too high during unload operation, tapping sound increases and disk wear will be accelerated, while unload level will be observed when it is too low.

(12) Set the oscilloscope trigger to the negative (-) mode and observe the waveform at TP7 or TP8 after the input of a head load command. Confirm that the read waveform more than 50msec after the head load command is almost settled.
Or confirm that bottom "A" of the read level more than 35msec after the input of the head load command is more than 0.7 against the average read level "B". ($A/B \geq 0.7$ in Fig.3407)

(13) Make the head move to the innermost track.

(14) Repeat the procedure from item (7) to (12).



(Fig.3407) Read waveforms at head loading/unloading

(15) If the value in item (6), (11), (12), or (14) is out of the specified range, adjust according to the following procedure.

(a) Execute items (3) through (10).

(b) Loosen the unload adjusting screw until the unload level is observed at 100msec after the unload command. Refer to dotted line in Fig.3407.

(c) Tighten the adjusting screw little by little and search the screwing point where the unload level exactly disappears at 100msec after the unload command.

(d) Make the head move to the innermost track.

(e) Confirm unload level according to item (11).
If the unload level is observed at 100msec after the unload command, repeat item (c) at the innermost track.

(f) Tighten the adjusting screw by 90° from the above point.

(g) Apply a drop of locking paint on the adjusting screw.

(16) Again set the head to track 00.

(17) After opening the front lever, draw out the disk slowly. In the process of drawing out, the side 0 and side 1 heads shall not catch the head window edge of the disk jacket (opening area of the jacket to make the head be in contact with the disk surface). The jacket can be drawn out smoothly with appropriate space margin.

(18) Insert the disk slowly and confirm that the disk jacket does not touch the side 0 nor side 1 head and goes into the FDD smoothly with appropriate space margin.

(19) If the strap setting was changed, back it to the initial setting after the check and adjustment.

(B-2) Check and adjustment procedure (SKA method)

(1) Connect an SKA according to item 3-2-4 and set the FD PWR switch to the PSA side.

(2) Install a work disk.

(3) Use two channels of oscilloscope. Connect the 1st channel to the DOUT terminal and the 2nd channel to the DIF terminal of the SKA. Apply negative trigger by the DOUT terminal.

Oscilloscope range, The 1st channel: DC mode, 2V, 20msec
The 2nd channel: AC mode, 0.5 ∿ 1V, 20msec

Note: For the check and adjustment in this item, it is required to set the straps according to item 3-2-4-8 (1).

(4) Key in "BC F". (DRIVE SELECT observation)

(5) Start the spindle motor by key "5". (MON indicator turns on).

(6) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

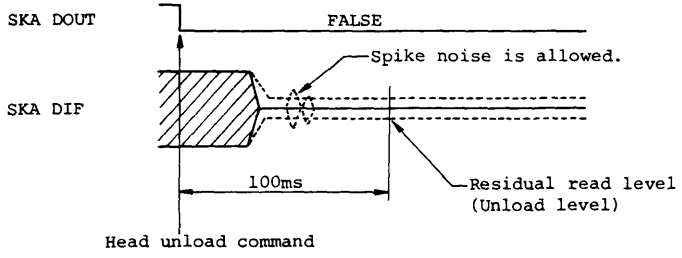
(7) Select the side 1 head by key "4". (SIDE 1 indicator turns on).

(8) Execute drive select and head loading by key "0". (DS0 indicator turns on).

(9) Confirm that the gap between the upper arm and the arm lifter is larger than 0.2mm. Refer to Fig.3405.

(10) Key in "C9" for a conventional SKA or key in "C9A" for SKA3. (HEAD LOAD TIME).

(11) Observe the waveform of the DIF terminal at head unloading using the oscilloscope.



(Fig.3408) Read waveform at head unloading

(12) Confirm that there is no unload level (excludes very small one) at 100msec after the unload command as shown by dotted line in Fig.3408.

Note: This item shall be executed when the side 1 head is selected (SIDE 1 indicator turns on).
If the side 1 head is lifted too high during unload operation, tapping sound increases and disk wear will be accelerated, while unload level will be observed when it is too low.

(13) Confirm that the DATA indicator, XXXX (%) of the SKA indicates a value within the following range.

Head load settling level: 70%, Min.

(14) Key in "F". (STOP)

(15) If the DS0 indicator of the SKA is off, execute drive select by key "0". (DS0 indicator turns on).

(16) Key in "C1". (SEEK TMAX)

(17) Repeat the procedure from item (10) to (14).

(18) If the value in item (9), (12), (13), or (17) is out of the specified range, adjust according to the following procedure.

(a) Key in "C0" (RECALIBRATE) and execute items (10) and (11).

(b) Loosen the unload adjusting screw until the unload level is observed at 100msec after the unload command. Refer to dotted line in Fig.3408.

(c) Tighten the adjusting screw little by little and search the screwing point where the unload level exactly disappears at 100msec after the unload command.

(d) Key in "F". (STOP)

(e) Key in "C1" (SEEK TMAX) and execute items (10) and (11).

(f) Confirm unload level according to item (12).
If the unload level is observed at 100msec after the unload command, repeat item (c) at the innermost track.

(g) Key in "F". (STOP)

(h) Tighten the adjusting screw by 90° from the above point.

(i) Apply a drop of locking paint on the adjusting screw.

(19) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

(20) After opening the front lever, draw out the disk slowly. In the process of drawing out, the side 0 and side 1 heads shall not catch the head window edge of the disk jacket (opening area of the jacket to make the

head be in contact with the disk surface). The jacket can be drawn out smoothly with appropriate space margin.

(21) Insert the disk slowly and confirm that the disk jacket does not touch the side 0 nor side 1 head and goes into the FDD smoothly with appropriate space margin.

(22) If the strap setting was changed, back it to the initial setting after the check and adjustment.

3-4-4. Check of CSS Ass'y

This item is applied only for a double sided CSS model (without head load solenoid).

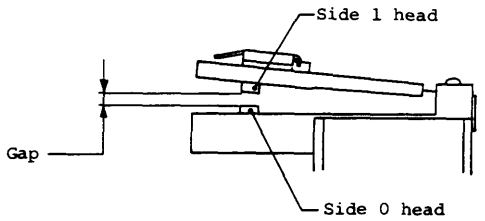
(A) Equipment

(1) Work disk
(2) SKA or user's system

(B-1) Check procedure (General method)

(1) Open and close the front lever with no insertion of a disk.

(2) Confirm that the side 1 head is lifted even if the front lever is closed and it has enough gap against the side 0 head. (See Fig.3409).



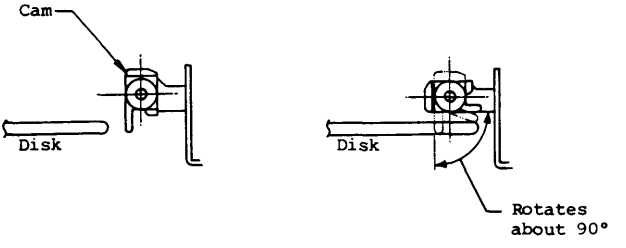
(Fig.3409) Gap between side 0 and side 1 heads

(3) After opening the front lever, insert a work disk slowly. Confirm that the disk jacket does not touch the side 0 nor side 1 head and goes into the FDD smoothly with appropriate space margin.

(4) Draw out the disk slowly. Confirm that the side 0 and side 1 heads do not catch the head window edge of the disk jacket (opening area of the jacket to make the head be in contact with the disk surface)

and that the jacket can be drawn out smoothly with appropriate space margin.

(5) Confirm that the cam (natural color) of the CSS Ass'y attached to the left side of the head carriage moves as in Fig.3410 by opening/closing of the front lever and insertion/ejection of the disk.



(a) Disk is not fully inserted. (b) Disk is fully inserted and front lever is close.

(Fig.3410) Cam rotation of CSS Ass'y

(6) Insert a work disk and start the spindle motor.

(7) Set the head to track 00.

(8) In the close condition of the front lever, confirm that the gap between the upper arm and the arm lifter is 0.2mm, Min. Refer to Fig.3405.

(9) Make the head move to the innermost track.

(10) Confirm as in item (8).

(B-2) Check procedure (SKA method)

(1) Open and close the front lever with no insertion of a disk.

(2) Confirm that the side 1 head is lifted even if the front lever is closed and it has enough gap against the side 0 head. Refer to Fig.3409.

(3) After opening the front lever, insert a work disk slowly.
Confirm that the disk jacket does not touch the side 0 nor side 1 head and goes into the FDD smoothly with appropriate space margin.

(4) Draw out the disk slowly. Confirm that the side 0 and side 1 heads do not catch the head window edge of the disk jacket (opening area of the jacket to make the head be in contact with the disk surface) and that the jacket can be drawn out smoothly with appropriate space margin.

(5) Confirm that the cam (natural color) of the CSS Ass'y attached to the Left side of the head carriage moves as in Fig.3410 by opening/closing of the front lever and insertion/ejection of the disk.

(6) Connect an SKA according to item 3-2-4 and set the FD PWR switch to the PSA side.

(7) Start the spindle motor by key "5". (MON indicator turns on).

(8) Execute drive select by key "0". (DS0 indicator turns on).

(9) Key in "C0" and confirm that the TRACK indicator becomes "00".
(RECALIBRATE)

(10) In the close condition of the front lever, confirm that the gap between the upper arm and the arm lifter is 0.2mm, Min.
Refer to Fig.3405.

(11) Key in "C1". (SEEK TMAX)

(12) Confirm as in item (10).

3-4-5. Check of File Protect Sensor

(A) Equipment

(1) MAX media jig C
(2) SKA or user's system

(B-1) Check procedure (General method)

(1) Place the FDD on the work bench with the LED indicator up and the front lever down. (See Fig.3411).

(2) Connect an oscilloscope (DC range, 2V/div) to the WRITE PROTECT interface line.

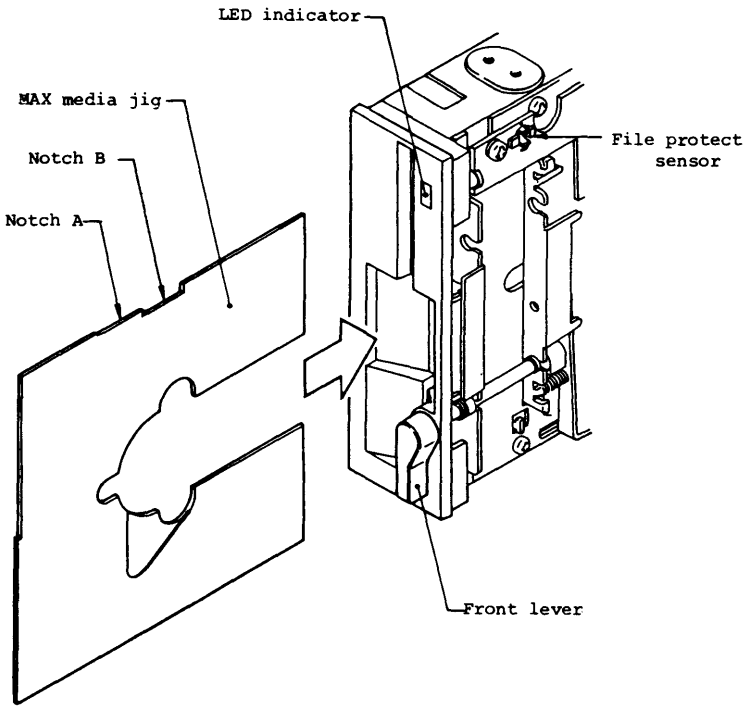
(3) Insert the MAX media jig C from open side and set it so that the notch A area is located on the light pass from the file protect sensor LED. See Fig.3411.

(4) Adjust the orientation of the FDD so that it is not exposed with strong light.

(5) Confirm that the WRITE PROTECT signal goes to LOW level when power is supplied and the FDD is DRIVE SELECTed.

(6) Pull out the jig a little so that the notch B area is located on the light pass.

(7) Confirm that the WRITE PROTECT signal goes to HIGH level.



(Fig.3411) Check of file protect sensor

(B-2) Check procedure (SKA method)

(1) Connect an SKA according to item 3-2-4 and set the FD PWR switch to the PSA side.

(2) Insert the MAX media jig C from open side and set it so that the notch A area is located on the light path from the file protect sensor LED. See Fig.3411.

(3) Adjust the orientation of the FDD so that it is not exposed with strong light.

(4) Confirm that the WPROT indicator of the SKA turns on, when the FDD is selected by key "0". (DS0 indicator turns on).

(5) Pull out the jig a little so that the notch B area is located on the light path.

(6) Confirm that the WPROT indicator turns off.

3-4-6. Check of Disk Rotation Speed

Disk rotation speed is set to 300rpm for FD-55BR/FR and 360rpm for FD-55GR.

(A) Equipment

(1) SKA or user's system
(2) Frequency counter (not required when an SKA is used)
(3) Work disk

(B-1) Check procedure (General method)

(1) Connect a frequency counter to TP1 (Index) on the PCBA MFD control or to the INDEX interface signal line.

(2) Install a work disk and start the spindle motor.

(3) Set the head to track 00.

(4) Execute the head loading.

(5) Confirm that the pulse interval at TP1 or at the INDEX interface is withon the following range.

Index interval, FD-55BR/FR: 200 ± 3msec
FD-55GR: 166.7 ± 2.5msec

(B-2) Check procedure (SKA method)

(1) Connect an SKA referring to item 3-2-4 and set the FD PWR switch to the PSA side.

(2) Install a work disk.

(3) Start the spindle motor by key "5". (MON indicator turns on).

(4) Execute drive select by key "0". (DS0 indicator turns on).

(5) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

(6) Key in "C3". (INDEX INTERVAL)

(7) Confirm that the DATA (DATA 0 for SKA3) indicator, XXXX (ms) indicates a value within the following range.

Index interval, FD-55BR/FR: 200 ± 3msec
FD-55GR: 166.7 ± 2.5msec

(8) Depress "F" key. (STOP)

3-4-7. Check of Erase Gate Delay

The purpose of this item is to confirm the function of the control LSI. This item is not so important as far as the FDD operates normally.

(A) Equipment

(1) SKA or user's system
(2) Oscilloscope (not required when an SKA is used)
(3) Work disk

(B-1) Check procedure (General method)

(1) Use two channels of oscilloscope. Connect the trigger channel to the WRITE GATE interface line and the other channel to TP2 (Erase gate delay) on the PCBA MFD control.
Oscilloscope range: For both channels, DC mode, 5V, 100μsec

(2) Install a work disk and start the spindle motor.

(3) Execute the head loading.

(4) Set the oscilloscope to the negative trigger (-) mode. Make the WRITE GATE signal TRUE (write command).

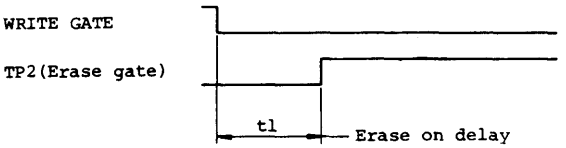
(5) Confirm that "t1" (Erase on delay) in Fig.3412 is within the following range.

Erase on delay, FD-55BR/FR: 240 ∿ 290μsec
FD-55GR: 200 ∿ 240μsec

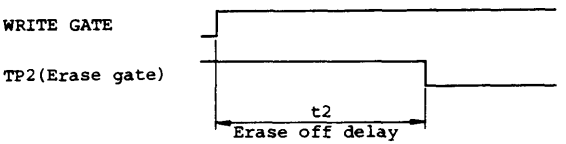
(6) Set the oscilloscope to the positive trigger (+) mode. Make the WRITE GATE signal FALSE.

(7) Confirm that "t2" (Erase off delay) in Fig.3413 is within the following range.

Erase ofd delay, FD-55BR/GR: 890 ∿ 990μsec
FD-55GR: 530 ∿ 590μsec



(Fig.3412) Erase on delay



(Fig.3413) Erase off delay

(B-2) Check procedure (SKA method)

(1) Connect an SKA and check cable according to item 3-2-4 and set the FD power switch to the PSA side.

(2) Install a work disk.

(3) Start the spindle motor by key "5". (MON indicator turns on).

(4) Execute drive select by key "0". (DS0 indicator turns on).

(5) Key in "7". (WRITE GATE ON)

(6) Confirm that the DATA (DATA 0 for SKA3) indicator, XXXX (μs) shows a value within the following range.

Erase on delay, FD-55BR/FR: 240 ∿ 290μsec
FD-55GR: 200 ∿ 240μsec

(7) Key in "7" again. (WRITE GATE OFF)

(8) Confirm that the DATA (DATA 1 for SKA3) indicator, XXXX (μs) shows a value within the following range.

Erase off delay, FD-55BR/FR: 890 ∿ 990μsec
FD-55GR: 530 ∿ 590μsec

3-4-8. Check of Head Touch

(A) Equipment

(1) Work disk
(2) SKA or user's system
(3) Oscilloscope (not required when an SKA is used)
(4) DC clip on ammeter (not required when an SKA is used)

(B-1) Check procedure (General method)

(1) Connect an oscilloscope to TP7 or TP8 (Differentiation amp.) on the PCBA MFD control.
Oscilloscope range: AC mode, 0.1 ∿ 0.2V, 20msec

(2) Install a work disk and start the spindle motor.

(3) Set the head to the innermost track.

(4) Execute the head loading.

(5) Repeat the cycle of one write rotation and one read rotation.
Write data should be the fixed pattern of 2F (250KHz of WRITE DATA frequency for FD-55BR/FR and 500KHz for FD-55GR).

(6) Write down the average read level measured during the read operation of item (5).

(7) Execute items (5) and (6) with a slight depression (very slight depression easy to release: 10 ∿ 20g) by a finger on the top of the upper head, and measure the average read level as in item (6).

(8) Confirm that the read level measured in item (6) is greater than 80% of that in item (7).

(9) Execute items (5) through (8) respectively for side 0 and side 1 heads.

(10) After making the head move to track 00, execute items (5) through (9).

(11) Possible causes for insufficient head touch:

Following causes are assumed for the insufficient result in items (8) through (10).

(a) Inferior disk:

Disk and/or jacket is deformed or damaged. Replace the work disk with a new one.

(b) Inferior head flexture:

Because of the failed performance of the arm lifter in item 3-4-3 (model with head load solenoid) or the failed performance of the CSS Ass'y in item 3-4-4 (CSS model without head load solenoid), the flexture on which the head piece is located may be deformed. Remove the disk. Then open and close the front lever slowly to observe the gap between the side 1 and side 0 heads from the front bezel. If the two head surfaces are not in parallel each other, it is considered to be the deformation.
Replace the head carriage Ass'y according to item 3-5-1.

(c) Inferior load force:

If the upper arm is over-lifted manually by careless handling during replacement of the head carriage Ass'y and etc., spring at the upper arm supporting point may be deformed and the head load force may decrease. Carefully replace the head carriage Ass'y according to item 3-5-1.

(d) Inferior pressure of the jacket pads:

If the jacket pad attached under the set arm does not touch the jacket surface, replace the pads. Refer to Fig.405 in Parts List.

Caution: If the jacket surface is excessively pressed by the pads, the spindle motor might be overloaded because of increasing the rotation torque.

(B-2) Check procedure (SKA method)

(1) Connect an SKA and check cable according to item 3-2-4 and set the FD PWR switch to the PSA side.

(2) Install a work disk.

(3) Start the spindle motor by key "5". (MON indicator turns on).

(4) Execute drive select by key "0". (DS0 indicator turns on).

(5) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

(6) Key in "C1". (SEEK TMAX)

(7) Key in "D3". (WRITE/READ LEVEL PRE 2F)

(8) Write 2F and read operations are repeated.
The DATA indicator, XXXX (mV) indicates the average read level at TP4 and TP5 (Pre-amp.) after each cycle of operation (one rotation of write and one rotation of read) is finished.

(a) When SKA3 is used:
By keying in "D3", side 0 and side 1 read levels are indicated on DATA 0 and DATA 1 indicators successively.

(b) When conventional SKA is used:
Depress "F" key (STOP) and then depress "4" key to execute items (7) through (10) for side 0 and side 1 heads respectively. The side is changed alternately by a depression of "4" key. If side 1 is selected, SIDE 1 indicator of the SKA turns on.

(9) Observe the DATA indicators with a slight depression (very slight

depression easy to release: 10 ∿ 20g) by a finger on the top of the upper head.

(10) Confirm that side 0 and side 1 read levels measured in item (8) are more than 80% of that in item (9).

(11) Key in "C0" (RECALIBRATE), and execute items (7) through (10) in the similar way.

(12) Possible causes for insufficient head touch:

Refer to item (11) of "General method".

3-4-9. Check of Asymmetry

Adjustment is applied only for a model with variable resistor on the PCBA MFD control.

(A) Equipment

(1) Common screwdriver, small size
(2) Work disk
(3) SKA or user's system
(4) Oscilloscope (not required when SKA3 is used)

(B-1) Check and adjustment procedure (General method)

(1) Connect an oscilloscope to the READ DATA interface line.
Oscilloscope range: DC mode, 2V, 0.5 ∿ 1μsec

(2) Install a work disk and start the spindle motor.

(3) Set the head to the innermost track.

(4) Execute the head loading.

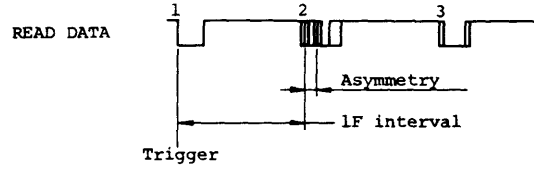
(5) Execute 1F write operation for one rotation of the disk (125KHz of WRITE DATA frequency for FD-55BR/FR and 250KHz for FD-55GR).

(6) Measure the asymmetry referring to Fig.3414.

Note: Oscilloscope should be so set that three READ DATA pulses can be observed. Asymmetry value shall be measured at the second READ DATA pulse from the trigger pulse.

(7) Confirm that the average asymmetry is within the following range.

Innermost track 1F asyymetry, FD-55BR/FR: 0.7μsec, Max.
FD-55GR: 0.35μsec, Max.



(Fig.3414) Measurement of asymmetry

(8) Execute items (5) through (7) for side 0 and side 1 heads respectively.

(9) If the value in item (7) or (8) is out of the specified range, adjust according to the following procedure.

Note: This item is applied only for a model with a variable resistor for asymmetry adjustment.

(a) Adjust the variable resistor, R1 on the PCBA MFD control so that the asymmetry takes a small value while repeating 1F write and 1F read operations alternately.

(b) Repeat the operation in item (a) for side 0 and side 1 heads alternately. The variable resistor shall be so adjusted that both asymmetry for side 0 and side 1 heads take the minimum value. Refer to Fig.220 in item 2-3-2.

(10) If the value in item (7) or (8) is out of the specified range on a model without variable resistor, or if the adjustment in item (9) cannot be done sufficiently, following causes are assumed.

(a) Leakage flux density in the environmental condition of the FDD is high:

If there is some flux sources near the FDD such as magnet, transformer, motor, Brown tube, magnetized iron plate, etc., take it apart from the FDD. Then measure the asymmetry and adjust again.

(b) Inferior disk:
Replace the work disk with a new one.

(c) Inferior head:
Replace the head carriage Ass'y according to item 3-5-1.

(d) Inferior PCBA MFD control:
Replace the PCBA according to item 3-5-7.

(B-2) Check and adjustment procedure (Conventional SKA method)

(1) Connect an conventional SKA according to item 3-2-4 and set the FD PWR switch to the PSA side.

(2) Key in "B1 F". (1F DUTY)

(3) Connect an oscilloscope to the DOUT terminal of the SKA.
Oscilloscope range: DC mode, 2V, 0.1 ∿ 0.2μsec

(4) Install a work disk.

(5) Start the spindle motor by key "5". (MON indicator turns on).

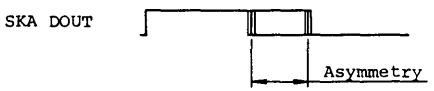
(6) Execute drive select by key "0". (DS0 indicator turns on).

(7) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

(8) Key in "C1". (SEEK TMAX)

(9) Key in "D4". (WRITE/READ LEVEL PRE 1F)

(10) Measure the asymmetry as in Fig.3415.



(Fig.3415) Measurement of asymmetry

(11) Confirm that the average asymmetry is within the following range.

Innermost track 1F asymmetry, FD-55BR/FR: 0.7μsec, Max.
FD-55GR: 0.35μsec, Max.

(12) Depress "4" key and execute items (9) through (11) for side 0 and side 1 heads respectively. The side is changed alternately by a depression of "4" key. If the side 1 is selected, SIDE 1 indicator of the SKA turns on.

(13) If the value in item (11) or (12) is out of the specified range, adjust according to the following procedure.

Note: This item is applied only for a model with a variable resistor for asymmetry adjustment.

(a) Adjust the variable resistor, R1 on the PCBA MFD control so that the asymmetry takes a small value by keying in "D4".

(b) Execute the operation in item (a) for both sides alternately by changing the side by key "4". The variable resistor shall be so adjusted that both asymmetry for side 1 and side 0 heads take the minimum value. Refer to Fig.220 in item 2-3-2.

(14) If the value in item (11) or (12) is out of the specified range on a model without variable resistor, or if the adjustment in item (13) cannot be done sufficiently, refer to item (10) of "General method".

(B-3) Check and adjustment procedure (SKA3 method)

(1) Connect the SKA3 referring to item 3-2-4 and set the FD PWR switch to the PSA side.

(2) Install a work disk.

(3) Start the spindle motor by key "5". (MON indicator turns on).

(4) Execute drive select by key "0". (DS0 indicator turns on).

(5) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

(6) Key in "C1". (SEEK TMAX)

(7) Key in "DD". (ASYMMETRY)

(8) Write 1F and read operations are repeated.
Asymmetry values of side 0 and side 1 heads are indicated on the DATA 0 and DATA 1 indicators, XXXX (ns) successively after each cycle of operation. DATA 0 indicates a value of side 0 head while DATA 1 indicates a value of side 1 head. The initial digit shows "E" which has no relation to this item.

(9) Confirm that the both average values are within the following range.

Innermost track 1F asymmetry, FD-55BR/FR: 700nsec, Max.
FD-55GR: 350nsec, Max.

(10) Key in "F". (STOP)

(11) If the value in item (9) is out of the specified range, adjust according to the following procedure.

Note: This item is applied only for a model with a variable resistor for asymmetry adjustment.

(a) Key in "DD" and adjust the variable resistor, R1 on the PCBA MFD control so that the asymmetry takes the minimum value. Since the asymmetry changes at every measurement, rough adjustment will be done.

(b) The variable resistor shall be so adjusted that both asymmetry for side 0 and side 1 heads take the minimum value. Refer to Fig.220 in item 2-3-2.

(c) Key in "F".

(12) If the value in item (9) is out of the specified range on a model without variable resistor, or if the adjustment in item (11) cannot be done sufficiently, refer to item (10) of "General method".

3-4-10. Check of Read Level

(A) Equipment

(1) Level disk
(2) SKA or user's system
(3) Oscilloscope (not required when an SKA is used)

(B-1) Check procedure (General method)

(1) Use two channels of an oscilloscope and connect them to TP7 and TP8 (Differentiation amp.) on the PCBA MFD control.
Oscilloscope range: AC mode, 0.2 ∿ 0.5V
Set both channels, 1 and 2 to the above range. Set either of the channels to Invert mode and Add both channels.

(2) Install a level disk and start the spindle motor.

(3) Set the head to the innermost track.

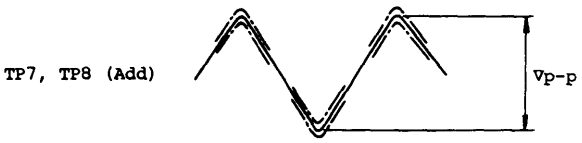
(4) Execute the head loading.

(5) Execute 2F write operation for one rotation of the disk (250KHz of WRITE DATA frequency for FD-55BR/FR and 500KHz for FD-55GR).

(6) Measure the average amplitude (Vp-p) of the read waveform as in Fig.3416.

(7) Calculate the read level by substituting the following expression with the measured value in item (6) and READ LEVEL calibration value (see level disk label).

$$\text{Read level (True value)} = \text{Measured value} \times \frac{100}{\text{Calibration value}} \ (\%)$$



(Fig.3416) Measurement of average read level (2F)

(8) Confirm that the true value of the read level is within the following range.

Innermost track read level, FD-55BR/GR: 800mVp-p, Min.
FD-55FR: 600mVp-p, Min.

(9) Execute items (5) through (8) for side 0 and side 1 heads respectively.

(10) If the value in item (8) or (9) is out of the specified range, following causes are assumed.

(a) Inferior disk:
Disk and/or jacket is deformed or damaged. Replace the level disk with a new one.

(b) Abnormal disk rotational speed:
Check for the speed according to item 3-4-6.

(c) Inferior head touch:
Check for the head touch according to item 3-4-8.

(d) Inferior head:
Replace the head carriage Ass'y according to item 3-5-1.

(e) Inferior PCBA MFD control:

Replace the PCBA MFD control according to item 3-5-7.

(11) Eject the level disk and release the Invert and Add modes of the oscilloscope.

(B-2) Check procedure (SKA method)

(1) Connect an SKA and check cable referring to item 3-2-4 and set the FD PWR switch to the PSA side.

(2) Install a level disk.

(3) Start the spindle motor by key "5". (MON indicator turns on).

(4) Execute drive select by key "0". (DS0 indicator turns on).

(5) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

(6) Key in "C1". (SEEK TMAX)

(7) Key in "D7". (WRITE/READ LEVEL DIF 2F)
Calibration value of the level disk should be set previously in the SKA.

(8) The DATA indicator, XXXX (mVo-p) indicates the average read level at TP7 and TP8 (Dif-amp.).

(a) When SKA3 is used:
By keying in "D7", side 0 and side 1 read levels are indicated on DATA 0 and DATA 1 indicators successively.

(b) When conventional SKA is used:
Depress key "4" (STOP) and then execute item (7) for side 0 and side 1 heads respectively. The side is changed alternately by a depression of "4" key. When side 1 is selected, SIDE 1 indicator of the SKA turns on.

(9) Confirm that both read levels are within the following range.

Innermost track read level, FD-55BR/GR: 400mVp-p, Min.
FD-55FR: 300mVo-p, Min.

(10) If the value in item (9) is out of the specified range, refer to item (10) of "General method".

(11) Eject the level disk.

3-4-11. Check of Resolution

(A) Equipment

(1) Level disk
(2) SKA or user's system
(3) Oscilloscope (not required when an SKA is used)

(B-1) Check procedure (General method)

(1) Use two channels of an oscilloscope and connect them to TP4 and TP5 (Pre-amp.) on the PCBA MFD control.
Oscilloscope range: AC mode, 20mV ∿ 0.1V
Set both channels, 1 and 2 to the above range. Set either of the channels to Invert mode and Add both channels.

(2) Install a level disk and start the spindle motor.

(3) Set the head to the innermost track.

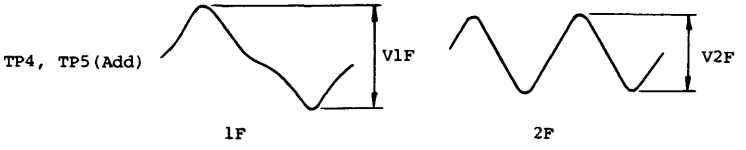
(4) Execute the head loading.

(5) Execute 1F write operation for one rotation of the disk (125KHz of WRITE DATA frequency for FD-55BR/FR and 250KHz for FD-55GR).

(6) Measure the average amplitude (V1F) as in Fig.3417.

(7) Execute 2F write operation like in item (5), doubled in frequency to that in item (5).

(8) Measure the average amplitude (V2F) as in Fig.3417.



(Fig.3417) Measurement of resolution

(9) Calculate the resolution by substituting the following expression with the measured values V1F, V2F, and RESOLUTION calibration value (see level disk label).

$$\text{Resolution (true value)} = \frac{V2F}{V1F} \times \frac{100}{\text{Calibration value}} \ (\%)$$

(10) Confirm that the true value of resolution is within the following range.

Innermost track resolution: 60%, Min.

(11) Execute items (5) through (10) for side 0 and side 1 heads respectively.

(12) If the value in item (10) or (11) is out of the specified range, following causes are assumed.

(a) Inferior disk:
Disk and/or jacket is deformed or damaged. Replace the level disk with a new one.

(b) Inferior disk rotational speed:
Check for the speed according to item 3-4-6.

(c) Inferior head touch:
Check for the head touch according to item 3-4-8.

(d) Inferior head:

Replace the head carriage Ass'y according to item 3-5-1.

(e) Inferior PCBA MFD control:

Replace the PCBA MFD control according to item 3-5-7.

(13) Eject the level disk and release the Invert and Add modes of the oscilloscope.

(B-2) Check procedure (SKA method)

(1) Connect an SKA and check cable referring to item 3-2-4 and set the FD PWR switch to the PSA side.

(2) Install a level disk.

(3) Start the spindle motor by key "5". (MON indicator turns on).

(4) Execute drive select by key "0". (DS0 indicator turns on).

(5) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

(6) Key in "C1". (SEEK TMAX)

(7) Key in "D8". (RESOLUTION)
Calibration value of the level disk should be set previously in the SKA.

(8) The DATA indicator, XXXX (%) indicates the resolution at TP4 and TP5 (Pre-amp.).

(a) When SKA3 is used:
By keying in "D8", side 0 and side 1 resolutions are indicated on DATA 0 and DATA 1 indicators successively.

(b) When conventional SKA is used:
Depress key "4" (STOP) and them execute item (7) for side 0 and side 1 heads respectively. The side is changed alternately by a depression of "4" key. When side 1 is selected, SIDE 1 indicator of the SKA turns on.

(9) Confirm that both resolution values are within the following range.

Innermost track resolution: 60%, Min.

(10) If the value in item (9) is out of the specified range, refer to item (12) of "General method".

(11) Eject the level disk.

3-4-12. Check and Adjustment of Track Alignment

(A) Equipment

(1) Cross point screwdriver, M3
(2) Alignment disk
(3) Alignment adjustment jig or M3 screw of 15mm long
(4) SKA or user's system
(5) Oscilloscope
(6) Hygrometer
(7) Locking paint

(B) Precaution for check and adjustment

(1) Environmental condition

Check and adjustment of track alignment should be done in an environment of room temperature of 20 ∿ 30°C (68 ∿ 86°F) and relative humidity of 40 ∿ 60%. Even if the environmental condition is within the specified operational condition, extreemly high or low temperature, or high or low humidity should be avoided. Check and adjustment should be done after two hours, Min. of storing the FDD and the alignment disk in the above mentioned condition. If the actual relative humidity is out of the above range and it is difficult to control, use the humidity calibration method in item (C) or (D).

(2) Orientation of the FDD

It is recommended that the orientation of the FDD for the track alignment check is the same as when the FDD is actually installed in the user's system.

(3) Alignment disk handling

(a) Confirm that the interface cable is correctly connected before power on to the FDD. If the odd numbered pins of the interface connector are connected to the even numbered pins, the data on the disk might be erased without a command from the host side. (There will be no damage to the FDD itself).

(b) Install and eject an alignment disk during power on of the FDD.

(c) Before installation, be sure to check that the write enable notch of the alignment disk is masked.

(d) The installation of an alignment disk to the FDD should be as less time as possible. Remove the disk immediately after the required check and adjustment.

(C) Check and adjustment procedure (General method)

(1) Use two channels of an oscilloscope and connect them to TP7 and TP8 (Differentiation amp.) on the PCBA MFD control. Also connect the external trigger of the oscilloscope to TP1 (Index) and apply positive trigger.
Oscilloscope range: AC mode, 0.2 ∿ 0.5V, 20msec
Set both channels, 1 and 2 to the above range. Set either of the channels to Invert mode and Add both channels.

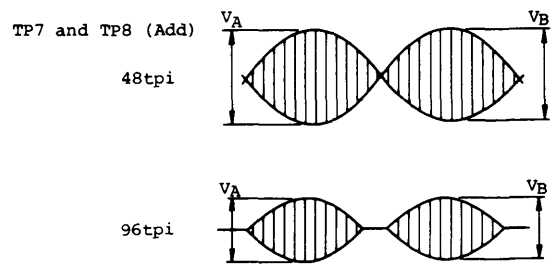
(2) Install an alignment disk and start the spindle motor.

(3) Execute the head loading.

(4) Set the head to the following alignment check track.

Alignment check track, 48tpi (FD-55BR): Track 16
96tpi (FD-55FR/GR): Track 32

(5) Confirm that two lobe patterns as in Fig.3418 can be observed (it is not necessary that the levels of VA and VB are equal).



(Fig.3418) Alignment check lobe pattern

If only one lobe pattern can be observed or if two lobes become one

pattern, the head is not on the alignment check track.
In such event, execute step-out or step-in for the following tracks' space to obtain the most similar waveform to that in Fig.3418.

48tpi: 2 tracks
96tpi: 4 tracks

Note: The above number of tracks to be stepped is required to make the alignment track position be fit with the magnetized condition of the basic phase "A" of the stepping motor. If the stepped track numbers are inassured, set it again from track 00 (TRACK 00 output signal goes to TRUE).
For a 48tpi FDD, the lobe pattern in Fig.3418 shall be observed at the even track, while it shall be observed at the track of multiple number of four for a 96tpi FDD.

(6) After one or several step-outs from the check track, step in the head to the check track again and measure VA and VB at that time.

(7) Calculate the true value of misalignment by substituting the value in item (6) and ALIGNMENT calibration value (see alignment disk label, attention to the side).

$$\text{Misalignment(true value)} = \left(\frac{\text{VA-VB}}{\text{Larger value in VA \& VB}} \times 100 - \text{Calibration value}\right) - (\text{Relative humidity}-50) \times K$$

"K" is humidity compensation factor.

48tpi: K=0.26
96tpi: K=0.42

e.g. 96tpi, VA=0.58V, VB-0.61V, Calibration value=-6(%)
Relative humidity= 65%:

$$\text{Misalignment(true value)} = \{\frac{0.58 \times 0.61}{0.61} \times 100-(-6)\} - (65-50)$$

$$\times 0.42 \simeq -5.2(\%)$$

If the calculated value is positive, the magnetic head is shifted inward from the reference position, while the head is shifted outward from the reference position when the value is negative.

(8) Conversely, measure VA and VB when the head is on the alignment check track by stepping-out after one or several step-ins.

(9) Calculate the true value of misalignment as described in item (7).

(10) Confirm that both of the calculated values in items (7) and (9) are within the following range.

True value of misalignment: 30%, Max.

(11) Execute items (4) through (10) for side 0 and side 1 heads respectively.

(12) If the value in item (10) or (11) is out of the specified range, adjust the track alignment according to the following procedure.

(a) Loosen the two fixing screws of the stepping motor a little.

(b) Insert the alignment adjustment jig of M3 screw from the back side of the FDD as shown in Fig.3419.

(c) Repeat step-in and step-out operations and adjust the misalignment to be the smallest on the alignment check track during both step-in and step-out operations by turning the jig or the screw (stepping motor moves little by little).

Note: When you adjust the alignment by observing the lobe pattern using the oscilloscope, pay attention to the calibration value on the alignment disk label and the ambient relative humidity.

i) Calibration value + (Relative humidity - 50) x k $\geq$ 0:
When the left side lobe pattern level, VA is assumed as "1", lobe pattern ratio should be so adjusted that the right side lobe pattern level VB takes the following value:

$$VB = 1 - \frac{\text{Calibration value} + (\text{Relative humidity} - 50) \times K}{100}$$

ii) Calibration value + (Relative humidity - 50) x K $\geq$ 0:
When the right side lobe pattern level, VB is assumed as "1", lobe pattern ratio should be so adjusted that the left side lobe pattern level VB takes the following value.

$$VA = 1 - \frac{\text{Calibration value} + (\text{Relative humidity} - 50) \times K}{100}$$

e.g. 96tpi, Calibration value = -6%, Relative humidity = 35%:

$$-6 + (35 - 50) \times 0.42 = -12.3 < 0$$

$$VA = 1 - \frac{-6 + (35 - 50) \times 0.42}{100} = 0.88$$

Therefore, the target value of VB when VB is assumed as "1" is 0.88.

(d) Repeat the adjusting operation in item (c) alternately for side 0 and side 1 heads until the both misalignment take the smallest value.

(e) Tighten the two fixing screws of the stepping motor little by little for adjusting the true value of misalignment after tightening the screws with the specified torque to be within ±20%.

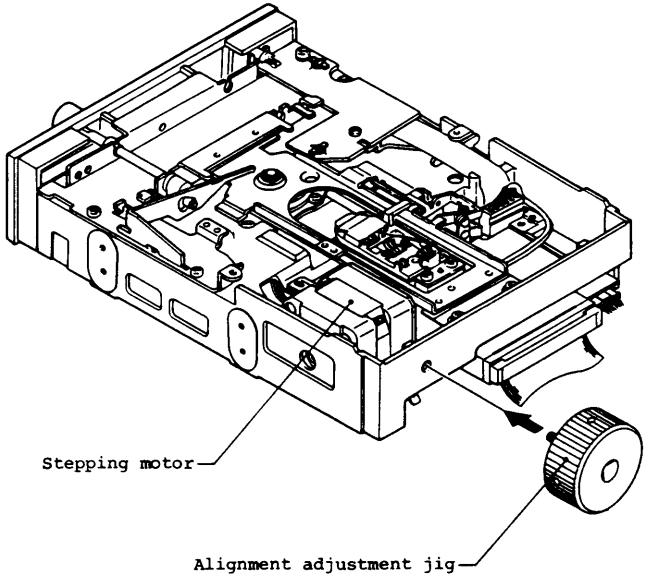
(f) Remove the alignment disk.

(g) Apply a drop of locking paint to the head of the stepping motor fixing screws.

(h) Check and adjust the track 00 sensor according to item 3-4-13.

(i) Check the track 00 stopper according to item 3-4-14.

(13) Release the Invert and Add modes of the oscilloscope.



(Fig.3419) Adjustment of track alignment

(D) Check and adjustment procedure (SKA method)

(1) Connect an SKA and check cable referring to item 3-2-4 and set the FD PWR switch to the PSA side.

(2) Use two channels of an oscilloscope. Connect the 1st channel to the DOUT terminal of the SKA and the 2nd channel to the DIF terminal of the SKA. Apply positive trigger by DOUT terminal.
Oscilloscope range, The 1st channel: DC mode, 2V, 20msec
The 2nd channel: AC mode, 0.2 ∿ 0.5V, 20msec

(3) Key in "B9 F". (INDEX observation)

(4) This item is applied only for 96tpi FDD (FD-55FR/GR) using a conventional SKA. Refer to item 3-2-4-7.
Key in "DD". (H GAIN indicator turns on).

(5) Install an alignment disk.

(6) Start the spindle motor by key "5". (MON indicator turns on).

(7) Execute drive select by key "0". (DS0 indicator turns on).

(8) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

(9) Set the head to the alignment check track by the following operation:

48tpi (FD-55BR): Key in "C2 16" and confirm that the TRACK indication becomes "16".
96tpi (FD-55FR/GR): Key in "C2 32" and confirm that the TRACK indication becomes "32".

(10) Confirm that two lobe patterns as in Fig.3418 can be observed by the

oscilloscope (it is not necessary that the levels of VA and VB are equal).

If only one lobe pattern can be observed or if two lobes become one pattern, the head is not on the alignment check track.

In such event, execute step-in or step-out of the following tracks' space to obtain the most similar waveform to that in Fig.3418. Step operation can be done by key "8" (STEP-IN) and key "9" (STEP-OUT). By a depression of these keys, head will move for one track space.

48tpi: 2 tracks
96tpi: 4 tracks

Note: The above number of tracks to be stepped in required to make the alignment track position be fit with the magnetized condition of the basic phase "A" of the stepping motor.
For a 48tpi FDD, the lobe pattern shall be observed at the even track, while it shall be observed at the track of multiple number of four for a 96tpi FDD.

(11) Key in "E3". (ALIGNMENT)
Calibration value of the alignment disk and environmental relative humidity should be set previously in the SKA.

(12) The DATA indicator, XXXX (%) indicates the misalignment value. + (+) mark means that the head is shifted inward from the reference position, while - mark means that the head is shifted outward.

(a) When SKA3 is used:
By keying in "E3", side 0 and side 1 values are indicated on DATA 0 and DATA 1 indicators successively. The initial digit indicates I (IN) or O (OUT). "IN" means the value after step-in operation, while "OUT" means the value after step-out operation.

(b) When conventional SKA is used:

Key in "0" following the operation of item (11). The side is changed alternately by a depression of "0" key during the execution of E3 command. When side 1 is selected, SIDE 1 indicator of the SKA turns on.

(13) Confirm that all the misalignment values are within the following range.

Misalignment value: Less than ±30%

(14) Depress "F" key. (STOP)

(15) If the value in item (13) is out of the specified range, adjust the track alignment according to the following procedure.

(a) Loosen the two fixing screws of the stepping motor a little.

(b) Insert the alignment adjustment jig or M3 screw from the back side of the FDD as shown in Fig.3419.

(c) Key in "E3" and adjust the jig or M3 screw so that the DATA indicator, XXXX (%) shows the smallest value. The stepping motor moves little by little when the jig or the screw is turned.

(d) Repeat the adjusting operation in item (c) alternately for side 0 and side 1 heads until the both misalignment take the smallest value. Refer to item (12).

(e) Tighten the two fixing screws of the stepping motor little by little to obtain the value within ±20% on the DATA indicator when the screws are tightened with the specified torque.

(f) Remove the alignment disk.

(g) Apply a drop of locking paint on the screw head of the stepping motor fixing screws.

(h) Check and adjust the track 00 sensor according to item 3-4-13.

(i) Check the track 00 stopper according to item 3-4-14.

(16) Release the Invert and Add modes of the oscilloscope.

(17) When the H GAIN indicator of the conventional SKA is on for a 96tpi FDD, key in "DD" again to turn off the indicator.

3-4-13. Check and Adjustment of Track 00 Sensor

(A) Equipment

(1) Cross point screwdriver, M3
(2) Work disk
(3) Alignment disk
(4) SKA or user's system
(5) Oscilloscope or digital voltmeter (not required when SKA3 is used)
(6) Locking paint

(B-1) Check and adjustment procedure (General method)

Note: Check and adjustment of the track 00 sensor using this general method is not so precise. It is recommended to use an SKA method as much as possible.

(1) Connect an oscilloscope or digital voltmeter to TP3 (Track 00 sensor) on the PCBA MFD control.
Oscilloscope range: DC mode, 1V

(2) Install a work disk and start the spindle motor.

(3) Execute the head loading

(4) Confirm that the voltage at TP3 is within the following range when the head is set to track 00.

Track 00 position TP3 voltage: 3.7V, Min.

(5) Turn the power off of the FDD and then turn it on again at the track 00 position. Confirm that the head carriage once moves to inner track and then it returns to track 00 position (auto-recalibration).

(6) Set the head to the following track.

48tpi (FD-55BR): Track 02
96tpi (FD-55FR/GR): Track 04

(7) Confirm that the voltage at TP3 is within the following range at the track position in item (6).

TP3 voltage at track 02 (48tpi) or 04 (96tpi): 0.5V, Max.

(8) If the value in item (4), (5), or (7) is out of the specified range, adjust the position of the track 00 sensor according to the following procedure.

(a) Connect the oscilloscope to TP7 or TP8 (Differentiation amp.) of the PCBA MFD control.
Oscilloscope range: AC mode, 0.2 ∿ 0.5V, 20msec

(b) Install an alignment disk. The track alignment should be previously adjusted according to item 3-4-12.

(c) Make the head move to the position where the lobe pattern as in Fig. 3418 can be observed.

(d) Remove the alignment disk.

(e) Connect the oscilloscope or digital voltmeter to TP3 (Track 00 sensor) on the PCBA MFD control.
Oscilloscope range: DC mode, 1V

(f) Step out the head for the following space from the position where the normal lobe pattern is observed.

48tpi: 15 tracks (the head will be on track 01)
96tpi: 30 tracks (the head will be on track 02)

(g) Install a work disk.

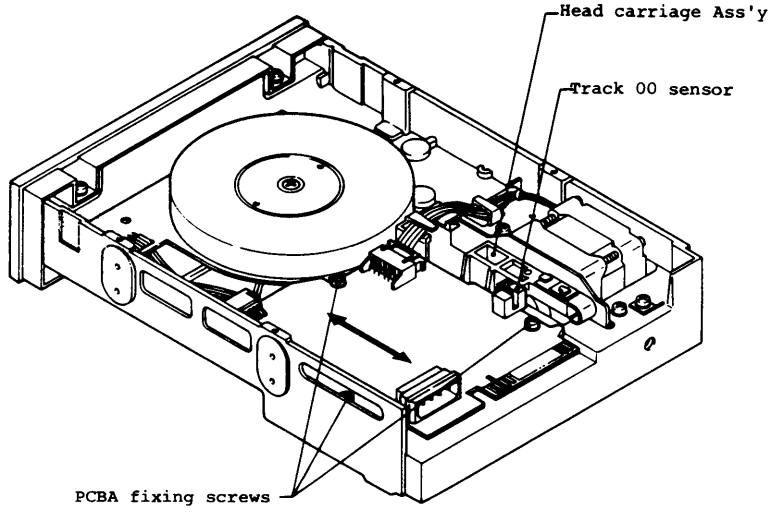
(h) Loosen the three fixing screws of the PCBA MFD control (see Fig.3420) and move the PCBA position a little so that the voltage at TP3 falls within the following range.

TP3 voltage at track 01 (48tpi) or track 02 (96tpi):
1V ∿ 3V (2V, approx. center)

(i) Confirm the items (4) through (7).

(j) Adjust the track 00 sensor position so that the values in items (h) and (i) satisfy the specification when the screws have been tightened with the specified torque (6Kg.cm).

(k) Check the track 00 stopper according to tiem 3-4-14.



(Fig.3420) Adjustment of track 00 sensor

(B-2) Check and adjustment procedure (Conventional SKA method)

(1) Connect an SKA and check cable referring to item 3-2-4 and set the FD PWR switch to the PSA side.

(2) Use two channels of oscilloscope and connect them as follows:

(a) The 1st channel: SKA DOUT terminal

(b) The 2nd channel: TP3 (Track 00 sensor) on PCBA MFD control, 2V range

(c) External trigger: DIRECTION SELECT interface signal (Interface connector pin No.18) or pin 3 of J3 (resistor network RA1 for terminator) on the PCBA MFD control, (+) trigger.

(3) Key in "B8 F". (STEP observation)

(4) Install a work disk and start the spindle motor by key "5". (MON indicator turns on).

(5) Execute drive select by key "0". (DS0 indicator turns on).

(6) Set the step rate and the settling time as follows referring to item 3-2-4-3.
FD-55BR, 6msec seek model: Step rate 6msec, Settling time 15msec
FD-55BR, 4msec seek model: Step rate 4msec, Settling time 10msec
FD-55FR/GR: Step rate 3msec, Settling time 15msec

(7) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

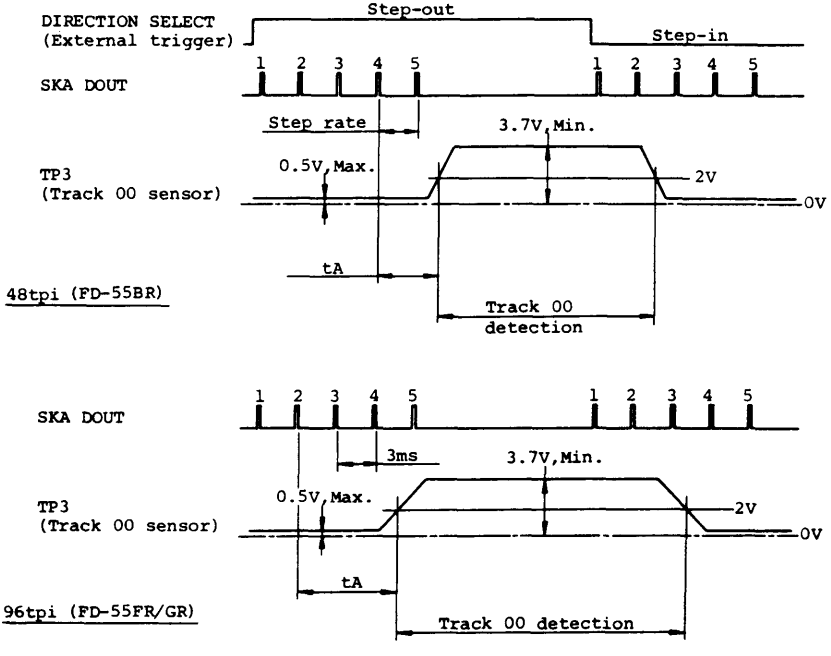
(8) Key in "C5". (T00 TIMING)

(9) Measure the timing, tA according to Fig.3421. tA shall be within the following range.

Track 00 detection timing:

FD-55BR (6msec seek model) and FD-55FR/GR: tA= 7.5 ± 1.5msec

FD-55BR (4msec seek model): tA= 6.3 ± 1.3msec



(Fig.3421) Track 00 sensor output waveform

(10) Key in "F". (STOP)

(11) Turn the FD PWR switch of the SKA off at the track 00 position and then set it again to the PSA side. Confirm that the head carriage once moves to inner track and then it returns to track 00 position

(auto-recalibration).

(12) If the value in item (9) or (11) is out of the specified range, adjust the position of the track 00 sensor according to the following procedure.

(a) Connect the 2nd channel of the oscilloscope to TP7 or TP8 (Differentiation amp.) of the PCBA MFD control and change the trigger to this channel.
Oscilloscope range: AC mode, 0.2 ∿ 0.5V, 20msec

(b) Install an alignment disk. The track alignment should be previously adjusted according to item 3-4-12.

(c) Key in "C0" and confirm that the track indicator becomes "00". (RECALIBRATE).

(d) Key in the following number and confirm that two lobe patterns as in Fig.3418 can be observed.
48tpi: C2 16
96tpi: C2 32

If normal lobe pattern cannot be observed, move the head to the track position where the typical lobe pattern can be observed by stepping in by key "8" or by stepping out by key "9".

(e) Remove the alignment disk.

(f) Key in the following number. (SET TRACK NUMBER)
48tpi: E4 16
96tpi: E4 32

(g) Key in "C2 00". (SEEK 00)
Don't key in "C0". (RECALIBRATE)

(h) Change the connection of the oscilloscope as in item (2).

(i) Key in "C5". (T00 TIMING)

(j) Loosen the three fixing screws of the PCBA MFD control (see Fig.3420) and move the PCBA position so that the track 00 detection timing falls within the specified range.

(k) Repeat the adjustment so that the timing satisfies the specification when the screws have been tightened with the specified torque (6Kg.cm).

(L) Check the track 00 stopper according to item 3-4-14.

(B-3) Check and adjustment procedure (SKA3 method)

(1) Connect the SKA3 and check cable referring to item 3-2-4 and set the FD PWR switch to the PSA side.

(2) Install a work disk.

(3) Start the spindle motor by key "5". (MON indicator turns on).

(4) Execute drive select by key "0". (DS0 indicator turns on).

(5) Set the step rate and the settling time as follows referring to item 3-2-4-3.

FD-55BR, 6msec seek model: Step rate 6msec, Settling time 15msec
FD-55BR, 4msec seek model: Step rate 4msec, Settling time 10msec
FD-55FR/GR: Step rate 3msec, Settling time 15msec

(6) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

(7) FD-55BR, 6msec seek model: Key in "C5". (T00 TIMING)
FD-55BR, 4msec seek model: Key in "C5A" (T00 TIMING, 4msec model)
FD-55FR/GR: Key in "C5". (T00 TIMING)

(8) Confirm that DATA 0 indicator, XXXX (ms) indicates a value within the following range. Value on DATA 1 indicator must be ignored.

Track 00 detection timing
FD-55BR (6msec seek model): DATA 0 = 7.5 ± 1.5msec
FD-55BR (4msec seek model): DATA 0 = 6.3 ± 1.3msec
FD-55FR/GR: DATA 0 = 7.5 ± 1.5msec

(9) Depress "F" key. (STOP)

(10) Turn the FD PWR switch of the SKA3 off at the track 00 position and then set it again to the PSA side. Confirm that the head carriage once moves to inner track and then it returns to the track 00 position (auto-recalibration).

(11) If the value in item (8) or (10) is out of the specified range, adjust the position of the track 00 sensor according to item (B-2)-(12), conventional SKA method excluding the step (h).

3-4-14. Check of Track 00 Stopper

(A) Equipment

(1) SKA or user's system

(B-1) Check procedure (General method)

(1) Set the head to track 00.

(2) Step out the head from the track 00 position.

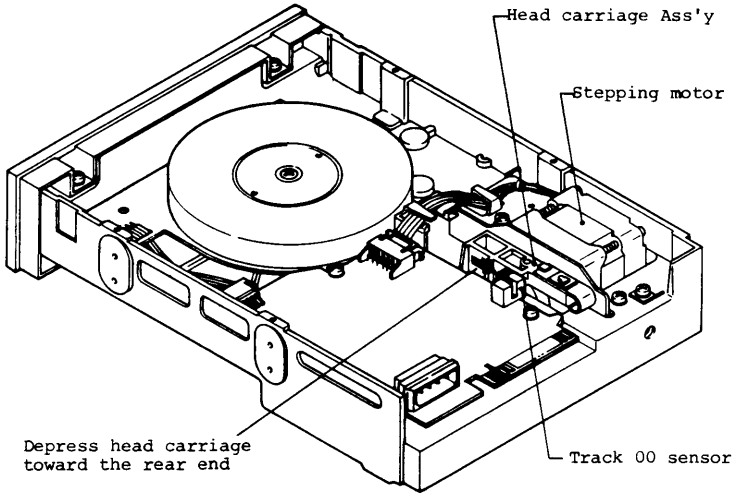
(3) Confirm that the head carriage does not move by the step-out command (head carriage rests on track 00).

(4) Repeat step-in and step-out operations between track 00 and track XX. Confirm that no impact sound can be heard between the head carriage and the other fixing parts (track 00 stopper).

(5) Turn off the FDD power and depress the head carriage lightly toward the rear end of the FDD with fingers. Refer to arrow mark in Fig.3422.

(6) Turn on the FDD power. Confirm that the head carriage once moves to inner track automatically and then it returns to track 00 position.

(7) Confirm that the TRACK 00 output signal is LOW during DRIVE SELECTed.



(Fig.3422) Check of track 00 stopper

(B-2) Check procedure (SKA method)

(1) Connect an SKA referring to item 3-2-4 ans set the FD PWR switch to the PSA side.

(2) Execute drive select by key "0". (DS0 indicator turns on).

(3) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

(4) Set the step rate and the settling time as follows referring to item 3-2-4-3.
FD-55BR (6msec seek model): Step rate 6msec, Settling time 15msec
FD-55BR (4msec seek model): Step rate 4msec, Settling time 10msec
FD-55FR/GR: Step rate 3msec, Settling time 15msec

(5) Key in "9". (STEP OUT)

(6) Confirm that the head carriage does not move even if "9" is keyed in (head carriage rests on track 00).

(7) Key in "C0" and key in "C5". (STEP TIMING)

(8) Confirm that no impact sound can be heard between the head carriage and the other fixing parts (track 00 stopper).

(9) Turn off the FD PWR switch of the SKA and depress the head carriage lightly towards the rear end of the FDD with fingers. Refer to arrow mark in Fig.3422.

(10) Turn on the FD PWR switch again. Confirm that the head carriage once moves to inner track automatically and then it returns to track 00 position.

(11) Confirm that the T00 indicator of the SKA is on.

3-4-15. Check and Adjustment of Index Burst Timing

(A) Equipment

(1) Cross point screwdriver, M3
(2) Alignment disk
(3) SKA or user's system
(4) Oscilloscope (not required when an SKA is used)

(B-1) Check and adjustment proceudre (General method)

(1) Use two channels of an oscilloscope. Connect the 1st channel to TP1 (index) on the PCBA MFD control and the 2nd channel to TP4 or TP5 (Pre-amp.). Apply positive trigger by TP1.

Oscilloscope range, The 1st channel: DC mode, 2V, 50μsec
The 2nd channel: AC mode, 0.5V, 50μsec

(2) Install an alignment disk and start the spindle motor.

(3) Execute the head loading.

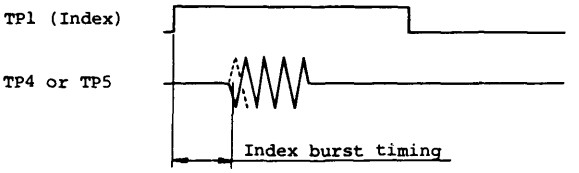
(4) Set the head to the following track:

48tpi (FD-55BR): Track 01
96tpi (FD-55FR/GR): Track 02

(5) Measure the index burst timing in Fig.3423.

(6) Substitute the following equation with the measured value in item (5) and INDEX TIMING calibration value (see alignment disk label).

Index burst timing (true value) = Measured value - Calibration value (μs)



(Fig.3423) Index burst timing

(7) Confirm that the true value of the index burst timing is within the following range.

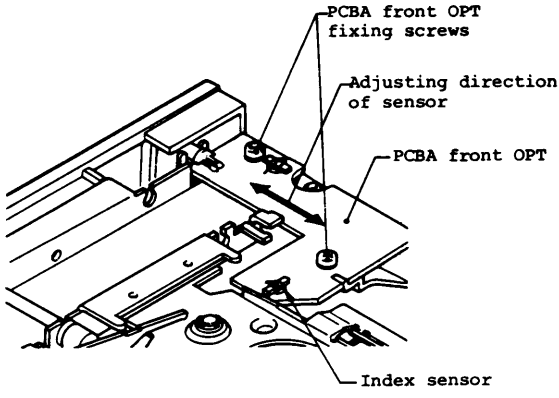
Index burst timing, FD-55BR/FR: 200 ± 200μsec
FD-55GR: 165 ± 165μsec

(8) If the value in item (7) is out of the specified range, adjust the index sensor position according to the following procedure.

(a) Loosen the two fixing screws (see Fig.3424) of the PCBA front OPT and adjust its position to make the true value of the index burst timing fall in the specified range in item (7).

(b) Repeat the adjustment so that the true value of the index burst timing falls in the range of item (7) when the fixing screws have been tightened with the specified torque (4.5Kg.cm).

(9) Remove the alignment disk.



(Fig.3424) Adjustment of index sensor

(B-2) Check and adjustment procedure (SKA method)

(1) Connect an SKA and check cable referring to item 3-2-4 and set the FD PWR switch to the PSA side.

(2) Install an alignment disk.

(3) Start the spindle motor by key "5". (MON indicator turns on).

(4) Execute drive select by key "0". (DS0 indicator turns on).

(5) Key in "C0" and confirm that the TRACK indicator becomes "00". (RECALIBRATE)

(6) Set the head to the index check track by the following operation:

48tpi (FD-55BR): Key in "C2 01" and confirm that the TRACK indication becomes "01".
96tpi (FD-55FR/GR): Key in "C2 02" and confirm that the TRACK indication becomes "02".

(7) Key in "E6". (INDEX TIMING)
Calibration value of the index timing should be set previously in the SKA.

(8) Confirm that the DATA indicator, XXXX (μs) indicates the value within the following range.

Index burst timing, FD-55BR/FR: 200 ± 200μsec
FD-55GR: 165 ± 165μsec

(9) Key in "F". (STOP)

(10) If the value in item (8) is out of the specified range, adjust the

index sensor position according to the following procedure.

(a) Loosen the two fixing screws (see Fig.3424) of the PCBA front OPT and its position so that the DATA indication under execution of item (7) shows the median value in the specified range of item (8).

(b) Repeat the adjustment so that the DATA indication takes the median value when the fixing screws have been tightened with the specified torque (4.5Kg.cm).

(c) Depress "F" key. (STOP)

(11) Remove the alignment disk.

3-5. MAINTENANCE PARTS REPLACEMENT

3-5-1. Replacement of Head Carriage Ass'y

(A) Equipment

(1) Cross point screwdriver, M3
(2) Common screwdriver, small size
(3) A pair of tweezers
(4) Alcohol and gauze
(5) Locking paint
(6) Oil (FLOIL 946P)
(7) SKA or user's system
(8) Required equipment for each referring item

(B) Replacement procedure

(1) Disconnect the head connector (J4).

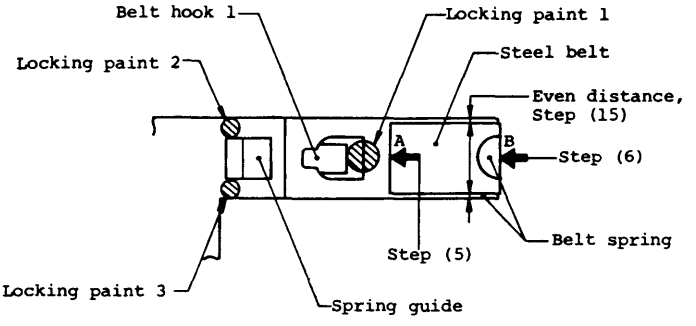
(2) Remove the set arm sub Ass'y (Fig.405, No.3) by removing two fixing screws (Fig.405, S8).

(3) Apply alcohol to locking paint areas on the head carriage. There are four points of shaded area as shown in Fig.3501 and Fig.3502.

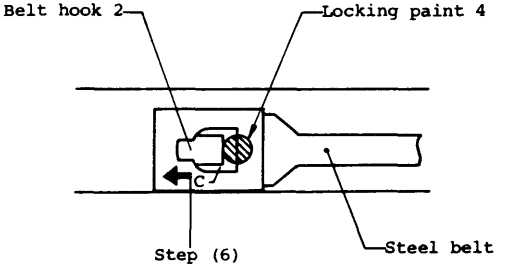
(4) Wait a minute.

(5) Turn the FDD over so that the spindle motor (bottom side) goes up. Depress A point of the steel belt (Table 402C, No.23c) according to Fig.3501 in the direction of arrow mark using a common screwdriver or rear end of a pair of tweezers, to make the locking paint 1 free.

(6) Depressing B area of the belt spring (Table 402C, No.23d) according to Fig.3501 with fingers in the direction of arrow mark, remove the steel belt from the belt hook 1 of the carriage using a pair of tweezers.



(Fig.3501) Belt hook area in the back side of carriage



(Fig.3502) Belt hook area on the upper side of the carriage

(7) Make the belt spring slide in the reverse direction of the arrow mark in Fig.3501 using a pair of tweezers, and make the locking paint 2 and 3 free. Then remove the belt spring from the spring guide of the carriage.

(8) Place the FDD so that the top side comes up. Pull C point of the steel belt in the direction of arrow mark in Fig.3502 using a pair of tweezers to make the locking paint 4 free. Then remove the steel belt from the

belt hook 2 of the carriage.

(9) Remove three screws (Fig.405, S1) to remove the spring guides A and B (Fig.405, Nos.24 & 25) which fix two guide shafts (Table 402C, No.23b).

(10) Remove the head carriage Ass'y with the guide shafts. Refer to Fig. 3503.

(11) Remove a screw (Fig.405, S1) on the capstan of the stepping motor Ass'y and remove the steel belt and the plate washer (Fig.405, No.26).

(12) Fix a new steel belt (accessory of the carriage) temporarily to the capstan with the plate washer and the screw in item (11) as they were.

Notes: 1. Fundamentally, the steel belt and the belt spring should be replaced with the head carriage. However, if there is no inferior points for these belt and spring, they may be used after cleaning the surface carefully with alcohol and gauze.

2. Pay attention not to damage the surface of the steel belt or the capstan.

(13) Install a new head carriage Ass'y with two guide shafts in the reverse order of items (5) through (10).
When fixing the steel belt to the carriage, install the belt spring at the bottom side first, and hook the steel belt to the belt hook 1. Refer to Fig.3501.
Then place the FDD with the top side up. Pull the steel belt in the direction of arrow mark in Fig.3502 using a pair of tweezers and hook it to the belt hook 2.

Note: When replacing the head carriage Ass'y, replace the two guide shafts at the same time because of matching the respective hole diameter of the carriage with those of the guide shafts. Each

guide shaft is to be designated in combination with corresponding hole of the head carriage Ass'y.
Guide shaft which goes through the hole of the carriage smoothly with a little clearance is considered to be the best.

(14) After finishing the installation of the carriage, loosen the screw which fixes the steel belt to the capstan temporarily.

(15) Confirm that the steel belt runs on the center of the belt spring referring to Fig.3501.

(16) After moving the head carriage several times manually, tighten the fixing screw of the steel belt in item (14) carefully with the specified torque of 4.5Kg.cm. At this time, be careful that the belt is tensioned straightly. Pay attention not to damage the surface of the belt or the capstan.

Note: Do not pinch the upper arm of the head carriage when move it manually. Pinch the rear side of the carriage.

(17) Move the head carriage to the middle of movable area and apply a drop of oil (FLOIL 946P) on three points of guide shafts' surface near the shaft holes of the carriage. This item shall be omitted, if the oil has been already applied.

Notes: 1. A small drop of oil shall be applied to each point.
For example, dip the tip of a narrow object such as wire or a pair of tweezers with oil.

2. If the head carriage or the head piece is smeared with oil, wipe it out completely by such a cotton swab dipped with alcohol.

(18) Make the head carriage move manually several times to spread the oil on all over the moving area.

(19) Apply a drop of locking paint to four points between the steel belt and the carriage referring to locking paint 1 through 4 in Figs. 3501 and 3502.

(20) Install the set arm and the head cable according to the reverse order of items (1) and (2). Refer to item 3-2-3 as to the head cable treatment.

(21) Adjust the set arm position according to item 3-4-1.

(22) Model with head load solenoid:
Check and adjust the arm lifter according to item 3-4-3.

CSS model:
Check the CSS Ass'y according to item 3-4-4.

(23) Make the head move continuously between the track 00 and the innermost track and confirm that the steel belt does not meander nor undulate. When an SKA is used, key in "C6" for this check and key in "F" for stop.

Note: If the steel belt is replaced with a new one, continue the head seek operation in item (23) for 3 minutes, approx.

(24) Check the head touch according to item 3-4-8.

(25) Check the asymmetry according to item 3-4-9.

(26) Adjust the track alignment according to item 3-4-12.

(27) Adjust the track 00 sensor position according to item 3-4-13.

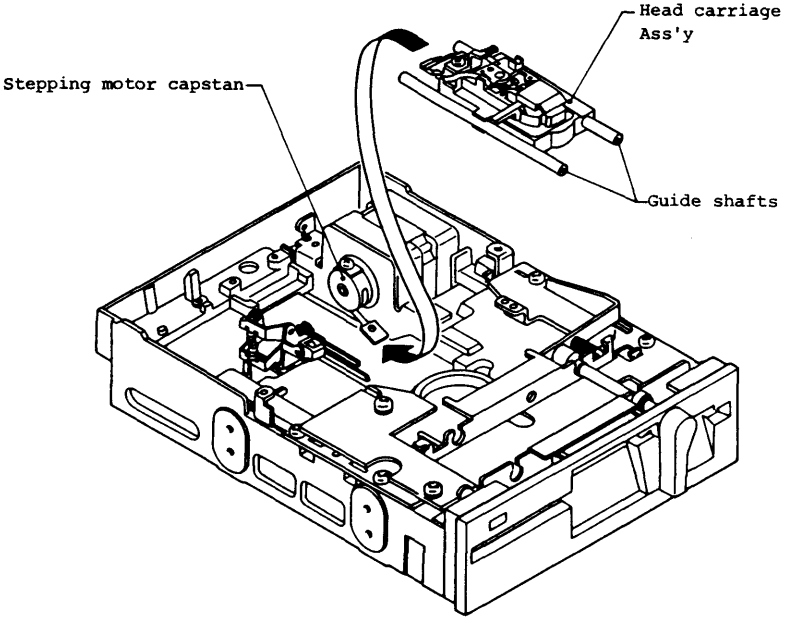
(28) Check the track 00 stopper according to item 3-4-14.

(29) Check or adjust the index burst timing according to item 3-4-15.

(30) Check the read level according to item 3-4-10.

(31) Check the resolution according to item 3-4-11.

(32) It is recommended to connect the FDD to the system for overall test.
Refer to item 3-2-5 (1) for the window margin test.



(Fig.3503) Replacement of head carriage Ass'y

3-5-2. Replacement of Stepping Motor Ass'y

(A) Tools

(1) Cross point screwdriver, M3
(2) A pair of tweezers
(3) Alcohol and gauze
(4) Locking paint
(5) SKA or user's system
(6) Required equipment for rach referring item

(B) Replacement procedure

(1) Disconnect the stepping motor connector (J6).

(2) Remove the stepping motor cable from the cable hooks of the frame to make the cable be free.

(3) Remove the steel belt (Table 402C, No.23c) and the belt spring (Table 402C, No.22d) according to item 3-5-1 (3) through (8).

(4) Remove two fixing screws (Fig.405, S9) of the stepping motor Ass'y (Fig.405, No.27) and remove the stepping motor with the steel belt.

(5) Remove a screw (Fig.405, S1) on the capstan of the stepping motor and remove the steel belt and the plate washer (Fig.405, No.26).

(6) Confirm that there is no inferior nor defective point for the steel belt and belt spring. Then carefully clean the surface of the steel belt, belt spring and capstan with alcohol and gauze.
If an inferior or defective point is found, replace the steel belt or the belt spring with a new one.

(7) Fix the steel belt temporarily to the capstan of a new stepping motor

with the plate washer and the screw as they were.

Note: Never remove the plate of the stepping motor Ass'y since they are combined each other.

(8) Install the stepping motor in item (7) according to the reverse order of items (1) through (4).

When fixing the steel belt to the carriage, install the belt spring at the bottom side first and hook the steel belt to the belt hook 1 (refer to Fig.3501).
Then place the FDD with the top side up. Pull the belt in the direction of arrow mark in Fig.3502 using a pair of tweezers and hook it to the belt hook 2.

(9) Loosen the screw which fixes the steel belt to the capstan.

(10) Confirm that the steel belt runs on the center of the belt spring when viewed from the bottom side. Refer to Fig.3501.

(11) After moving the head carriage several times manually, tighten the fixing screw of the steel belt in item (9) carefully with the specified torque of 4.5Kg.cm. At this time, be careful so that the belt is tensioned straightly. Pay attention not to damage the surface of the belt or the capstan.

Note: Do not pinch the upper arm of the head carriage when move it manually. Pinch the rear side of the carriage.

(12) Make the head move continuously between the track 00 and the innermost track and confirm that the steel belt does not meander nor undulate. When an SKA is used, key in "C6" for this check and key in "F" for stop. If there is some abnormal running of the steel belt, readjust the belt with screws in item (9). After the adjustment tighten the

screws carefully with the specified torque of 4.5Kg.cm.

Note: If the steel belt is replaced, execute the continuous seek operation in item (12) for 3 minuites, approx.

(13) Adjust the track alignment according to item 3-4-12.

(14) Adjust the track 00 sensor position according to item 3-4-13.

3-5-3. Replacement of DD motor Ass'y (Spindle Motor)

(A) Tools

(1) Cross point screwdriver, M3
(2) Common screwdriver, small size
(3) A pair of tweezers
(4) Locking paint
(5) SKA or user's system
(6) Required equipment for each referring item

(B) Replacement procedure

(1) Disconnect the spindle motor connector (J7).

(2) Remove three fixing screws (Fig.405, S5) of the DD motor Ass'y from the upper side of the FDD and draw out the DD motor Ass'y from the rotor side (PCBA side).

(3) Install a new DD motor Ass'y in the reverse order of items (1) and (2). Refer to item 3-2-2-5 as to the handling of J7 connector.

Note: The spindle area of the DD motor (clamping cup of the disk) is precisely machined. For installing the motor to the frame, place the spindle in parallel to the frame and push into the frame slowly. Handle the spindle very carefully not to damage the spindle surface.

(4) Adjust the set arm position according to item 3-4-1.

(5) Check the file protect sensor according to item 3-4-5.

(6) Check the disk rotational speed according to item 3-4-6.

(7) Adjust the track alignment according to item 3-4-12.

(8) Check or adjust the track 00 sensor position according to item 3-4-13.

(9) Check or adjust the index burst timing according to item 3-4-15.

3-5-4. Replacement of Collet Ass'y

(A) Equipment

(1) Cross point screwdriver, M3
(2) A pair of tweezers
(3) Round nose pliers
(4) Locking paint
(5) SKA or user's system
(6) Required equipment for each referring item

(B) Replacement procedure

(1) Remove the set arm sub Ass'y (Fig.405, No.3) by removing two fixing screws (Fig.405, S8).

(2) Remove an E-ring (Fig.405, S12) which fixes the collet Ass'y (Fig.405, No.9) to the set arm and remove the collet and the pressure spring (Fig.405, No.10).

(3) Install a new collet Ass'y in the reverse order. Pay attention to the orientation of the spring. The smaller diameter side shall face the collet side and the larger diameter side shall face the set arm side.

(4) Adjust the set arm position according to item 3-4-1.

(5) Check (or adjust) the track alignment according to item 3-4-12.

3-5-5. Replacement of Head Load Solenoid

This item is applied only for a model with head load solenoid Ass'y.

(A) Tools

(1) Cross point screwdriver, M3
(2) Hexagon wrench key, 1.5mm
(3) A pair of tweezers
(4) Locking paint
(5) SKA or user's system
(6) Required equipment to each referring item

(B) Replacement procedure

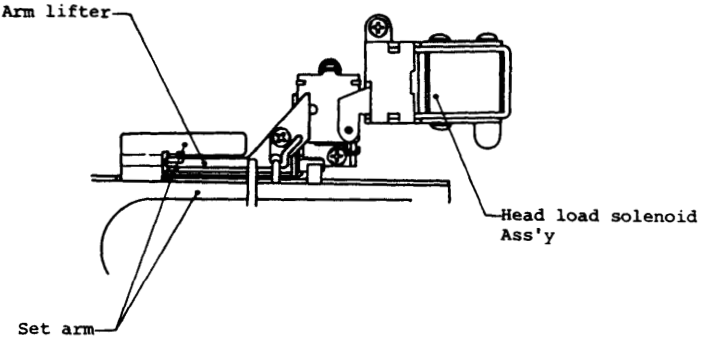
(1) Disconnect the head load solenoid connector (J8).

(2) Remove two fixing screws (Fig.405, S2) to remove the head load solenoid Ass'y (Fig.405, No.20).

(3) Install a new head load solenoid Ass'y in the reverse order.

(4) Position the head load solenoid Ass'y so that the arm lifter is in parallel with the set arm. Refer to Fig.3504.

(5) Check and adjust the arm lifter according to item 3-4-4.



(Fig.3504) Installation of the head load solenoid Ass'y

3-5-6. Replacement of CSS Ass'y

This item is applied only for a CSS model (without head load solenoid).

(A) Tools

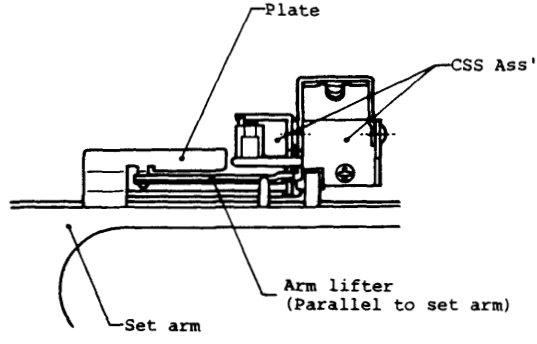
(1) Cross point screwdriver, M3
(2) Required equipment for each referring item

(B) Replacement procedure

(1) Remove a fixing screw (Fig.405, S2) to remove the CSS Ass'y (Fig.405, No.21) from the frame.

(2) Install a new CSS Ass'y in the reverse order. Be careful to install the arm lifter area to be in parallel to the set arm.

(3) Check the CSS Ass'y according to item 3-4-4.



(Fig.3505) CSS Ass'y and shift lever position

3-5-7. Replacement of PCBA MFD Control

(A) Tools

(1) Cross point screwdriver, M3
(2) Common screwdriver, small size
(3) SKA or user's system
(4) Required equipment for each referring item

(B) Replacement procedure

(1) Disconnect all of the connectors connected to the PCBA MFD control (Fig.405, No.29) referring to item 3-2-2.

(2) Remove the PCBA MFD control by removing three fixing screws (Fig.405, S3).

(3) Install a new PCBA in the reverse order.

(4) Set the straps and terminator as they were on the old PCBA.

(5) Check the file protect sensor according to item 3-4-5.

(6) Check the erase gate delay according to item 3-4-7.

(7) Check (or adjust) the asymmetry according to item 3-4-9.

(8) Check the read level according to item 3-4-10.

(9) Check the resolution according to item 3-4-11.

(10) Adjust the track 00 sensor position according to item 3-4-13.

(11) Check the index burst timing according to item 3-4-15.

(12) It is recommended to connect the FDD to the system for overall test. Refer to items 3-2-5 (1) for the window margin test.

3-5-8. Replacement of PCBA Front OPT

(A) Tools

(1) Cross point screwdriver, M3

(2) SKA or user's system

(3) Required equipment for each referring item

(B) Replacement procedure

(1) Disconnect PCBA front OPT connector (J5).

(2) Remove two fixing screws (Fig.405, S7) to remove the PCBA front OPT (Fig.405, No.30).

(3) Install a new PCBA in the reverse order.

(4) Check the file protect sensor according to item 3-4-5.

(5) Adjust the index burst timing according to item 3-4-15.

(6) Check the front bezel indicator.

3-5-9. Replacement of Front Bezel Ass'y

(A) Tools

(1) Cross point screwdriver, M3
(2) Required equipment for each referring item

(B) Replacement procedure

(1) Draw out the front lever Ass'y (Fig.405, No.32).

(2) Remove two fixing screws (Fig.405, S8) of the front bezel Ass'y (Fig. 405, No.31) and draw the front bezel out.

(3) Install a new front bezel Ass'y in the reverse order. For the installation of the front bezel, press the longitudinal ends of the bezel against the frame and tighten the fixing screws with the specified torque.

(4) Insert the front lever Ass'y fully against the lever shaft as it was.

3-5-10. Replacement of Front Lever Ass'y

(A) Tools

(1) Required equipment for each referring item

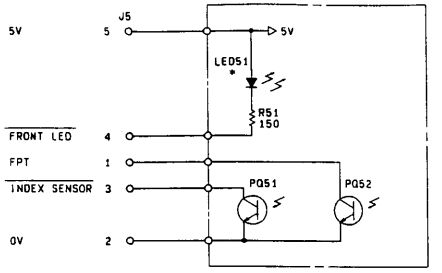
(B) Replacement procedure

(1) Draw out the front lever Ass'y (Fig.405, No.32).

(2) Insert a new front lever Ass'y fully against the lever shaft as it was.

(3) Check (or adjust) the holder position according to item 3-4-2.

部番	品番	図番	品名・文字	指定	備考	適用



PCBA VERSIONS	MAIN SPEC	* PARTS
15532091-00	STD	LED51(RED)
15532091-01	STD	LED51(GREEN)
15532091-07	STD	LED51(GREEN)
15532091-10	STD	LED51(AMBER)

VERSION TABLE

NOTES: ABBREVIATED NAMES ARE AS FOLLOWS.
RED, GREEN, AMBER : FRONT LED COLOR

P/N 15532091-XX(PCB ISSUE A~)

記号	改訂番号	年月日	担当	承認
承認			尺度	
検図				
設計			第三角法	
製図		87-05-28	単位 mm	

材料
仕上 指定以外のエッジはイトメのこと
処理
普通寸法差 TS-E_____(級)

TEAC ティアック株式会社
形式 FD-55R
品名 PCBA FRONT OPT#N
図名 SCHEMATIC
図番

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JKW1 KATAYO FILE:55RFOPT#NSTO.1118

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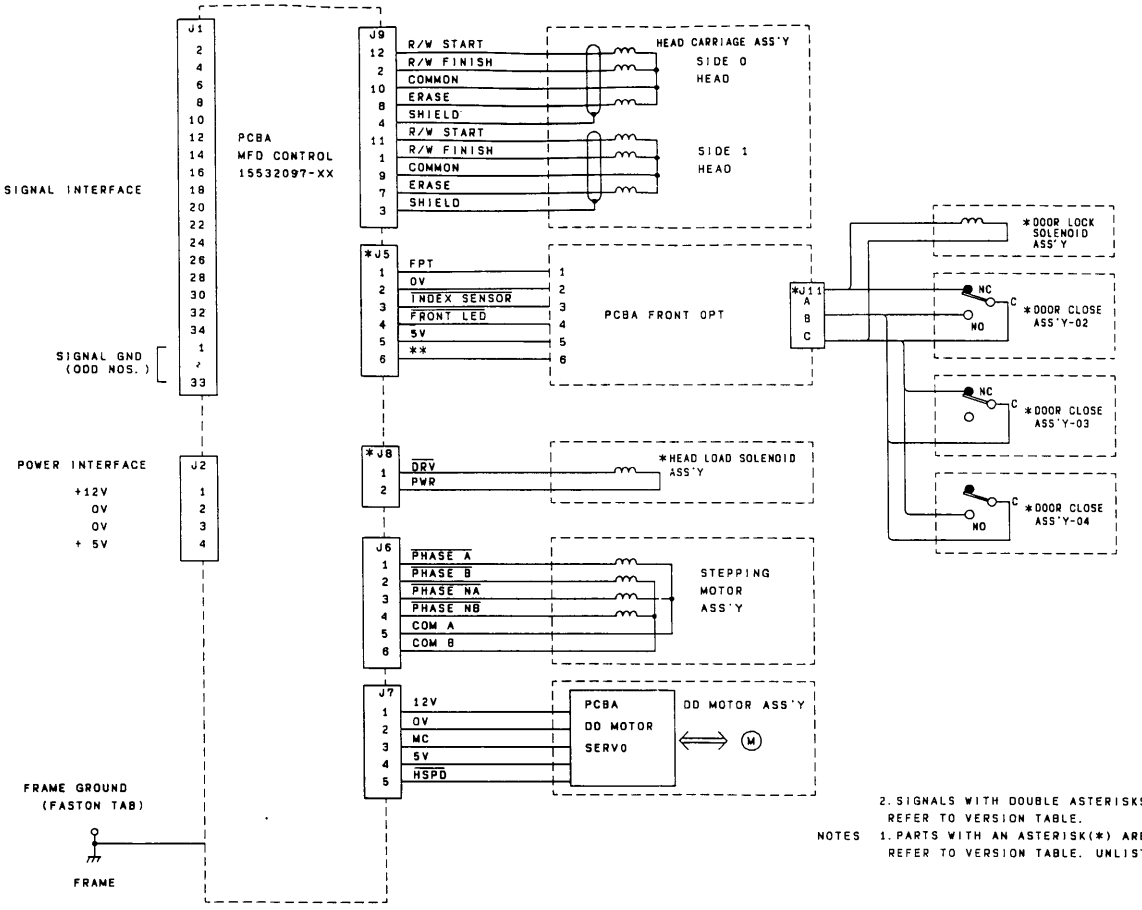

2. SIGNALS WITH DOUBLE ASTERISKS(**) ARE USED ONLY FOR OPTIONAL VERSIONS. REFER TO VERSION TABLE.

NOTES 1. PARTS WITH AN ASTERISK(*) ARE USED IN SOME FDD VERSIONS. REFER TO VERSION TABLE. UNLISTED PARTS ARE NOT USED IN THAT VERSION.

P/N 1930727X-XX

部品番号	品番	図番	品名・定格	個数	備考	適用

記号	改訂番号	年月日	担当	承認

材料		TEAC ティアック株式会社	
仕上	指定以外のエッジはイトメのこと	形式	FD-55BR/FR/GR
処理		品名	TOTAL DIAGRAM
普通寸法差	TS-E (級)	図名	
		図番	

未認	検図	設計	製図	尺度	第三角法	単位 mm
			87·05·28			

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10010230-01

部番	品番	図番	品名・文字	指定	備考	適用

TYPICAL FDD VERSION	MAIN SPEC	* PARTS	PCBA VERSION			** SIGNALS
			MFD CONTROL	FRONT OPT 15532091-XX	FRONT OPT 15532092-XX	
BR-500. BR-528. ETC	CSS. FULL STRAP		-00	LED COLOR RED :-00 GREEN:-01 AMBER:-10		
BR-501. BR-505. ETC	HL . FULL STRAP	HL ASS'Y	-01			
BR-502. BR-506. BR-578. ETC	CSS. HALF STRAP		-02			
BR-503. ETC	HL . HALF STRAP	HL ASS'Y	-03			
BR-504. ETC	CSS. MINI STRAP		-04			
FR-510. ETC	CSS. FULL STRAP		-05			
FR-511. ETC	HL . FULL STRAP	HL ASS'Y	-06			
FR-512. ETC	CSS. HALF STRAP		-07			
FR-513. ETC	HL . HALF STRAP	HL ASS'Y	-08			
BR-523	CSS. FULL STRAP. CUSTOM		-11	-10		
BR-320	CSS. HALF STRAP. CUSTOM		-12	-00		
BR-565	HL . FULL STRAP. CUSTOM	HL ASS'Y	-15	-01		
FR-582	HL . FULL STRAP. CUSTOM	HL ASS'Y DL SOL. ASS'Y	-16	-03		
FR-576. ETC	CSS. FULL STRAP. DRIVE STATUS	DC ASS'Y -03	-17	-04		J5-6:DC SENSOR
FR-558. FR-559	CSS. FULL STRAP. CUSTOM	DC ASS'Y -02	-18		-04	J5-6:D SEN

VERSIONS TABLE

TYPICAL FDD VERSION	MAIN SPEC	* PARTS	PCBA VERSION			** SIGNALS
			MFD CONTROL	FRONT OPT 15532091-XX	FRONT OPT 15532092-XX	

NOTE : ABBREVIATED NAMES ARE AS FOLLOWS :

HL	:	HEAD LOAD SOLENOID
CSS	:	WITHOUT HL SOLENOID
DC	:	DOOR CLOSE
DL	:	DOOR LOCK
DL SOL	:	DOOR LOCK SOLENOID
D SEN	:	DISK SENSOR

P/N 1930727X-XX

記号	改訂番号	年月日	担当	承認
承認				
検図				
設計				
製図		87·05·28		

材料
仕上 指定以外のエッジはイトメのこと
処理
普通寸法差 TS-E (級)
尺度
第三角法
単位 mm

TEAC ティアック株式会社

形式	FD-55BR/FR/GR
品名	TOTAL DIAGRAM
図名	
図番	

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部番	品番	図番	品名 変更	指示	備考	適用

TYPICAL FDD VERSION	MAIN SPEC	* PARTS	PCBA VERSION			** SIGNALS
			MFD CONTROL	FRONT OPT		
				15532091-XX	15532092-XX	

VERSIONS TABLE

TYPICAL FDD VERSION	MAIN SPEC	* PARTS	PCBA VERSION			** SIGNALS
			MFD CONTROL	FRONT OPT		
				15532091-XX	15532092-XX	

P/N 1930727X-XX

記号	改訂番号	年 月 日	担当	承認
承認			R度	
検図				
設計			第三角法	
製図		87·05·28	単位 mm	

材料		TEAC ティアック株式会社	
仕上	指定以外のエッジはイトメのこと	形式	FD-55BR/FR/GR
処理		品名	TOTAL DIAGRAM
普通寸法差	TS-E_____(級)	図名	
		図番	

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M P

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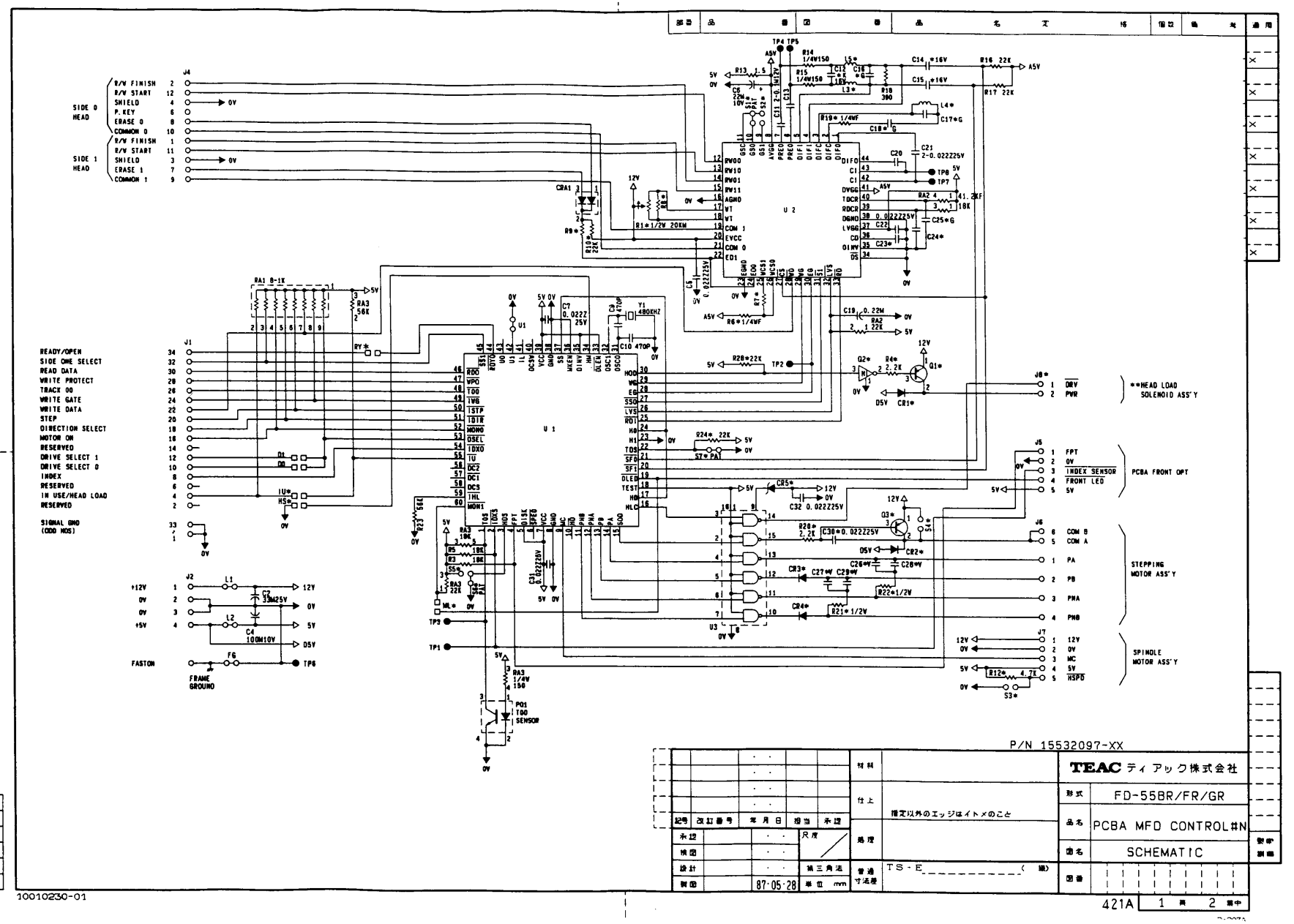
TEAC ティアック株式会社
FD-55BR/FR/GR
PCBA MFD CONTROL#N
SCHEMATIC
P/N 15532097-XX
421A
10010230-01
JKV1 KATAYO FILE:55BFRMFDN#X/DHST.112B
JKV1 KATAYO FILE:55BFRMFDN#X/DHST.212B
87-05-28
TS-E
READY/OPEN
SIDE ONE SELECT
READ DATA
WRITE PROTECT
TRACK 00
WRITE GATE
WRITE DATA
STEP
DIRECTION SELECT
MOTOR ON
RESERVED
DRIVE SELECT 1
DRIVE SELECT 0
INDEX
RESERVED
IN USE/HEAD LOAD
RESERVED
SIGNAL GND
(ODD NOS)
SIDE 0 HEAD
SIDE 1 HEAD
R/W FINISH
R/W START
SHIELD
P.KEY
ERASE 0
COMMON 0
ERASE 1
COMMON 1
**HEAD LOAD SOLENOID ASS'Y
PCBA FRONT OPT
STEPPING MOTOR ASS'Y
SPINDLE MOTOR ASS'Y
FASTON
FRAME GROUND

PCBA VERSIONS	MAIN SPEC.	* PARTS
-02	48tpi 8-CSS T1K	Q3. CR2. R6(2.80K). R8(2.2K). R9(120). R10. R12. R19(165). R20. R21(100). R22(100). C12(2200P). C14(2200P). C15(2200P). C16(2200P). C18(1500P). C23(180P). C24(100P). C25(100P). C28(6.8.50V). C29(6.8.50V). C30. L3~L5(330) JUMPER WIRE : CR3~CR5. L1. L2. U1. IU. FG STRAP POSTS : D0. D1. ML. RY
-03	48tpi 8-HL T1K	Q1. Q2. Q3. CR1. CR2. R4. R6(2.80K). R8(2.2K). R9(120). R10. R12. R19(165). R20. R21(100). R22(100). R28. C12(2200P). C14(2200P). C15(2200P). C16(2200P). C18(1500P). C23(180P). C24(100P). C25(100P). C28(6.8.50V). C29(6.8.50V). C30. L3~L5(330). J8(2P) JUMPER WIRE : CR3~CR5. L1. L2. U1. FG STRAP POSTS : D0. D1. IU. HS. RY
-04	48tpi 8-CSS T1K	R6(2.80K). R8(2.2K). R9(120). R10. R12. R19(165). R21(100). R22(100). C12(2200P). C14(2200P). C15(2200P). C16(2200P). C18(1500P). C23(180P). C24(100P). C25(100P). C28(6.8.50V). C29(6.8.50V). L3~L5(330) JUMPER WIRE : CR3~CR5. L1. L2. U1. IU. RY. S4. FG STRAP POSTS : D0. D1

PCBA VERSIONS	MAIN SPEC.	* PARTS
-07	96tpi F-CSS T1K	Q3. CR2. R1. R6(3.74K). R7(13K). R8(4.7K). R9(240). R10. R12. R19(150). R20. R21(100). R22(100). R24. C12(2200P). C14(2700P). C15(2700P). C16(2200P). C18(1500P). C23(180P). C24(100P). C25(100P). C26~C29(6.8.25V). C30. L3~L5(330) JUMPER WIRE : CR3~CR5. L1. L2. U1. IU. FG STRAP POSTS : D0. D1. ML. RY CUT:S7
-08	96tpi F-HL T1K	Q1. Q2. Q3. CR1. CR2. R1. R4. R6(3.74K). R7(13K). R8(4.7K). R9(240). R10. R12. R19(150). R20. R21(100). R22(100). R24. R28. C12(2200P). C14(2700P). C15(2700P). C16(2200P). C18(1500P). C23(180P). C24(100P). C25(100P). C26~C29(6.8.25V). C30. L3~L5(330). J8(2P) JUMPER WIRE : CR3~CR5. L1. L2. U1. FG STRAP POSTS : D0. D1. IU. HS. RY CUT:S7
-12	48tpi 8-CSS T1K	R1 THE OTHERS ARE THE SAME AS-02

VERSION TABLE

8. —O-O— MARK SHOWS JUMPER WIRE(JW).

7. ABBREVIATED NAMES ARE AS FOLLOWS:
   PAT: PATTERN SHORT
   JW : JUMPER WIRE

6. POLARIZING KEY POSITIONS FOR CONNECTOR(J) ARE:
   J1: BETWEEN PIN4 AND PIN6. J4: PIN6

5. TOLERANCE SYMBOLS FOR R.RA.C.AND L ARE:
   F: ±1%. G: ±2%. J: ±5%. K: ±10%. M: ±20%. V: +20~-10%. Z: +80~-20%

4. INDUCTOR (L) VALUES ARE IN MICRO-HENRIES.±5%(J).UNLESS OTHERWISE SPECIFIED.

3. CAPACITOR (C) VALUES ARE IN MICRO-FARADS.50V OR HIGHER.±5%(J).UNLESS OTHERWISE SPECIFIED.

2. RESISTOR (R) AND RESISTOR ARRAY (RA) VALUES ARE IN OHMS.1/8W OR GREATER.±5%(J).
   UNLESS OTHERWISE SPECIFIED.

NOTES. 1. PARTS WITH AN ASTERISK(*) DIFFER IN EACH PCBA VERSION.
   REFER TO VERSION TABLE. UNLISTED PARTS ARE NOT USED IN THAT VERSION.

P/N 15532097-XX

記号	改訂番号	年 月 日	担当	承認

材料		TEAC ティアック株式会社	
仕上	指定以外のエッジはイトメのこと	形式	FD-55BR/FR/GR
処理		品名	PCBA MFD CONTROL基N
普通寸法差	TS-E (級)	図名	SCHEMATIC
		図番	

未設			尺度
検図			
設計			第三角法
製図		87-05-28	単位 mm

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10010230-01

JKW1.KATAYO FILE:55BFRWFDRM4/DHST.122B

4-5. RECOMMENDABLE SPARE PARTS LIST

It is recommended to replace the wear parts periodically if the FDD is operated at a specially heavy duty condition or if it is operated over five years. Periodic replacement is not required for the parts if the FDD is operated at a normal operation duty.
Table 406 shows all of the maintenance parts. Replace the wear parts according to the recommended replacement cycle. Periodic replacement is not required for parts without a recommended replacement cycle.
The replacement of the parts should be done according to each referred item in Table 406.

Notes for Table:

1. Head carriage Ass'y are used always in pair with two guide shafts. The head carriage Ass'y represented by listed parts number in Table 406 includes these guide shafts which parts number is different from that of a head carriage Ass'y itself without these guide shafts. Refer to Note 2 and Table 402-C in item 4-2-1 as to the details.

2. It is recommended that the steel belt and belt spring are replaced together with the head carriage Ass'y. Parts number of the head carriage Ass'y in Table 406 includes these two parts. Refer to Note 2 and Table 402-C in item 4-2-1 as to the details.

   If the steel belt and belt spring are replaced individually or replaced with the stepping motor Ass'y, use the individual parts number in Table 406.

3. Periodic replacement is not required for parts without a recommended replacement cycle. Replace the parts when required such as during repair.

4. If two recommended cycles are listed, the cycle which the parts reach

first should have priority.

5. The required time for replacement includes the time for basic check and adjustment after the replacement.

6. Use the designated parts number for ordering the spare parts.

(Table 406) FD-55BR recommendable spare parts list

Spare parts			Replacement		
Parts name	Description	Parts No.	Replacement cycle	Required time	Referred items
Head carriage Ass'y BR	Note 1	17987603-00	10,000 head load & motor on hrs. or 1×10^7 seeks	45 min	
Steel belt	Note 2	16792349-00	Replace with head carriage Ass'y	—	
Belt spring		16392054-00			
Stepping motor Ass'y		14769070-80 14769070-80	1×10^7 seeks	30 min	
DD motor Ass'y (Spindle motor)		14733730-70	30,000 motor on hrs.	20 min	
Collet Ass'y		17987272-00	3×10^8 clamps	15 min	
CSS sub Ass'y		17987309-00	6×10^8 clamps	10 min	
PCBA MFD control #N		15532097-02	—	30 min	
PCBA front OPT #N		15532091-00	—	10 min	
Front bezel Ass'y		17987267-68	—	10 min	
Front lever Ass'y		17987281-68	—	5 min	

Software

Software

Software Contents

BIOS Services

Device I/O Services
Introduction

The BIOS (Basic Input/Output System) is the lowest-level interface between other software (application programs and the operating system itself) and the hardware. The BIOS routines provide various device input/output services as well as bootstrap and print screen and other services. Some of the services that BIOS provides are not available through the operating system, such as the graphics routines.

All calls to the BIOS are made through software interrupts (that is, by means of assembly language "INT *x*" instructions). Each I/O device is provided with a software interrupt, which transfers execution to the routine.

Entry parameters to BIOS routines are normally passed in CPU registers. Similarly, exit parameters are generally returned from these routines to the caller in CPU registers. To insure BIOS compatibility with other machines, the register usage and conventions are, for the most part, identical.

The following pages describe the entry and exit requirements for each BIOS routine. To execute a BIOS call, load the registers as indicated under the "Entry Conditions" banner. (Register AH will contain the function number in cases where a single interrupt can perform more than one operation.) Then issue the interrupt given for the call. The following example can be used to read a character from the keyboard:

```
MOV AH,0
INT 16H
```

Upon return, AL contains the ASCII character and AH the keyboard scan code.

Note: All registers except those used to return parameters to the caller are saved and restored by the BIOS routines.

Following is a quick reference list of software interrupts for all device I/O and system status services.

Service	**Software Interrupts**
Video Display	10 hex (16 dec)
Equipment	11 hex (17 dec)
Memory Size	12 hex (18 dec)
Diskette	13 hex (19 dec)
Serial Communications	14 hex (20 dec)
System Services	15 hex (21dec)
Keyboard	16 hex (22 dec)
Line Printer	17 hex (23 dec)
Bootstrap Loader	19 hex (25 dec)
System Clock	1Ahex (26 dec)

Keyboard

16 hex (22 dec)

Function Summary

AH	= 0:	Read keyboard (destructive with wait)
AH	= 1:	Scan keyboard (nondestructive, no wait)
AH	= 2:	Get current shift status
AH	= 5:	Store ASCII character and scan code in keyboard buffer
AH	= 10H:	Extended keyboard read
AH	= 11H:	Extended ASCII status
AH	= 12H:	Extended shift status read

Function Descriptions

Read Keyboard

Read the next character typed at the keyboard. Return the ASCII value of the character and the keyboard scan code, removing the entry from the keyboard buffer (destructive read).

Entry Conditions

AH = 0

Exit Conditions

AL = *ASCII value of character*

AH = *keyboard scan code*

Scan Keyboard

Set up the zero flag (Z flag) to indicate whether a character is available to read from the keyboard or not. If a character is available, return the ASCII value of the character and the keyboard scan code. The entry remains in the keyboard buffer (non-destructive read).

Entry Conditions

AH = 1

Exit Conditions

Z = no character available

NZ = a character is available, in which case:

AL = *ASCII value of character*

AH = *keyboard scan code*

Get Shift Status

Return the current shift status.

Entry Conditions

AH = 2

Exit Conditions

AL = *current shift status* (bit settings: set = true, reset = false)

Bit 0 = RIGHT SHIFT key depressed
Bit 1 = LEFT SHIFT key depressed
Bit 2 = CTRL (control) key depressed
Bit 3 = ALT (alternate mode) key depressed
Bit 4 = SCROLL state active
Bit 5 = NUMBER lock engaged
Bit 6 = CAPS lock engaged
Bit 7 = INSERT state active

Store ASCII Character

Entry Conditions

AH = 5

CL = ASCII character

CH = Scan Code

Exit Conditions

AL = 00: Successful

AL = 01: Buffer full

[C] = Operation failed

Extended Keyboard Read

Entry Conditions

AH = 10H

Exit Conditions

AL = *ASCII value of character*

AH = *keyboard scan code*

Extended ASCII Status

Entry Conditions

AH = 11H

Exit Conditions

Z = No character is available

NZ = A character is available, in which case:

AL = *ASCII value of character*

AH = *keyboard scan code*

Extended Shift Status Read

Entry Conditions

AH = 12H

Exit Conditions

AL = *shift status* (bit settings: set = true, reset = false)

- Bit 7 = INSERT active
- Bit 6 = CAPS LOCK active
- Bit 5 = NUM LOCK active
- Bit 4 = SCROLL LOCK active
- Bit 3 = ALT pressed
- Bit 2 = CTRL pressed
- Bit 1 = LEFT SHIFT pressed
- Bit 0 = RIGHT SHIFT pressed

AH = *extended shift status* (bit settings: set = true, reset = false)

- Bit 7 = SYS REQ pressed
- Bit 6 = CAPS LOCK active
- Bit 5 = NUM LOCK active
- Bit 4 = SCROLL LOCK active
- Bit 3 = RIGHT ALT active
- Bit 2 = RIGHT CTRL active
- Bit 1 = LEFT ALT active
- Bit 0 = LEFT CTRL active

Video Display

These routines provide an interface for the video display - the output half of the console (CON) device. MS-DOS considers the video display to be the default standard output (STDOUT) device.

Software Interrupts

10 hex (16 dec)

Function Summary Table
Supported Video BIOS Calls

INT 10H

AH = 00	Set Video Mode
AH = 01	Set Cursor Type
AH = 02	Set Cursor Position
AH = 03	Read Cursor Position
AH = 05	Select Active Display Page
AH = 06	Scroll Active Page Up
AH = 07	Scroll Active Page Down
AH = 08	Read Attribute/Character at Current Cursor Position
AH = 09	Write Attribute/Character at Current Cursor Position
AH = 0A	Write Character Only at Current Cursor Position
AH = 0B	Set Color Palette
AH = 0C	Write Dot
AH = 0D	Read Dot
AH = 0E	Write TTY to Active Display
AH = 0F	Current Video State

INT 10H

AH = 10	Color Palette Interface
AL = 00	Set Individual Register
AL = 01	Set Border Color
AL = 02	Set All Palette Registers and Border
AH = 13	Write String
AL = 00	Write Character String
AL = 01	Write Character String and Move Cursor
AL = 02	Write Character and Attribute Strings
AL = 03	Write Character and Attribute Strings and Move Cursor

Function Descriptions
Set CRT Mode

Entry Conditions

AH = 0

AL = *mode value*, as follows:

Alpha Modes

AL = 0: 40x25 black and white
AL = 1: 40x25 color
AL = 2: 80x25 black and white
AL = 3: 80x25 color

Graphics Modes

AL = 4: 320x200 color graphics
AL = 5: 320x200 black and white graphics with 4 shades
AL = 6: 640x200 black and white graphics with 2 shades
AL = 7: monochrome text

Additional Modes

AL = 8: 160x200 color graphics with 16 colors
AL = 9: 320x200 color graphics with 16 colors
AL = A: 640x200 color graphics with 4 colors

Note: If the high order bit of the AL register is 1, then the video buffer is not cleared.

Set Cursor Type

Set the cursor type and attribute.

Entry Conditions

AH = 1

CH = *bit values:*

Bits 5-6 = an invisible or erratically blinking cursor

Bits 5-6 = 0: produces a visible, blinking cursor

Bits 4-0 = *start line for cursor within character cell*

CL = *bit values:*

Bits 4-0 = *end line for cursor within character cell*

Set Cursor Position

Write (set) cursor position.

Entry Conditions

AH = 2

BH = *page number* (must be 0 for graphics modes)

DH = *row* (0 = top row)

DL = *column* (0 = leftmost column)

Get Cursor Position

Read (get) cursor position.

Entry Conditions

AH = 3

BH = *page number* (must be 0 for graphics modes)

Exit Conditions

DH = *row of current cursor position* (0 = top row)

DL = *column of current cursor position* (0 = leftmost column)

CX = *cursor type currently set* [1]:

See previous "Set Cursor Type" (AH = 1).

Select Active Page

Select active display page (valid in alpha mode only).

Entry Conditions

AH = 5

AL = 0 through 7: *new page value for modes 0, 1*

AL = 0 through 3: *new page values for modes 2, 3*

AL = 80H: read CRT/CPU page registers

AL = 81H: set CPU page register to value in BL

AL = 82H: set CRT page register to value in BH

AL = 83H: set CRT and CPU page registers in BH and BL

Exit Conditions

If Bit 7 of AL = 1 upon entry, then:

BH = *contents of CRT page register*

BL = *contents of CPU page register*

Scroll Up

Scroll active page up.

Entry Conditions

AH = 6

AL = *numbers of lines to scroll*. The number of lines that will be left blank at the bottom of the window. (0 = blank entire window)

CH = *row of upper left corner of scroll window*

CL = *column of upper left corner of scroll window*

DH = *row of lower right corner of scroll window*

DL = *column of lower right corner of scroll window*

BH = *attribute* (alpha modes) *or color* (graphics modes) *to be used on blank line*

Attributes

Color modes.

Foreground color:

Bit 0 = blue

Bit 1 = green

Bit 2 = red

Bit 3 = intensity

All bits off = black

Background color:

Bit 4 = blue

Bit 5 = green

Bit 6 = red

Bit 7 = blink

All bits off = white

Scroll Down

Scroll active page down.

Entry Conditions

AH = 7

AL = *number of lines to scroll* (0 = blank entire window)

CH = *row of upper left corner of scroll window*

CL = *column of upper left corner of scroll window*

DH = *row of lower right corner of scroll window*

DL = *column of lower right corner of scroll window*

BH = *attribute* (alpha modes) *of color* (graphics modes) *to be used on blank line.* See "Scroll Up" (AH = 6) for attribute values and "Set Color Palette" (AH = 11) for color values.

Read Attribute or Color/Character

Read a character and its attribute or color at the current cursor position.

Entry Conditions

AH = 8

BH = *display page number* (not used in graphics modes)

Exit Conditions

AL = *character read*

AH = *attribute of character* (alpha modes only)

Write Attribute or Color/Character

Write a character and its attribute or color at the current cursor position.

Entry Conditions

AH = 9

BH = *display page number* (not used in graphics modes)

CX = *number of characters to write*

AL = *character to write*

BL = *attribute of character* (for alpha modes) *or color of character* (for graphics modes. If Bit 7 of BL is set, the color of the character is XOR'ed with the color value). See "Scroll Up" (AH = 6) for attribute values and "Set Color Palette" (AH = 0BH) for color values.

Write Character Only

Write character only at current cursor position.

Entry Conditions

AH = 0AH

BH = *display page number* (valid for alpha modes only)

CX = *number of characters to write*

AL = *character to write*

BL = *color of character* (graphics mode)

Set Color Palette

Select the color palette.

Entry Conditions

AH = 0BH

BH = 0: Set background color (0-15) to color value in BL.

BL = *color value*:

1 = blue	5 = magenta	9 = light blue	13 = light magenta
2 = green	6 = yellow	10 = light green	14 = yellow
3 = cyan	7 = light grey	11 = light cyan	15 = white
4 = red	8 = dark grey	12 = light red	

or

BH = 1: Set default palette to the number (0 or 1) in BL.

In black and white modes:

BL = 0: 1 for white

BL = 1: 1 for black

In 4 color graphics modes:

BL = 0: (1 = green, 2 = red, 3 = yellow)

BL = 1: (1 = cyan, 2 = magenta, 3 = white)

In 16 color graphics modes:

1 = blue	5 = magenta	9 = light blue	13 = light magenta
2 = green	6 = yellow	10 = light green	14 = yellow
3 = cyan	7 = light grey	11 = light cyan	15 = white
4 = red	8 = dark grey	12 = light red	

Note: For alpha modes, Palette Entry 0 indicates the border color. For graphics modes, Palette Entry 0 indicates the border and the background color.

Write Dot

Write a pixel (dot).

Entry Conditions

AH = 0CH

DX = *row number*

CX = *column number*

AL = *color value* (When Bit 7 of AL is set, the resultant color value of the dot is the exclusive OR of the current dot color value and the value in AL.)

Read Dot

Read a pixel (dot).

Entry Conditions

AH = 0DH

DX = *row number*

CX = *column number*

Exit Conditions

AL = *color value of dot read*

Write TTY

Write a character in teletype fashion. (Control characters are interpreted in the normal manner.)

Entry Conditions

AH = 0EH

AL = *character to write*

BL = *foreground color* (graphics mode)

BH = *display page* (alpha modes)

Get CRT Mode

Get the current video mode.

Entry Conditions

AH = 0FH

Exit Conditions

AL = *current video mode*. See the previous "Set CTR Mode" (AH = 0) for values

AH = *number of columns on screen*

BH = *current active display page*

Set Palette Registers

Sets palette registers.

Entry Conditions

AH = 10H

AL = 0: Set Palette register

BL = *number of palette register* (0 -15) to set

BH = *color value to store*

AL = 1: Set border color register

BH = *color value to store*

AL = 2: Set palette color value to store and border registers

ES:DX points to a 17-byte list.

Bytes 0-15 = *values for palette registers 0-15*

Byte 16 = *value for border register*

Write String

Display a string of characters on screen.

Entry Conditions

AH = 13H

ES:BP = *pointer to start of string*

CX = *length of string* (attributes do not count)

DX = *starting cursor position* (DH = row, DL = column)

BH = *page number* (for text modes)

BL = *attribute for characters* (graphics modes)

AL = 00: Characters only string, cursor not updated

= 01: Characters only string, cursor updated

= 02: Character, attribute alternating string, cursor not updated

= 03: Character, attribute alternating string, cursor updated

Serial Communications

These routines provide asynchronous byte stream I/O from and to the RS-232C serial communications port. This device is labeled the auxiliary (AUX) I/O device in the device list maintained by MS-DOS.

Software Interrupts

14 hex (20 dec)

Function Summary

AH = 0: Reset Comm port

AH = 1: Transmit character

AH = 2: Receive character

AH = 3: Get current Comm status

DX = *communication port number* (0 or 1)

Function Descriptions
Reset Comm Port

Reset (or initialize) the communication port according to the parameters in AL, DL, and DH.

Entry Conditions

AH = 0

AL = *RS-232C parameters,* as follows:

DX = *port number* (0 or 1)

7 6 5	4 3	2	1 0
Baud Rate	*Parity*	*Stop Bits*	*Word Length*

000 = 110 baud
001 = 150 baud
010 = 300 baud
011 = 600 baud
100 = 1200 baud
101 = 2400 baud
110 = 4800 baud
111 = 9600 baud

00 = none
01 = odd
11 = even

0 = 1 bit
1 = 2 bits

10 = 7 bits
11 = 8 bits

Exit Conditions

AX = *RS-232C status*; See the following"Get Current Comm Status" (AH = 3)

Transmit Character

Transmit (output) the character in AL (which is preserved).

Entry Conditions

AH = 1

AL = *character to transmit*

DX = *port number* (0 or 1)

Exit Conditions

AH = *RS-232C status;* See the following "Get Current Comm Status" (AH = 3). If Bit 7 is set, the routine was unable to transmit the character because of a timeout error.)

AL is preserved

Receive Character

Receive (input) a character in AL (wait for a character, if necessary). On exit, AH will contain the RS-232 status, except that only the error bits (1, 2, 3, 4, 7) can be set; the timeout bit (7), if set, indicates that data set ready was not received and the bits in AH are not meaningful. Thus, AH is non-zero only when an error occurred.

Entry Conditions

AH = 2

DX = *port number* (0 or 1)

Exit Conditions

AL = *character received*

AH = *RS-232C status;* See the following "Get Current Comm Status" (AH = 3)

Get Current Comm Status

Read the communication status into AX.

Entry Conditions

AH = 3

DX = *port number* (0 or 1)

Exit Conditions

AH = *RS-232C status*, as follows (set = true):

Bit 0 = data ready
Bit 1 = overrun error
Bit 2 = parity error
Bit 3 = framing error
Bit 4 = break detect
Bit 5 = transmitter holding register empty
Bit 6 = transmitter shift register empty
Bit 7 = timeout occurred

AL = *modem status,* as follows (set = true):

Bit 0 = delta clear to send
Bit 1 = delta data set ready
Bit 2 = trailing edge ring detector
Bit 3 = delta receive line signal detect
Bit 4 = clear to send
Bit 5 = data set ready
Bit 6 = ring indicator
Bit 7 = receive line signal detect

Line Printer

These routines provide an interface to the parallel line printer. This device is labeled "PRN" in the device list maintained by the operating system.

Software Interrupts

17 hex (23 dec)

Function Summary

AH = 0: Print character

AH = 1: Reset printer port

AH = 2: Get current printer status

Function Descriptions

Print a Character

Entry Conditions

AH = 0

AL = *character to print*

DX = *printer to be used* (0-2)

Exit Conditions

0AH = *printer status*. See the following "Get Current Printer Status" (AH = 2)

(If Bit 0 is set, the character could not be printed because of a timeout error.)

Reset Printer Port

Reset (or initialize) the printer port.

Entry Conditions

AH = 1

DX = *printer to be used* (0-2)

Exit Conditions

AH = *printer status;* See the following "Get Current Printer Status" (AH = 2)

Get Current Printer Status

Read the printer status into AH.

Entry Conditions

AH = 2

Exit Conditions

DX = *printer to be used* (0-2)

AH = *printer status as follows* (set = true):

Bit 0 = timeout occurred

Bit 1 = [unused]

Bit 2 = [unused]

Bit 3 = I/O error

Bit 4 = selected

Bit 5 = out of paper

Bit 6 = acknowledge

Bit 7 = not busy

System Clock

These routines provide methods of reading and setting the clock maintained by the system. This device is labeled CLOCK in the device list of the operating system. An interface for setting the multiplexer for audio source is also provided.

Software Interrupts

1A hex (26 dec)

Function Summary

AH	= 0:	Get time of day
AH	= 1:	Set time of day
AH	= 2:	Read real-time clock
AH	= 3:	Set real-time clock
AH	= 4:	Read date from real-time clock
AH	= 5:	Set the date in the real-time clock
AH	= 80H:	Set up sound multiplexer

The clock runs at the rate of 1,193,180/65,536 per second (about 18.2 times per second).

Function Descriptions

Get Time of Day

Get (read) the time of day in binary format.

Entry Conditions

AH = 0

Exit Conditions

CX = *high* (most significant) *portion of the clock count*

DX = *low* (least significant) *portion of the clock count*

AL = 0 of the clock was read or written (via AH = 0,1) within the current 24-hour period; otherwise, AL = 0

Set Time of Day

Set (write) the time of day using binary format.

Entry Conditions

AH = 1

CX = *high* (most significant) *portion of clock count*

DX = *low* (least significant) *portion of clock count*

Read Clock Time of Day

Read the time of day kept in the clock.

Entry Conditions

AH = 2

Exit Conditions

CH = hours in BCD

CL = minutes in BCD

DH = seconds in BCD

Set Clock Time of Day

Set the time of day kept in the clock.

Entry Conditions

AH = 3

CH = hours in BCD

CL = minutes in BCD

DH = seconds in BCD

Read Clock Date

Read the date kept in the clock.

Entry Conditions

AH = 4

Exit Conditions

CH = century in BCD

CL = year in BCD

DH = month in BCD

DL = day in BCD

Set Clock Date

Set the date kept in the clock.

Entry Conditions

AH = 5

CH = century in BCD

CL = year in BCD

DH = month in BCD

DL = day in BCD

Sound Multiplexer

Sets the multiplexer for audio source.

Entry Conditions

AH = 80

AL = *source of sound*

00 = 8253 channel 2

02 = audio in

03 = complex sound generator chip

Disk I/O Support for Diskette Only

System Configuration

Software Interrupt

13 hex (19 dec)

Function Summary

AH	= 0:	Reset diskette
AH	= 1:	Return status of last diskette operation
AH	= 2:	Read sector(s) from diskette
AH	= 3:	Write sector(s) to diskette
AH	= 4:	Verify sector(s) on diskette
AH	= 5:	Format track on diskette
AH	= 08H:	Read drive parameters
AH	= 15H:	Read DASD type
AH	= 16H:	Diskette change line status

Function Descriptions

Reset Diskette

Reset the diskette system. Resets associated hardware and recalibrates all diskette drives.

Entry Conditions

AH = 0

Exit Conditions

See the following "Exits From All Calls."

Return Status of Last Diskette Operation

Returns the diskette status of the last operation in AH.

Entry Conditions

AH = 1

Exit Conditions

AL = *status of the last operation*. For values, see the following "Exits From All Calls."

Read Sector(s) from Diskette

Read the desired sector(s) from the diskette into RAM.

Entry Conditions

AH = 2

DL = *drive number* (0-2 if Tandy 1000 TL; 0-1 if Tandy 1000 SL)

DH = *head number* (0-1)

CH = *track number* (0-79)

CL = *sector number* (1-9)

AL = *sector count* (1-9)

ES:BX = *pointer to disk buffer*

Exit Conditions

See the following "Exits from all Calls."

AL = *number of sectors read*

Write Sector(s) to Diskette

Write the desired sector(s) from RAM to disk.

Entry Conditions

AH = 3

DL = *drive number* (0-2 if Tandy 1000 TL; 0-1 if Tandy 1000 SL)

DH = *head number* (0-1)

CH = *track number* (0-79)

CL = *sector number* (1-9)

AL = *sector count* (1-9)

ES:BX = *pointer to disk buffer*

Exit Conditions

See the following "Exits From All Calls."

AL = *number of sectors written*

Verify Sector(s) on Diskette

Verify the desired sector(s) are readable.

Entry Conditions

AH = 4

DL = *drive number* (0-2 if Tandy 1000 TL; 0-1 if Tandy 1000 SL)

DH = *head number* (0-1)

CH = *track number* (0-79)

CL = *sector number* (1-9)

AL = *sector count* (1-9)

Exit Conditions

See the following "Exits From All Calls."

AL = *number of sectors verified*

Format on Diskette

Format the desired track.

Entry Conditions

AH = 5

AL = *sector count* (1-9)

DL = *drive number* (0-2 if Tandy 1000 TL; 0-1 if Tandy 1000 SL)

DH = *head number* (0-1)

CH = *track number* (0-79)

CL = *sector number* (1-9)

ES:BX = *pointer to a group of address fields for each track.* Each address field is made up of 4 bytes. These are C, H, R, and N, where:

C = *track number*

H = *head number*

R = *sector number*

N = *the number of bytes per sector*
(00 = 128, 01 = 256, 02 = 512, 03 = 1024)

There is one entry for every sector on a given track.

Exit Conditions

See the following "Exits From All Calls."

Read Drive Parameters

Return the drive parameters.

Entry Conditions

AH = 08H

DL = *drive number* (0-2 if Tandy 1000 TL; 0-1 if Tandy 1000 SL)

Exit Conditions

AX = 0
BH = 0
CH = Maximum usable track number
CL = Maximum usable sector number
DH = Maximum usable head number
DL = Number of diskette drives installed (0-2 if Tandy 1000TL; 0-1 if Tandy 1000 SL)
ES:Dl = Pointer to diskette drive parameter table for the maximum media type supported on the specified drive

CF = 0: No error

CF = 1: Illegal parameter

Read DASD Type

Return the change line status.

Entry Conditions

AH = 15H

DL = *drive number* (0-1 if Tandy 10000 TL; 0-1 if Tandy 1000 SL)

Exit Conditions

CF = 1: Operation was not successful. Previous versions of the Tandy 1000 will return CF = 1.

AH = 1: Invalid command.

CF = 0: Operation was successful

AH = 0: Drive not present

= 1: Diskette, no change line available

= 2: Diskette, change line available

Diskette Change Line Status

Return the status of the diskette change line.

Entry Conditions

AH = 16H

DL = *drive number* (0-2 if Tandy 1000 TL; 0-1 if Tandy 1000 SL)

Exit Conditions

CF = 0: If AH = 0
CF = 1: If AH is non 0
AH = 0: Diskette change signal not active
= 1: Invalid diskette parameter
= 6: Diskette change signal active
= 80: Diskette drive not ready (drive door is open)

Exits From All Calls

AH = *Status of operation*, where set = true

Error Code	Condition
01H	Illegal Function
02H	Address Mark Not Found
03H	Write Protect Error
04H	Sector Not Found
06H	Diskette Change Line Active
08H	DMA Overrun
09H	Attempt to DMA Across a 64K Boundary
10H	Bad CRC on Disk Read
20H	Controller Failure
40H	Seek Failure
80H	Device Timeout, Device Failed to Respond

[NC] = operation successful (AH = 0)
[C] = operation failed (AH = error status)

Equipment

This service returns the "equipment flag" (hardware configuration of the computer system) in the AX register.

Software Interrupts

11 hex (17 dec)

The "equipment flag" returned in the AX register has the following meanings for each bit:

Reset = the indicated equipment is not in the system

Set = the indicated equipment is in the system

Bit 0 = diskette installed

Bit 1 = math coprocessor

Bits 2,3 always = 11

Bits 4,5 *initial video mode*

01	40x25 Color
10	80x25 Color
11	80x25 Monochrome

Bits 6,7 *number of diskette drives* (only if Bit 0 = 1)

00	1
01	2
10	3 (Tandy 1000 TL ONLY)

Bit 8 0 = DMA present (**always present**)
1 = no DMA present

Bits 9, 10, 11 *number of RS232 cards*

Bit 12 game I/O adapter present (joystick)

Bit 13 not used

Bits 14,15 *number of printers*

Memory Size

This service returns the total number of kilobytes of RAM in the computer system (contiguous starting from Address 0) in the AX register. The maximum value returned is 640.

Software Interrupts

12 hex (18 dec)

Bootstrap Loader

Track 0, Sector 1 is read into Segment 0, Offset 7C00.

Control is then transferred as follows: (CS) = 0000H

(IP) = 7C00H

(DL) – drive where bootstrap sector was read

Software Interrupts

19 hex (25 dec)

System Services

Software Interrupts

15 hex (21dec)

Function Summary

AH = C0H: Machine identification

AH = 15H: Read and write EEPROM data

Function Descriptions

Machine Identification

The machine identification algorithm is the same as all previous Tandy 1000's. As well, the Tandy 1000 SL and Tandy 1000 TL computers have a new BIOS call to further identify the machine.

All current and previous Tandy 1000 computers have the following machine identification:

Byte at address FFFF:E = FF hex (compatible with IBM PC)

Byte at address FC000:0 = 21 hex (Tandy 1000 unique)

Entry Conditions

AH = C0H

Exit Conditions

If CF = 0

ES:BX = *pointer to machine identification data in ROM*

DW 0003 *Byte count of data that follows* (always 3)

DB *xx* *Model ID*

DB *xx* *Submodel ID*

DB *xx* *BIOS revision level*

IF CF = 1, the call is not supported (all previous versions of the Tandy 1000)

	Tandy 1000 SL	Tandy 1000 TL
Model ID	FF	FF
Submodel ID	00	01
BIOS revision level	*xx*	*xx*

Function Descriptions
Read From EEPROM

Read the 16-bit value from the indicated EEPROM word.

Entry Conditions

AH = 70H

AL = 0

BL = *word number to read* (0-63)

Exit Conditions

DX = *word value*

Carry flag set indicates EEPROM call not supported.

Write to EEPROM

Write a 16-bit value to the indicated EEPROM word.

Entry Conditions

AH = 70H

AL = 1

BL = *word number to write* (0-63)

DX = *word value to write*

Exit Conditions

Carry Flag set indicates EEPROM call not supported.

Tandy 1000 SL and Tandy 1000 TL BIOS Sound Support

The BIOS in these computers has the same support for sound as all previous Tandy 1000 computers, as well as support for additional sound features. The API for this new BIOS support is defined in the following information.

Software Interrupts

1A hex (26 dec)

Function Summary

AH	= 81H:	Get sound status
AH	= 82H:	Input sound (from the microphone)
AH	= 83H:	Output sound (to the speaker)
AH	= 84H:	Stop sound input and output

Function Descriptions

Get Sound Status

Gets sound status.

Entry Conditions

AH = 81H

Exit Conditions

Not Busy:

AX = 00C4H

CF = 0

Busy:

AX = 00C4H

CF = 1

Input Sound

Inputs sound from the microphone.

Entry Conditions

AH = 82H

ES:BX = *buffer address*

CX = *buffer length*

DX = *transfer rate* (1-4095, where 1 is the fastest transfer rate)

Exit Conditions

Not Busy:

AH = 0

CF = 0

Busy:

AH = 0

CF = 1

Output Sound

Outputs sound to the speaker.

Entry Conditions

AH = 83H: Output sound (to the speaker)

ES:BX = *buffer address*

CX = *buffer length*

DX = *transfer rate* (1-4095, where 1 is the fastest transfer rate)

AL = *volume* (0-7, where 0 = no sound)

Exit Conditions

Not Busy:

AH = 0

CF = 0

Busy:

AH = 0

CF = 1

Stop Sound Input and Output

Stops sound input and output.

Entry Conditions

AH = 84H

Notes: The transfer rate values in register DX are not the same for calls AH = 82H and AH = 83H. To input a buffer of data with the AH = 82H call with a given DX value, then play it back with the AH = 83H call so that it sounds the same, set the DX value for output approximately 11.5 times as large as the DX value for input when run on a Tandy 1000 SL and approximately 10.0 times faster on a Tandy 1000 TL.

This BIOS call uses the DMA hardware to input and output the sound buffer. When functions AH = 82H and AH = 83H are called, the BIOS initiates the I/O and returns to the calling program immediately. When the DMA transfer is complete, the BIOS will receive a hardware interrupt and will execute a software INT 15H with AH = 91H and AL = FBH. If an application program needs to know when the data transfer is complete, it has to hook INT 15H and watch for this event.

The BIOS call masks the hardware restriction of not being able to DMA across a 64 kilobyte memory address boundary from the calling program.

Keyboard ASCII and Scan Codes
Function Keys, Cursor Keypad, Numeric Keypad

SCAN CODE	NORM CASE ASCII CODE		UPPER CASE ASCII CODE		CTRL CASE ASCII CODE		ALT CASE ASCII CODE	
3B	F1	x3B	F11	x54	F21	x5E	F31	x68
3C	F2	x3C	F12	x55	F22	x5F	F32	x69
3D	F3	x3D	F13	x56	F23	x60	F33	x6A
3E	F4	x3E	F14	x57	F24	x61	F34	x6B
3F	F5	x3F	F15	x58	F25	x62	F35	x6C
40	F6	x40	F16	x59	F26	x63	F36	x6D
41	F7	x41	F17	x5A	F27	x64	F37	x6E
42	F8	x42	F18	x5B	F28	x65	F38	x6F
43	F9	x43	F19	x5C	F29	x66	F39	x70
44	F10	x44	F20	x5D	F30	x67	F40	x71
57	F11	e8500		e8700		e8900		e8B00
58	F12	e8600		e8800		e8A00		e8C00
E037	PrintScm*		PrintScm*		CPrSc	x72	SysRq*	--
46	Scr Lock	-	Scr Lock-		--	--	Scr Lock	--
E145	Pause*	--	Pause*	--			Pause*	--
E046					Break*	x00		
E052	Insert		x52	e52E0	--	e92E0	--	eA200
E047	Home		x47	e47E0	x77	e77E0	--	e9700
E049	Page Up		x49	e47E0	x84	e84E0	--	e9900
E053	Delete		x53	e53E0	--	e93E0	--	eA300
E04F	End		x4F	e4FE0	x75	e75E0	--	e9F00
E051	Page Down		x51	e51E0	x76	e76E0	--	eA100
E048	Up		x48	e48E0	--	e8DE0	--	e9800
E04B	Left		x4B	e4BE0	x73	e73E0	--	e9B00
E050	Down		x50	e50E0	--	e91E0	--	eA000
E04D	Right		x4d	e4DE0	x74	e74E0	--	e9D00
45	Num Lock	--	Num Lock	--	--	--	Num Lock	--
E035	/	2F	/	2F		e9500		eA400
37	*	2A	*	2A		e9600		e37F0
47	Home	x47	7	37	ClrSc	x77	¥	--
48	UP	x48	8	38		e8D00	¥	--
49	Page Up	x49	9	39	TOS	x84	¥	--
4A	-	2D	-	2D		e8E00		e4AF0
4B	Left	x4B	4	34	LWord	x73	¥	--
4C		e4CF0	5	35		e8F00	¥	--
4D	RIGHT	x4D	6	36	RWord	x74	¥	--
4E	+	2B	+	2B		e9000		e4EF0
4F	End	x4F	1	31	ErEOL	x75	¥	--
50	DOWN	x50	2	32		e9100	¥	--
51	Pg Dn	x51	3	33	ErEOS	x76	¥	--
52	Ins	x52	0	30		e9200	¥	--
53	Del	x53	.	2E		e9300	--	--
E01C	Enter	0D	Enter	0D	LF	0A		eA600
01	ESC	1B	ESC	1B	ESC	1B		e01F0
02	1	31	!	21	--	--	ALT1	x78
03	2	32	@	40	NULL	00	ALT2	x79
04	3	33	#	23	--	--	ALT3	x7A
05	4	34	$	24	--	--	ALT4	x7B
06	5	35	%	25	--	--	ALT5	x7C
07	6	36	^	5E	RS	1E	ALT6	x7D
08	7	37	&	26	--	--	ALT7	x7E
09	8	38	*	2A	--	--	ALT8	x7F

SCAN CODE	NORM CASE ASCII CODE		UPPER CASE ASCII CODE		CTRL CASE ASCII CODE		ALT CASE ASCII CODE	
0A	9	39	(	28	--	--	ALT9	x80
0B	-	30	)	29	--	--	ALT0	x81
0C	-	2D	_	5F	US	1F	ALT-	x82
0D	=	3D	+	2B	--	--	ALT=	x83
0E	BS	08	BS	08	DEL	7F		e0EF0
0F	HT	09	BTab	x0F		e9400		eA500
10	q	71	Q	51	DC1	11	ALTQ	x10
11	w	77	W	57	ETB	17	ALTW	x11
12	e	65	E	45	ENQ	05	ALTE	x12
13	r	72	R	52	DC2	12	ALTR	x13
14	t	74	T	54	DC4	14	ALTT	x14
15	y	79	Y	59	EM	19	ALTY	x15
16	u	75	U	55	NAK	15	ALTU	x16
17	i	69	I	49	HT	09	ALTI	x17
18	o	6F	O	4F	SI	0F	ALTO	x18
19	p	70	P	50	DLE	10	ALTP	x19
1A	[	5B	{	7B	ESC	1B		e1AF0
1B	]	5D	}	7D	GS	1D		e1BF0
1C	Enter	0D	Enter	0D	LF	0A		e1CF0
1D	Ctrl	--	Ctrl	--	Ctrl	--	Ctrl	--
E01D	Ctrl	--	Ctrl	--	Ctrl	--	Ctrl	--
1E	a	61	A	41	SOH	01	ALTA	x1E
1F	s	73	S	53	DC3	13	ALTS	x1F
20	d	64	D	44	EOT	04	ALTD	x20
21	f	66	F	46	ACK	06	ALTF	x21
22	g	67	G	47	BEL	07	ALTG	x22
23	h	68	H	48	BS	08	ALTH	x23
24	j	6A	J	4A	LF	0A	ALTJ	x24
25	k	6B	K	4B	VT	0B	ALTK	x25
26	l	6C	L	4C	FF	0C	ALTL	x26
27	;	3B	:	3A	--	--		e27FO
28	'	27	"	22	--	--		e28F0
29	`	60	~	7E	--	--		e29F0
2A	LShift	--	LShift	--			LShift	--
2B	\	5C	|	7C	FS	1C		e2BF0
2C	z	7A	Z	5A	SUB	1A	ALTZ	x2C
2D	x	78	X	58	CAN	18	ALTX	x2D
2E	c	63	C	43	ETX	03	ALTC	x2E
2F	v	76	V	56	SYN	16	ALTV	x2F
30	b	62	B	42	STX	02	ALTB	x30
31	n	6E	N	4E	S0	0E	ALTN	x31
32	m	6D	M	4D	CR	0D	ALTM	x32
33	,	2C	<	3C	--	--		e33F0
34	.	2E	>	3E	--	--		e34F0
35	/	2F	?	3F	--	--		e35F0
36	RShift	--	RShift	--	RShift	--	RShift	--
38	Alt	--	Alt	--	Alt	--	Alt	--
E038	Alt	--	Alt	--	Alt	--	Alt	--
39	SPACE	20	SPACE	20	SPACE	20	SPACE	20
3A	CapsLock	--	CapsLock	--	--	--	CapsLock	--
56+	\	5C	|	7C	--	--	--	--

Keyboard Tables

These symbols have special meanings in the following tables:

--	Indicates that no ASCII code is generated for the key combination.
x	Values preceded by x are extended ASCII codes. The keyboard driver returns a NULL ASCII code and the number in the table for the scan code.
e	Values preceded by e are produced when you are using an enhanced BIOS. When using the BIOS Read Key function, these keys are either discarded or translated to a value compatible with older computers. When using the Enhanced Read Key function, AH = 10H, INT 16H, these keys are returned to your program.
+	A + in the scan code field denotes the extra key on the international version of the enhanced keyboard. This key is not available on the standard USA enhanced keyboard.
¥	The ALT key provides a way to generate the ASCII code of the decimal numbers in the range 1 to 255. Hold down the ALT key while typing a number in that range on the numeric keypad. When you release the ALT key, the character of the ASCII code you typed is generated and displayed.
BREAK	Empties the keyboard queue and executes the keyboard break interrupt (INT 1BH). Places a NULL ASCII scan code in the keyboard queue.
PAUSE	Delays system activity until you press another key.
PrtSC or Print Scrn	Invokes the BIOS print screen function (INT 5H).

CPrSc	Tells MS-DOS to direct console output to both the printer and the console. A second CPrSc halts printer output.
SysRq	Interrupts the current process and allows another program to take control, if supported. When the SysRq key is pressed, INT 15H is invoked with AX = 8500H. When the key is released, INT 15H is invoked with AX = 8501H.
Reset	Restarts your computer.

MS-DOS Memory Map

Hexadecimal Starting Address (Segment:Offset)	Description
000:00	BIOS Interrupt Vectors
000:80	Available Interrupt Vectors
0040:00[1]	ROM BIOS Data Area
0050:00	MSDOS and BASIC Data Area
0070:00	I/O.SYS Drivers
0190:00[2]	MS-DOS
05B0:00[2]	Available to user
X800:00[3]	Video RAM in 32K video modes
XC00:00[3]	Video RAM in 16K video mode
B800:00[4]	Video RAM Window (32K)
E000:00	ROM Drive
F000:00	Reserved for system ROM
FC00:00	System BIOS ROM

Notes:

[1] Detailed description in following pages.

[2] Approximate address; subject to change.

[3] X is defined as follows:

Memory Size	X Value
128K	1
256K	3
384K	5
512K	7
640K	9
768K	B

[4] Video memory accessed through the B800:0 window for all video modes.

ROM BIOS Data Area

The following table gives the starting offset, and length of each BIOS device driver. This area is located at segment 40:00.

Comm card address	0000	8 (1 word per card)
Printer addresses	0008	8 (1 word per printer)
Devices installed	0010	2 (16 bits)
Not used	0012	1
Memory size	0013	2 (1 word)
I/O channel RAM size	0015	2 (1 word)
KBD data area	0017	39
Disk data area	003E	11
Video data area	0049	30
Not used	0067	5
Clock data area	006C	5
KBD Break & Reset flags	0071	3
Not used	0074	4
Printer timeout counter	0078	4 (1 byte per printer)
Comm timeout counter	007C	4 (1 byte per card)
KBD extra data area	0080	4 (2 words)

The structure and usage of the Video driver RAM data area is as follows:

HEX Offset From Segment 0040:0000	**Length and Intended Use**	
49H	1 byte -	current CRT mode (0-7)
4AH	1 word -	screen column width
4CH	1 word -	byte length of screen
4EH	1 word -	address/offset of beginning of current display page
50H	8 words-	row/col coordinates of the cursor for each of up to 8 display pages
60H	1 word -	current cursor type (See "Set Cursor Type" for correct encoding)
62	1 byte -	current display page 1 word - base address + 4 of the CRT controller card
65H	1 byte -	copy of value written to the Mode Select Register
66H	1 byte -	current color palette setting

The equipment check BIOS call (INT 11H) and memory size BIOS call (INT 12H) return information from the following data areas:

HEX Offset From Segment 0040:0000	**Length and Intended Use**
10H	Devices installed word
13H	Memory installed word

The structure and usage of the diskette driver RAM data area is as follows:

HEX Offset From Segment 0040:0000	**Length and Intended Use**	
3EH	1 byte -	drive recalibration status - bit 3-0, if 0 then drive 3-0 needs recalibration before next Seek. Bit 7 indicates interrupt occurrence
3FH	1 byte -	motor status - Bit 3-0 drive 3-0 motor is on/off. Bit 7 - current operation is write, requires delay
40H	1 byte -	motor turn off timeout counter (see Timer ISR)
41H	1 byte -	disk status - codes are defined as in this section
42H	7 bytes -	7 bytes of status returned by the controller during result phase of operation

Value	Error Condition
01H	Illegal Function
02H	Address Mark Not Found
03H	Write Protect Error
04H	Sector Not Found
06H	Diskette Change Line Active
08H	DMA Overrun
09H	Attempt to DMA Across a 64K Boundary
10H	Bad CRC on Disk Read
20H	Controller Failure
40H	Seek Failure
80H	Device Timeout, Device Failed to Respond

The structure and usage of the RS232 driver RAM data area is as follows:

HEX Offset From Segment 0040:0000	Length and Intended Use	
00H	4 words -	Base address of each one of 4 possible comm cards
7CH	4 words -	1 word timeout count for each of 4 possible comm cards

The structure and usage of the Keyboard driver RAM data area is as follows:

HEX Offset From Segment 0040:0010	**Length and Intended Use**
17	1 byte- Keyboard shift state flag returned by function 02
	Bits 7- INSERT state active, 6 - CAPS LOCK on/off, 5 - NUM LOCK on/off, 4 - SCROLL LOCK on/off, 3 - ALT key pressed 2 - CTRL key pressed 1 - Left SHIFT key pressed, 0 - Right SHIFT key pressed,
18	1byte- Secondary shift state flag, Bits INSERT key pressed, 6 - CAPS LOCK pressed, 5 - NUM LOCK pressed, 4 - SCROLL LOCK NUM LOCK pressed, 4 - SCROLL pressed, 4 - SCROLL LOCK pressed, 3 - Pause on/off, pressed, 3 - Pause on/off, 2,1,0 - not used
19	1 byte- Used to store ALT keypad entry
1A	1 word- Pointer to beginning of the keyboard buffer
1C	1 word- Pointer to end of the keyboard buffer
1E	16- Keyboard buffer (enough for words)
	15- Type ahead entries

The structure and usage of the clock service routine is as follows:

HEX Offset From Segment 0040:0000	**Length and Intended Use**
6CH	1 word - Least significant 16 bits of clock count
6EH	1 word - Most significant 16 bits of clock count
70H	1 byte - Twentyfour hour rollover flag

Additional Data Area

HEX Offset
From Segment
0040:0000

B0H	2 words international support				
B4H	1 byte	0 = No monochrome monitor			
		FFH = Monochrome monitor			
B5H	1 byte	Bit 0:	0	=	Drive A is 5-1/4"
			1	=	Drive A is 3-1/2"
		Bit 1:	0	=	Drive B is 5-1/4"
			1	=	Drive B is 3-1/2"
		Bit 2:	0	=	Tandy 1000 keyboard layout
			1	=	IBM keyboard layout
		Bit 3:	0	=	Slow CPU speed mode
			1	=	Fast CPU speed mode
		Bit 4:	0	=	Internal color video support enabled
			1	=	Internal color video support disabled, external color video enabled

HEX Offset
From Segment
0040:0000

	Bit 5: 0	= No external mono-chrome video installed	
	1 = External monochrome video installed		
B6H	1 byte	Bit 0:	0 = Drive C is 5-1/4"
			1 = Drive C is 3-1/2"
40:C2	1 byte		01 = ROM drive is A:
			02 = ROM drive is B:
			03 = ROM drive is C:

KEYBOARD SCAN CODES

Key #	Key Descript.	Hardware Kybrd Make Code	Hardware Kybrd Break Code	Kybrd Interrupt Make Code	Kybrd Interrupt Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
1	Esc	76	F076	01	81	011B	011B	011B	-----	011B	011B	011B	0100
2	F1	05	F005	3B	BB	3B00	5400	5E00	6800	3B00	5400	5E00	6800
3	F2	06	F006	3C	BC	3C00	5500	5F00	6900	3C00	5500	5F00	6900
4	F3	04	F004	3D	BD	3D00	5600	6000	6A00	3D00	5600	6000	6A00
5	F4	0C	F00C	3E	BE	3E00	5700	6100	6B00	3E00	5700	6100	6B00
6	F5	03	F003	3F	BF	3F00	5800	6200	6C00	3F00	5800	6200	6C00
7	F6	0B	F00B	40	C0	4000	5900	6300	6D00	4000	5900	6300	6D00
8	F7	83	F083	41	C1	4100	5A00	6400	6E00	4100	5A00	6400	6E00
9	F8	0A	F00A	42	C2	4200	5B00	6500	6F00	4200	5B00	6500	6F00
10	F9	01	F001	43	C3	4300	5C00	6600	7000	4300	5C00	6600	7000
11	F10	09	F009	44	C4	4400	5D00	6700	7100	4400	5D00	6700	7100
12	F11	78	F078	57	D7	-----	-----	-----	-----	8500	8700	8900	8B00
13	F12	07	F007	58	D8	-----	-----	-----	-----	8600	8800	8A00	8C00
14	Print Scrn	E07C	E0F07C	E02AE037	E0B7E0AA	Note[1]	Note[1]	7200	-----	Note[1]	Note[1]	7200	-----
15	Scroll Lock	7E	F07E	46	C6	Note[2]	Note[2]	------	Note[2]	Note[2]	Note[2]	-----	Note[2]
16	Pause Break	E11477	E1F014F077	E11D45	E19DC5	Note[3]	Note[3]	Note[4]	Note[3]	Note[3]	Note[3]	Note[4]	Note[3]
17	~ or \	0E	F00E	2B	AB	2960	297E	-----	-----	6000	7E00	-----	2900
18	! or 1	16	F016	02	82	0231	0221	-----	7800	0231	0221	-----	7800

KEYBOARD SCAN CODES

Key #	Key Descript.	Hardware Kybrd Make Code	Hardware Kybrd Break Code	Kybrd Interrupt Make Code	Kybrd Interrupt Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
19	@ or 2	1E	F01E	03	83	0332	0340	0300	7900	0332	0340	0300	7900
20	# or 3	26	F026	04	84	0433	0423	-----	7A00	0433	0423	-----	7A00
21	$ or 4	25	F025	05	85	0534	0524	-----	7B00	0534	0524	-----	7B00
22	% or 5	2E	F02E	06	86	0635	0625	-----	7C00	0635	0625	-----	7C00
23	^ or 6	36	F036	07	87	0736	075E	071E	7D00	0736	075E	071E	7D00
24	& or 7	3D	F03D	08	88	0837	0826	-----	7E00	0837	0826	-----	7E00
25	* or 8	3E	F03E	09	89	0938	092A	-----	7F00	0938	092A	-----	7F00
26	(or 9	46	F046	0A	8A	0A39	0A28	-----	8000	0A39	0A28	-----	8000
27	) or 0	45	F045	0B	8B	0B34	0B29	-----	8100	0B34	0B29	-----	8100
28	_ or -	4E	F04E	0C	8C	0C2D	0C5F	0C1F	8200	0C2D	0C5F	0C1F	8200
29	+ or =	55	F055	0D	8D	0D3D	0D2B	-----	8300	0D3D	0D2B	-----	8300
30	Backspace	66	F066	0E	8E	0E08	0E08	0E7F	-----	0E08	0E08	0E7F	0E00
31	Insert	E070	E0F070	E02AE052	E0D2E0AA	5200	5200	-----	-----	52E0	52E0	92E0	A200
32	Home	E06C	E0F06C	E02AE047	E0C7E0AA	4700	4700	7700	-----	47E0	47E0	77E0	9700
33	Pg Up	E07D	E0F07D	E02AE049	E0C9E0AA	4900	4900	8400	-----	49E0	49E0	84E0	9900
34	Num Lock	77	F077	45	C5	Note[5]	Note[5]	-----	Note[5]	Note[5]	Note[5]	----	Note[5]
35	/	E04A	E0F04A	E035	E0B5	352F	352F	-----	-----	E02F	E02F	9500	A400
36	*	7C	F07C	37	B7	372A	372A	-----	-----	372A	372A	9600	3700
37	-	7B	F07B	4A	CA	4A2D	4A2D	-----	-----	4A2D	4A2D	8E00	4A00

KEYBOARD SCAN CODES

Key #	Key Descript.	Hardware Kybrd		Kybrd Interrupt		Standard ASCII (Scancode/ASCII code)				Extended ASCII (Scancode/ASCII code)			
		Make Code	Break Code	Make Code	Break Code	Norm	Shift	Ctrl	Alt	Norm	Shift	Ctrl	Alt
38	Tab	0D	F00D	0F	8F	0F90	0F00	-----	-----	0F09	0F00	9400	A500
39	Q or q	15	F015	10	90	1071	1051	1011	1000	1071	1051	1011	1000
40	W or w	1D	F01D	11	91	1177	1157	1117	1100	1177	1157	1117	1100
41	E or e	24	F024	12	92	1265	1245	1205	1200	1265	1245	1205	1200
42	R or r	2D	F02D	13	93	1372	1352	1312	1300	1372	1352	1312	1300
43	T or t	2C	F02C	14	94	1474	1454	1414	1400	1474	1454	1414	1400
44	Y or y	35	F035	15	95	1579	1559	1519	1500	1579	1559	1519	1500
45	U or u	3C	F03C	16	96	1675	1655	1615	1600	1675	1655	1615	1600
46	I or i	43	F043	17	97	1769	1749	1709	1700	1769	1749	1709	1700
47	O or o	44	F044	18	98	186F	184F	180F	1800	186F	184F	180F	1800
48	P or p	4D	F04D	19	99	1970	1950	1910	1900	1970	1950	1910	1900
49	{ or [	54	D054	1A	9A	1A5B	1A7B	1A1B	-----	1A5B	1A7B	1A1B	1A00
50	} or]	5B	F05B	1B	9B	1B5D	1B7D	1B1D	-----	1B5D	1B7D	1B1D	1B00
51	| or \	5D	F05D	2B	AB	2B5C	2B7C	2B1C	-----	2B5C	2B7C	2B1C	2B00
52	Delete	E071	E0F071	E02AE053	E0D3E0AA	5300	5300	-----	-----	53E0	53E0	93E0	A300
53	End	E069	E0F069	E02AE04F	E0CFE0AA	4F00	4F00	7500	-----	4FE0	4FE0	75E0	9F00
54	Page Down	E07A	E0F07A	E02AE051	E0D1E0AA	5100	5100	7600	-----	51E0	51E0	76E0	A100
55	7 or Home	6C	F06C	47	C7	4700	4737	7700	Note[6]	4700	4737	7700	Note[6]
56	8	75	F075	48	C8	4800	4838	----	Note[6]	4800	4838	8D00	Note[6]
57	9 or Page Up	7D	F07D	49	C9	4900	4939	8400	Note[6]	4900	4939	8400	Note[6]

KEYBOARD SCAN CODES

Key #	Key Descript.	Hardware Kybrd Make Code	Hardware Kybrd Break Code	Kybrd Interrupt Make Code	Kybrd Interrupt Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
58	+	79	F079	4E	CE	4E2B	4E2B	----	----	4E2B	4E2B	9000	4E00
59	Caps Lock	58	F058	3A	BA	Note 7	Note 7	----	Note 7	Note 7	Note 7	----	Note 7
60	A or a	1C	F01C	1E	9E	1E61	1E41	1E01	1E00	1E61	1E41	1E01	1E00
61	S or s	1B	F01B	1F	9F	1F73	1F53	1F13	1F00	1F73	1F53	1F13	1F00
62	D or d	23	F023	20	A0	2064	2044	2004	2000	2064	2044	2004	2000
63	F or f	2B	F02B	21	A1	2166	2146	2106	2100	2166	2146	2106	2100
64	G or g	34	F034	22	A2	2267	2247	2207	2200	2267	2247	2207	2200
65	H or h	33	F033	23	A3	2368	2348	2308	2300	2368	2348	2308	2300
66	J or j	3B	F03B	24	A4	246A	244A	240A	2400	246A	244A	240A	2400
67	K or k	42	F042	25	A5	256B	254B	250B	2500	256B	254B	250B	2500
68	L or l	4B	F04B	26	A6	266C	264C	260C	2600	266C	264C	260C	2600
69	: or ;	4C	F04C	27	A7	273B	273A	----	----	273B	273A	----	2700
70	" or '	52	F052	28	A8	2827	2822	----	----	2827	2822	----	2800
71	Enter	5A	F05A	1C	9C	1C0D	1C0D	1C0A	----	1C0D	1C0D	1C0A	1C00
72	4	6B	F06B	4B	CB	4B00	4B34	7300	Note 6	4B00	4B34	7300	Note 6
73	5	73	F073	4C	CC	-----	4C35	---	Note 6	4C00	4C35	8F00	Note 6
74	6	74	F074	4D	CD	4D00	4D36	7400	Note 6	4D00	4D36	7400	Note 6

KEYBOARD SCAN CODES

Key #	Key Descript.	Hardware Kybrd Make Code	Hardware Kybrd Break Code	Kybrd Interrupt Make Code	Kybrd Interrupt Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
76	Left Shift	12	F012	2A	AA	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]
77	Z or z	1A	F01A	2C	AC	2C7A	2C5A	2C1A	2C00	2C7A	2C5A	2C1A	2C00
78	X or x	22	F022	2D	AD	2D78	2D58	2D18	2000	2D78	2D58	2D18	2000
79	C or c	21	F021	2E	AE	2E63	2E43	2E03	2E00	2E63	2E43	2E03	2E00
80	V or v	2A	F02A	2F	AF	2F76	2F56	2F16	2F00	2F76	2F56	2F16	2F00
81	B or b	32	F032	30	B0	3062	3042	3002	3000	3062	3042	3002	3000
82	N or n	31	F031	31	B1	316E	314E	310E	3100	316E	314E	310E	3100
83	M or m	3A	F03A	32	B2	326D	324D	320D	3200	326D	324D	320D	3200
84	< or ,	41	F041	33	B3	332C	333C	-----	-----	332C	333C	-----	3300
85	> or .	49	F049	34	B4	342E	343E	-----	-----	342E	343E	-----	3400
86	? or /	4A	F04A	35	B5	352F	353F	-----	-----	352F	353F	-----	3500
87	Right Shift	59	F059	36	B6	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]	Note[8]
88	Up Arrow	E075	E0F075	E02AE048	E0C8E0AA	4800	4800	-----	----	48E0	48E0	8DE0	9800
89	1 or End	69	F069	4F	CF	4F00	4F31	7500	Note[6]	4F00	4F31	7500	Note[6]
90	2	72	F072	50	D0	5000	5032	----	Note[6]	5000	5032	9100	Note[6]
91	3 or Pg Dn	7A	F07A	51	D1	5100[9]	5133[9]	7600[9]	Note[9]	5100[9]	5133[9]	7600[9]	Note[9]
92	Left Ctrl	14	F014	1D	9D	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]
93	Left Alt	11	F011	38	B8	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]	Note[10]
94	Space	29	F029	39	B9	3920	3920	3920	3920	3920	3920	3920	3920

KEYBOARD SCAN CODES

Key #	Key Descript.	Hardware Kybrd Make Code	Hardware Kybrd Break Code	Kybrd Interrupt Make Code	Kybrd Interrupt Break Code	Standard ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt	Extended ASCII (Scancode/ASCII code) Norm	Shift	Ctrl	Alt
95	Right Alt	E011	E0F011	E038	E0B8	Note 9[10]	Note 9[10]	Note 9[10]	Note 9[10]	Note 9[10]	Note 9[10]	Note 9[10]	Note 9[10]
96	Right Ctrl	E014	E0F014	E0ID	E09D	Note	Note	Note	Note	Note	Note	Note	Note
97	Left Arrow	E06B	E0F06B	E02AE04B	E0CBE0AA	4B00	4B00	7300	-----	4BE0	4BE0	73E0	9B00
98	Down Arrow	E072	E0F072	E02AE050	E0D0E0AA	5000	5000	-----	-----	50E0	50E0	91E0	A000
99	Right Arrow	E074	E0F074	E024E04D	E0CDE0AA	4D00	4000	7400	----	4DE0	4DE0	74E0	9D00[6]
100	0 or Ins	70	F070	52	D2	5200	5230	----	Note[6]	5200	523H	9200	Note[6]
101	. or Del	71	F071	53	D3	5300	532E	----	----	5300	532E	9300	-----
102	Enter	E05A	E0F05A	E01C	E09C	1C0D	1C0D	1C0A	----	E00D	E00D	E00A	A600

NOTES

Note1 —INT O5H is invoked and a screen dump is performed
Note2 —the scroll lock active bit is toggled
Note3 —the pause state is initiated
Note4 —INT 1BH is invoked
Note5 —the numlock active bit is toggled
Note6 —ALT num pad generates raw ascii code of typed number
Note7 —the caps lock active bit is toggled
Note8 —hold shift lock active until key is released
Note9 —hold control shift active until key is released
Note10—hold alternate shift active until key is released

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