

Radio Shack[®]

Service Manual

TRS-80[®] MODEL 100 MICROCOMPUTER

26-3801

PRELIMINARY
PRODUCT
INFORMATION

0220 TECHNICAL SUPPORT SERVICES



MODEL-100

SERVICE MANUAL

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CONFIDENTIAL

SECTION 1

INTRODUCTION

System Overview

1. Specifications

(1) Main Components

(a) Keyboard

71 keys (9 x 8 matrix)

- . Alphabet keys 27
- . Number keys 10
- . Picture-control keys 7
- . Function keys 8
- . Special symbol keys 8
- . Mode keys 5
- . Other special-use keys 6

(b) LCD display

- . Display Panel . . . 240 x 64 Full-Dot matrix
1/32 duty
1/6.66 bias
- . Dot Pitch 0.8 x 0.8 mm
- . Dot Size 0.73 x 0.73 mm
- . Effective Display Area . . . 191.2 x 50.4 mm

(c) Case

- . Dimensions 300 (W) x 46.5 (L) x 215 (H) mm
- . Material ABS

(d) Operation Batteries

- . Batteries Four alkali-manganese batteries
(AM-3)
- . Operation time . . . 5 days (at 4 hours/day)
20 days (at 1 hour/day)
(note: with I/O disconnected)

(e) Memory Protection Battery (on main PWB)

- . Battery Rechargeable Battery (3-51FT)
- . Protection time . . . About 40 days (8 KB)
About 10 days (32 KB)
- . Recharge method . . . Trickle charge by AC adaptor,
or operation batteries

(f) LSIs

- CPU . . . 80C85 (OKi)
Code and pin compatible with 8085
- ROM . . . Max. 64 KB (2 Banks of 32 KB)
STANDARD 32 KB
OPTION 32 KB
- RAM . . . Max. 32 KB
STANDARD 8 KB (four TC5518BF (TOSHIBA))
RAM PACK
incremental 8 KB RAM PACK on PWB
- CLOCK/CALENDAR . . . μ PD 1990AC (NEC)
No leap year/No February 29

(2) I/O Interface

(a) RS-232C

- Conforms to EIA standards
- Signal . . . TXR (Transmit Data)
RXR (Receive Data)
RTSR (Request To Send)
CTSR (Clear To Send)
DSRR (Data Set Ready)
DTRR (Data Terminal Ready)

Programmable Items

- * Data Length . . . 6, 7 or 8 bits
- * Parity NON, EVEN or ODD
- * Stop Bit Length . . 1 or 2 bits
- * Baud Rate 75, 110, 300, 600, 1200, 2400, 4800,
9600, 19200 BPS

- Maximum Transmission Distance . . . 5m
- Driver maximum voltage output . . . \pm 5V
- Driver minimum voltage output . . . \pm 3.5V
- Receiver maximum voltage input . . . \pm 18V
- Receiver minimum voltage input . . . \pm 3V

- (b) Modem/Coupler
 - Conforms to BEL103 standards
 - . Baud Rate . . . 300BPS
 - . Programmable Items
 - * Date Length . . . 6, 7 or 8 bits
 - * Parity NON EVEN or ODD
 - * Stop bit 1 or 2 bits
 - . Full Duplex Answer mode / Call mode, switchable
 - . Other Functions . . . Hang Up Function
Auto Dialer Function

- (c) Audio Cassette Interface
 - . Data Rate . . . 1,500 BPS
(MARK: 2,400 Hz, SPACE: 1,200 Hz)

- (d) Printer Interface
 - Conforms to Centronics Interface standards
 - . Handshake Signal . . . STROBE, BUSY, SELECT

(3.) Special functions

- (a) Automatic power OFF

When there is no program operation (awaiting command) for ten minutes, the power is automatically cut off. If the PPC is started once again, the power switch is to be switched OFF and then ON, thus releasing the automatic power OFF condition.

The display will remain the same as before the power was cut off.

2. Connectors, Switches and Contrast Volume

(1) Connectors

- RS-232C 25 pins (DB-25S)
- Printer 26 pins (FRC2-C26-L13-ON)
- Modem 8 pins (TCS-4490)
- Cassette 8 pins (TCS-4480)
- Bar Code Reader 9 pins (A-7224)
- System Bus 40 pins (IC Socket)
- AC Adaptor 5.5 ϕ (Center Minus)

(2) Switches

(a) Power Switch

This is the PPC system power switch.



Power OFF

Power ON

Fig. 1

(b) ANS/CALL selector

This switch is used to select the MODEM ANSWER mode or CALL mode.



Call mode

Answer mode

Fig. 2

(c) Coupler/telephone selector

This switch is used to select COUPLER (acoustic coupler connection) or TELEPHONE (direct connection).



COUPLER (ACOUSTIC COUPLER CONNECTION)

TELEPHONE (DIRECT TELEPHONE LINE CONNECTION)

Fig. 3

(d) MEMORY BACK UP Switch

This switch is for prevention of overdischarge of the Ni-Cd battery for RAM back-up. The HHC will not operate regardless of the setting of the power switch, unless this switch is ON.

Set this switch to OFF if the unit is not to be used for a long time.

Note that the RAM will not be backed up when this switch is set to OFF.

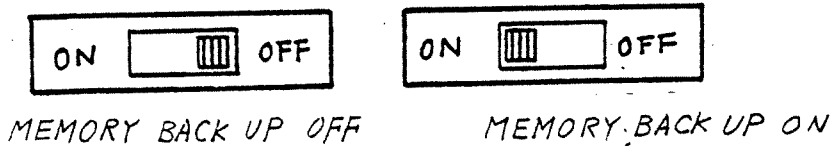


Fig. 4

(e) Reset switch (push switch)

This switch initializes (resets) the system. A cold start can be obtained by pressing it at the same time the **SHIFT** Key and **BRAKE** Key are pressed.

(3) DISP volume

This is for adjustment of contrast of the LCD relative to the viewing angle.

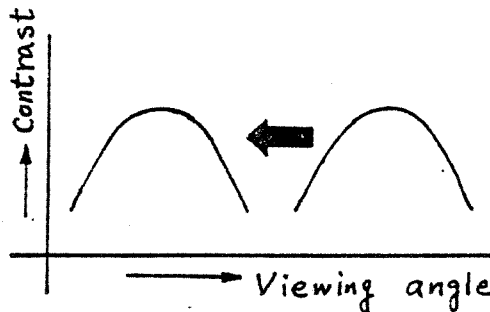
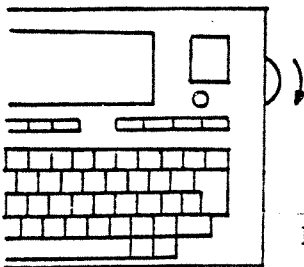
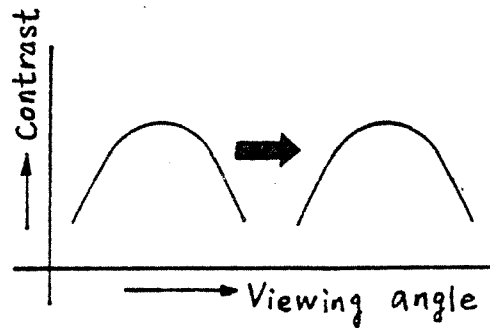
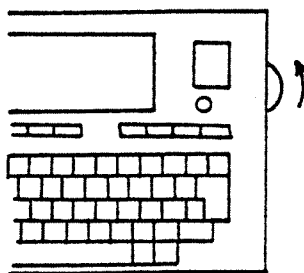
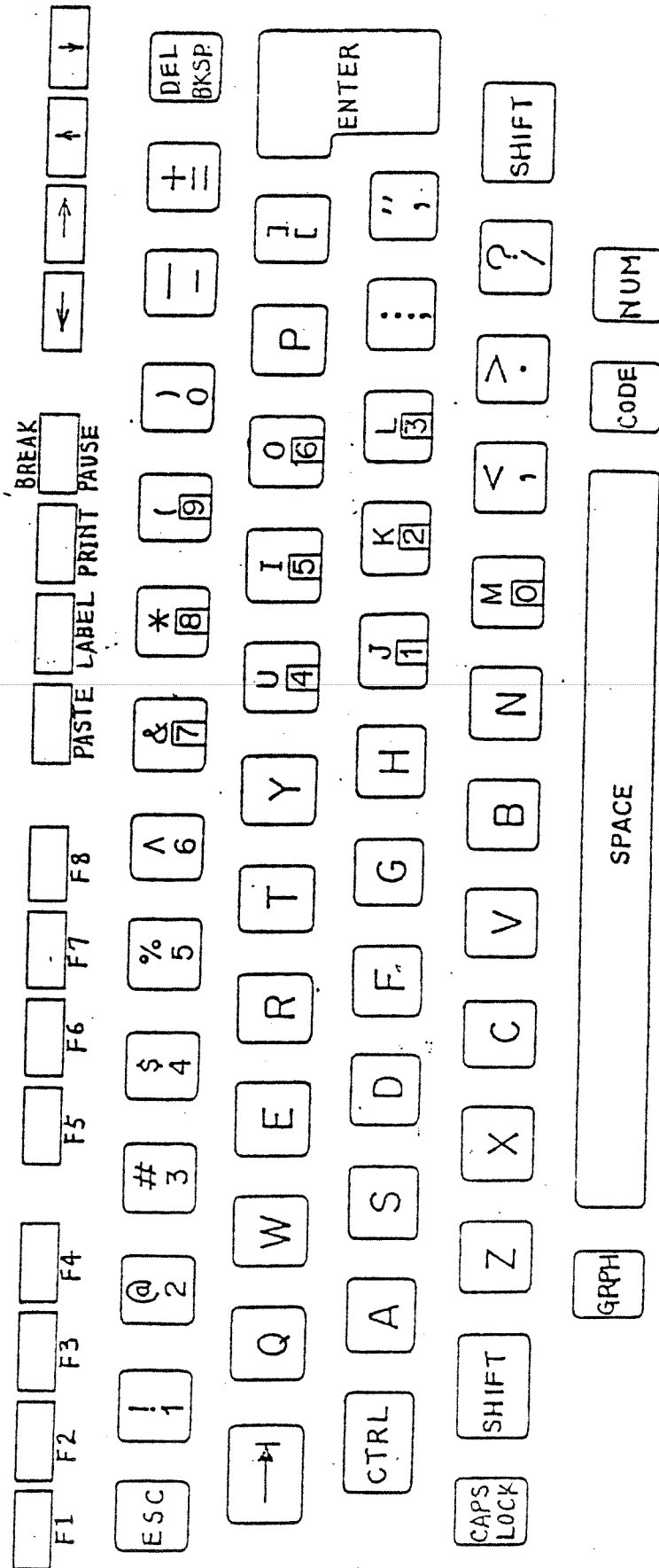
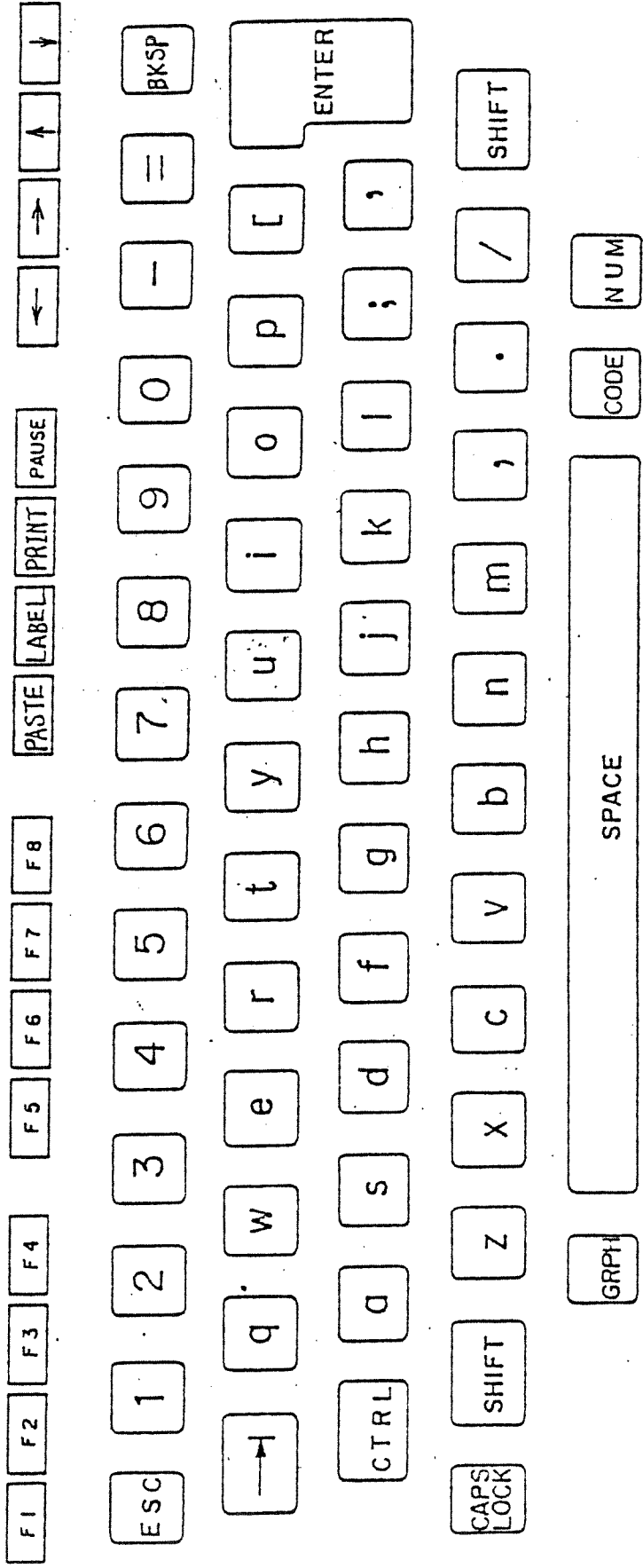


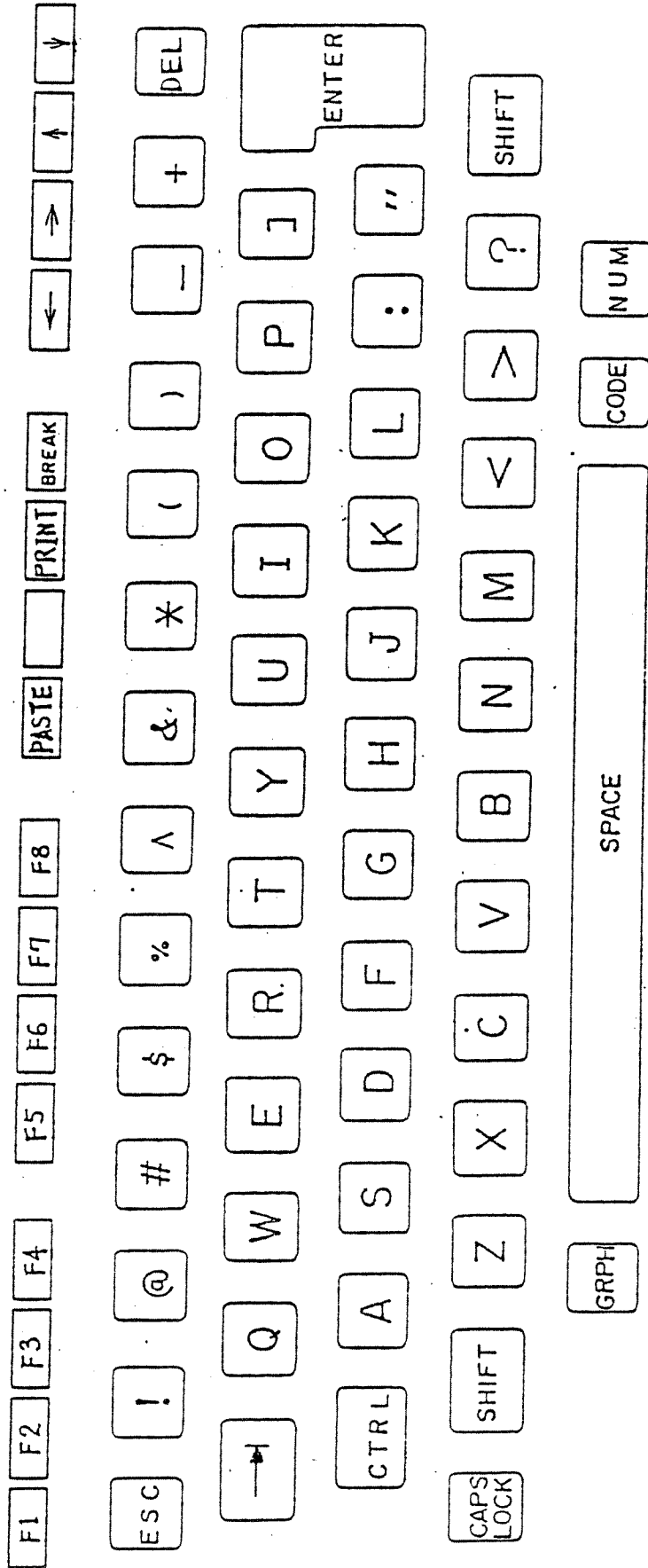
Fig. 5



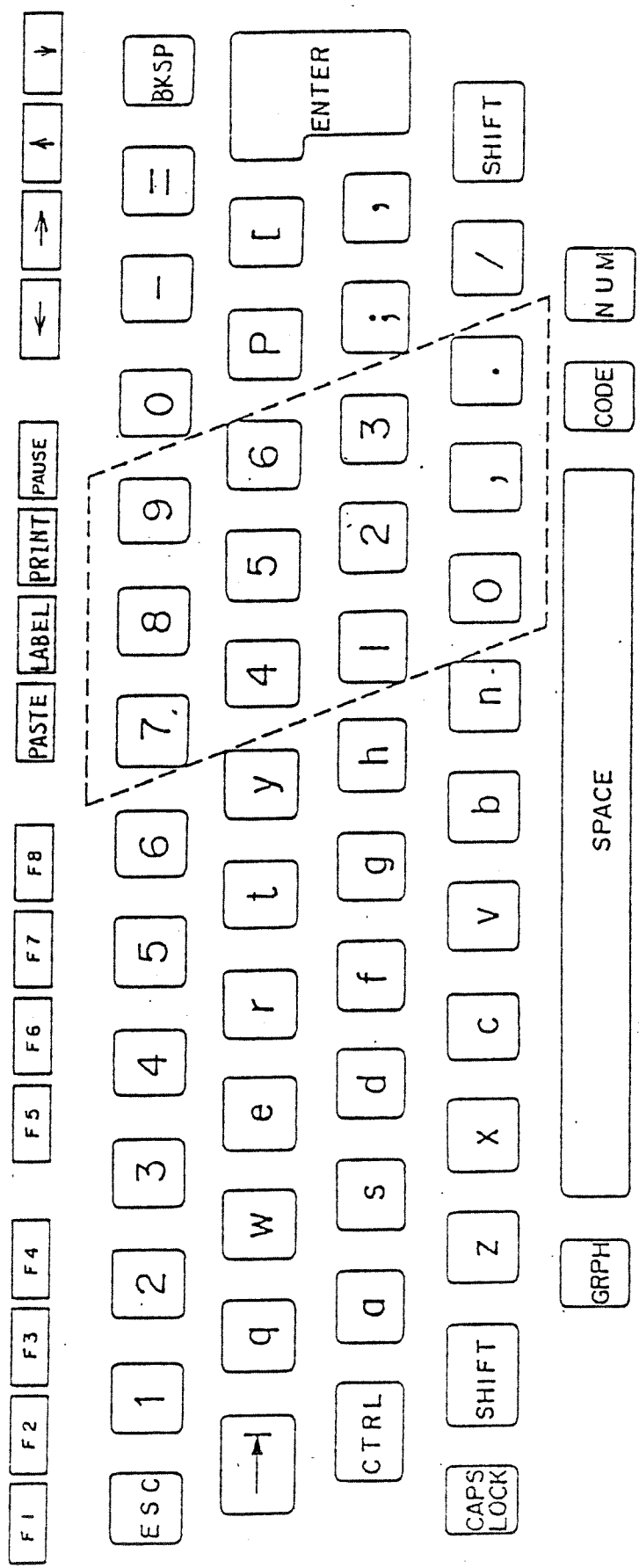
MODEL 100 - KEY TOP LAYOUT



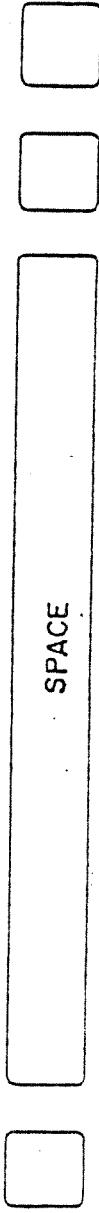
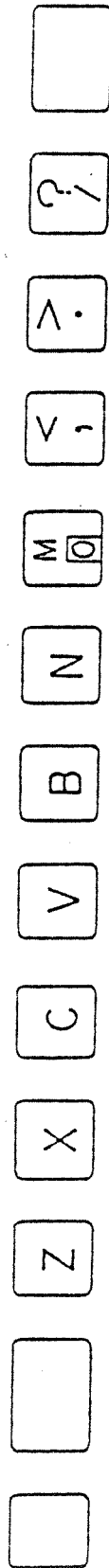
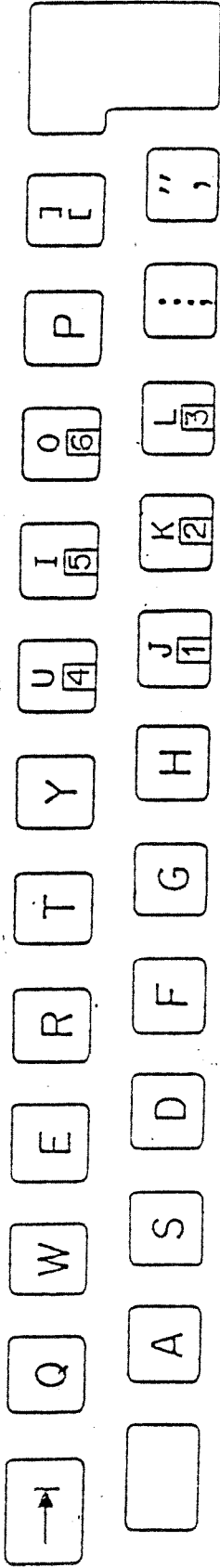
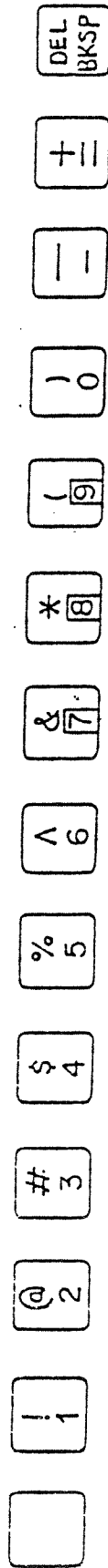
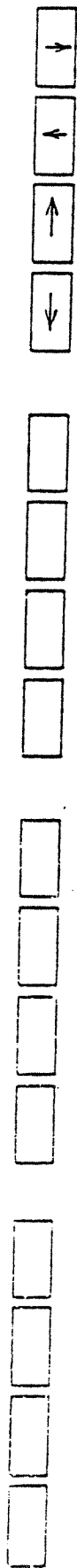
KEY DISPLAY WITHOUT PUSHING THE SHIFT KEY



KEY DISPLAY WITH SHIFT KEY IS PUSHED.



PUSH THE NUM KEY ONCE THUS ABLE TO USE THE KEYS INSIDE THE DOTTED LINE AS A TEN KEY.



THE REPEAT FUNCTION IS AVAILABLE IN THOSE KEYS WITH CHARACTERS AND SIGM MARKS DISPLAYED ON THE KEY-TOP.

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SERVICE MANUAL

Pages 15, 16, 17, and 18

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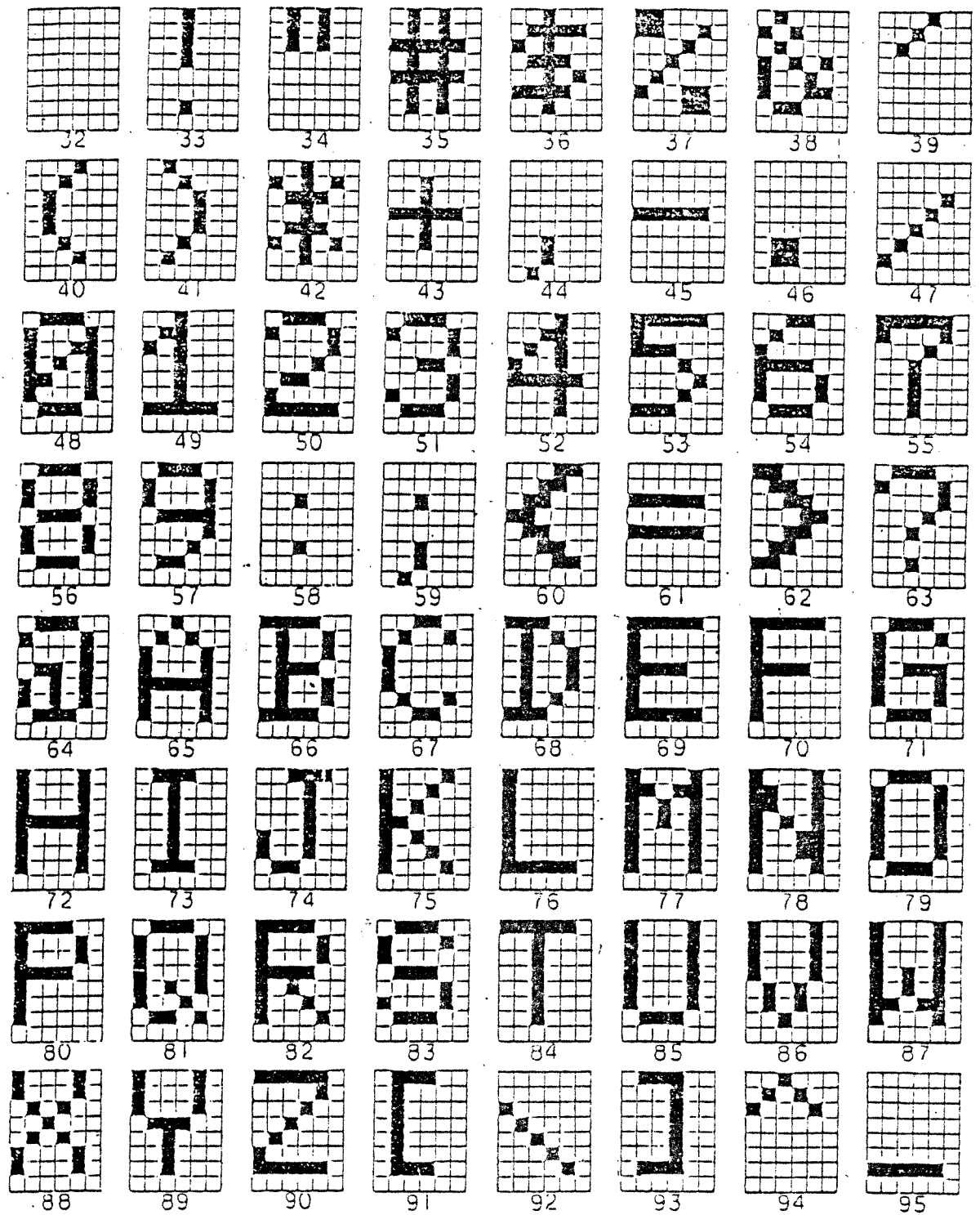


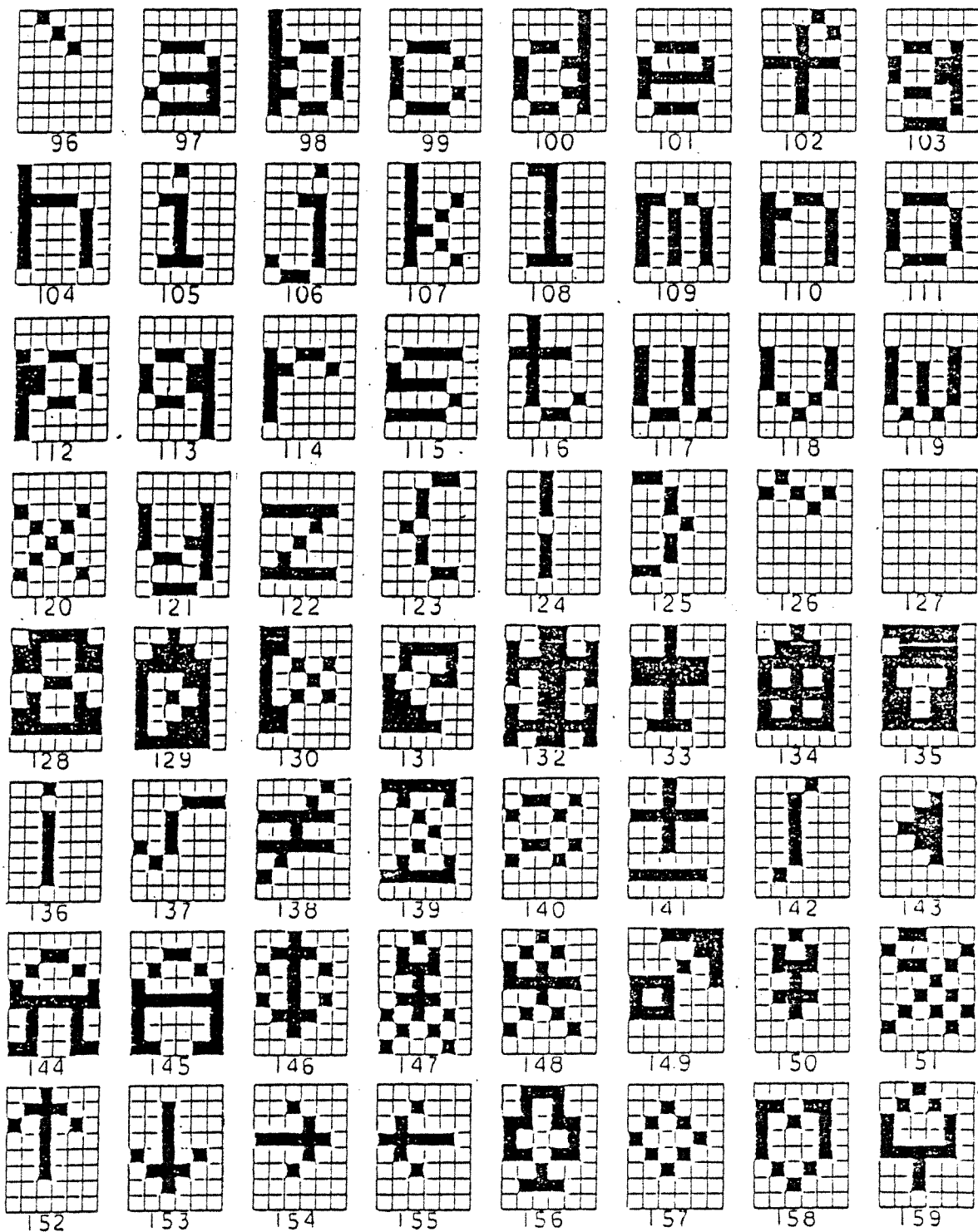


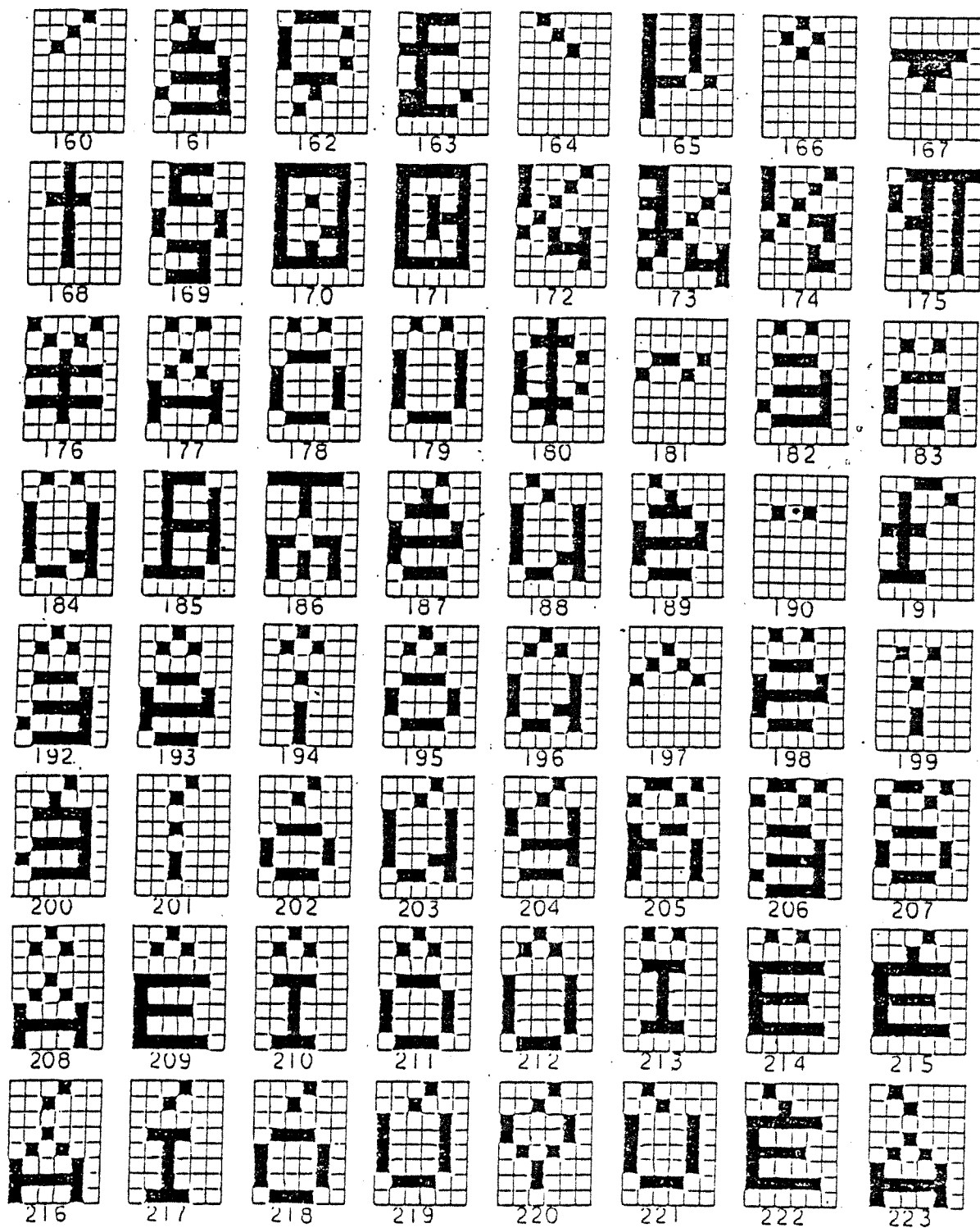


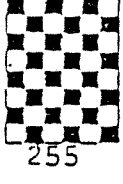
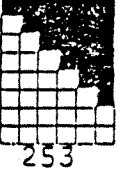
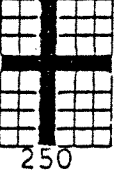
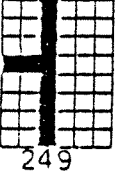
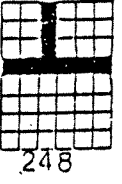
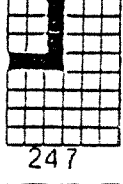
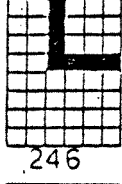
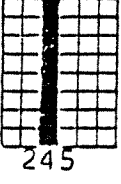
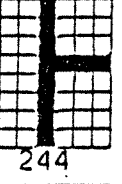
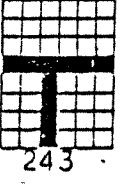
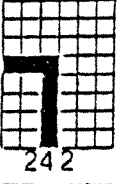
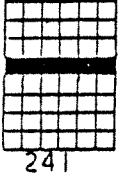
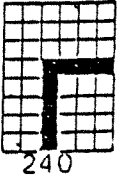
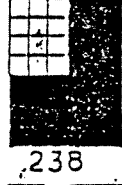
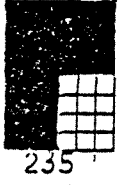
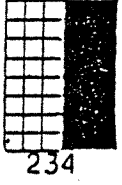
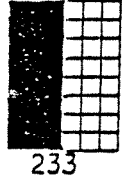
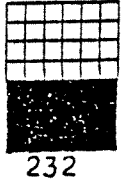
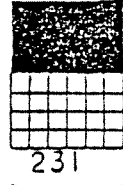
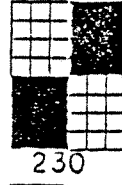
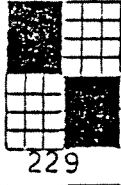
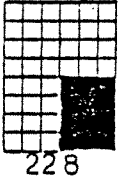
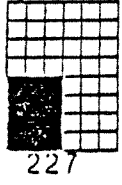
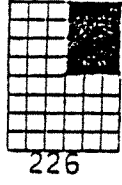
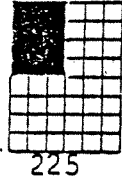
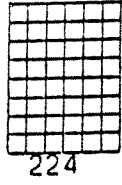


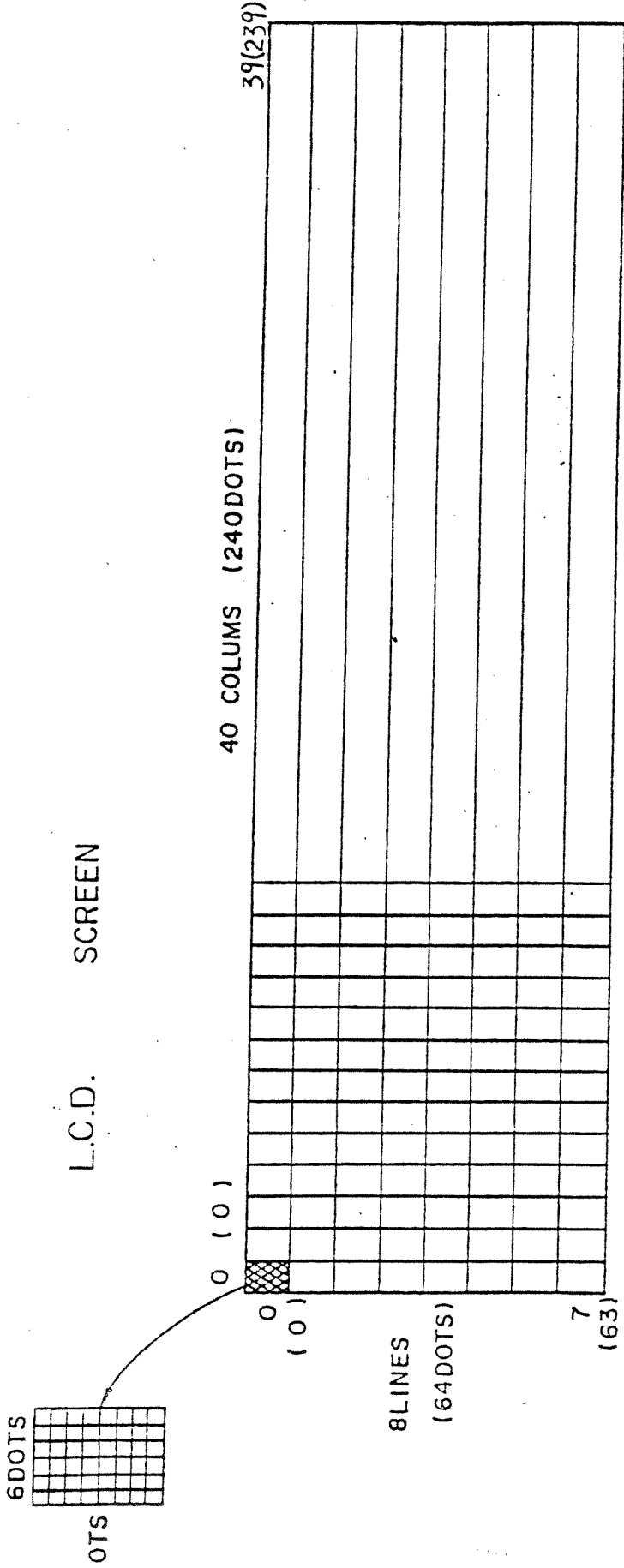












B-5 VIDEO DISPLAY WORKSHEET

SECTION II

DISASSEMBLY/REASSEMBLY

DISASSEMBLY

1. CASES

- (1) Disconnect the cables connected to the unit. Next, being careful not to scratch the key top, turn it over and remove the 4 screws from the upper and lower cases.
- (2) Remove the upper case so that it opens to the right side. Note that the upper and lower cases are secured by *snaps*. Also, don't apply too much force when pulling open, because the LCD and K/B connectors are attached.
- (3) Remove the LCD and K/B connectors from the main PWB.
- (4) Remove the buzzer connector from the LCD PWB.

2. K/B PWB

- (1) Remove the 5 screws, and then remove the K/B PWB.
- (2) Remove the K/B supports at the same time.

3. LCD PWB

- (1) Remove the 4 screws, and then remove the K/B PWB.

4. MAIN PWB

- (1) Remove the 7 screws.
- (2) Remove the main PWB upward. Be careful when removing the reset switch and battery contact spring.

REASSEMBLY

1. MAIN PWB

- (1) Align the screw positions of the lower case with the main PWB. Gently insert the main PWB from the rear and place the reset switch knob in the proper notch.
- (2) Secure the battery contact spring.
- (3) Attach the main PWB to the lower case by using the seven M3 x 8 screws.

2. LCD PWB

- (1) Attach the LCD PWB to the upper case by using the four M3 x 3 screws.
- (2) Insert the buzzer connector in the LCD PWB.

3. K/B PWB

- (1) Align the 2 K/B supports with the holes in the PWB, and attach them so that they fit to the PWB edge.
- (2) Align the K/B supports and K/B PWB holes with the upper case screws.
- (3) Attach the K/B supports and K/B PWB to the upper case by using the five M3 x 8 screws.

4. CASES

- (1) Turn the upper case over to the right side of the lower case. Be careful not to scratch the key top.
- (2) Attach the LCD and K/B connectors to the main PWB.
- (3) Then place the upper case over the lower case, taking care that the cable is not pulled.
- (4) Align the upper and lower cases so that the tabs fit well.
- (5) Turn the cases over, and secure them together by using the four M3 x 8 screws.

SECTION III

MAIN P.W. BOARD

TECHNICAL DESCRIPTION

As described below, the technical description of the Model 100 main P.W. board is divided into 16 sections.

1. LSIs
2. MEMORY
3. ADDRESS DECODING & BANK SELECTION
4. MEMORY MAP
5. I/O MAP & I/O PORT DESCRIPTION
6. KEYBOARD
7. CASSETTE INTERFACE CIRCUIT
8. PRINTER INTERFACE CIRCUIT
9. BAR CODE READER INTERFACE CIRCUIT
10. BUZZER CONTROL CIRCUIT
11. SYSTEM BUS
12. LCD INTERFACE CIRCUIT
13. CLOCK CIRCUIT
14. SERIAL INTERFACE
15. POWER SUPPLY & AUTO POWER OFF CIRCUIT
16. RESET CIRCUIT

1. LSIs

(1) MSM80C85ARS (CPU)

1-chip, 8-bit C-MOS Process Microprocessors

The MSM80C85ARS (80C85) is a complete 8-bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance with a higher system speed.

The 80C85 uses a multiplexed data bus. The address is split between the 8-bit address bus and the 8-bit data bus.

For the Model 100, the data bus and address bus are separated by M1 (TC40H373P: octal "D" type latch).

The driveability of the bus line is increased by M2 (TC40H24^Y₅P: octal bi-directional bus buffer) and M21 (TC40H244P: octal buffer/driver).

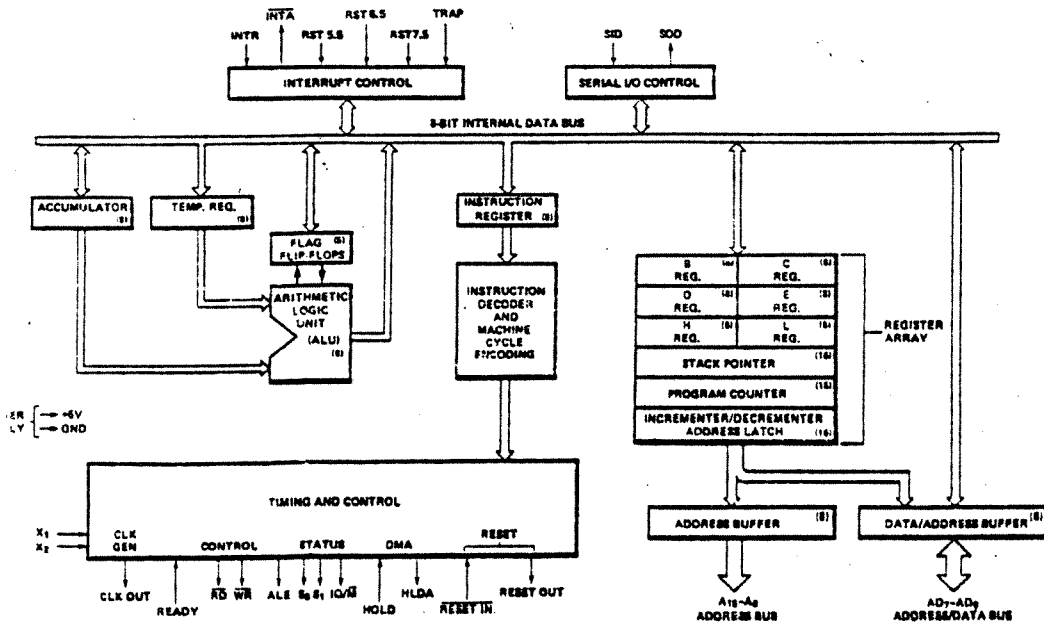


Fig. 1 80C85 CPU FUNCTIONAL BLOCK DIAGRAM

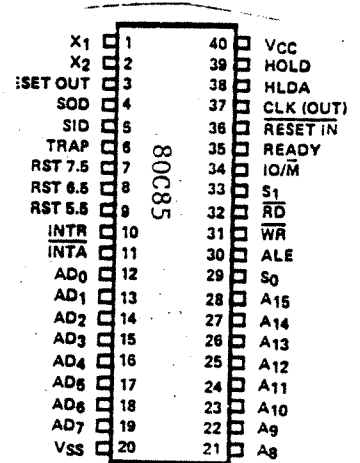


Fig. 2 80C85 Pinout Diagram

(a) 80C85 FUNCTIONAL PIN DESCRIPTION

The following describes the function of each pin:

Symbol

Function

A₈ – A₁₅
(Output, 3-state)

Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.

AD₀₋₇
(Input/Output, 3-state)

Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.

ALE
(Output)

Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.

Symbol
S₀, S₁, and IO/M
(Output)

Function

Machine cycle status:

IO/M	S ₁	S ₀	Status
0	0	1	Memory write
0	1	0	Memory read
1	0	1	I/O write
1	1	0	I/O read
0	1	1	Opcode fetch
1	1	1	Interrupt Acknowledge
*	0	0	Halt
*	X	X	Hold
*	X	X	Reset

* = 3-state (high impedance)

X = unspecified

S₁ can be used as an advanced R/W status. IO/M, S₀ and S₁ become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.

RD
(Output, 3-state)

READ control: A low level on RD indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.

WR
(Output, 3-state)

WRITE control: A low level on WR indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR. 3-stated during Hold and Halt modes and during RESET.

READY
(Input)

If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle.

Symbol	Function
HOLD (Input)	HOLD indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, RD, WR, and IO/M lines are 3-stated.
HLDA (Output)	HOLD ACKNOWLEDGE: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.
INTR (Input)	INTERRUPT REQUEST: is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an INTA will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
INTA (Output)	INTERRUPT ACKNOWLEDGE: is used instead of (and has the same timing as) RD during the Instruction cycle after an INTR is accepted.
RST 5.5 RST 6.5 RST 7.5 (Inputs)	RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.

Symbol	Function
TRAP (Input)	Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 1.)
RESET IN (Input)	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. RESET IN is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The cpu is held in the reset condition as long as RESET IN is applied.
RESET OUT (Output)	Indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X ₁ , X ₂ (Input)	X ₁ and X ₂ are connected to a crystal, LC, or RC network to drive the internal clock generator. X ₁ can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK (Output)	Clock Output for use as a system clock. The period of CLK is twice the X ₁ , X ₂ input period.
SID (Input)	Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD (Output)	Serial output data line. The output SOD is set or reset as specified by the SIM instruction.
Vcc	+5 volt supply.
Vss	Ground Reference.

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note (2).	High level until sampled.

Table 1. INTERRUPT PRIORITY, RESTART ADDRESS and SENSITIVITY

(b) FUNCTIONAL DESCRIPTION

The 80C85 has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 80C85 register set is as follows:

<u>Mnemonic</u>	<u>Register</u>	<u>Contents</u>
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Registers: data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The 80C85 uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The 80C85 provides RD, WR, S₀, S₁, and IO/M signals for bus control. An Interrupt Acknowledge signal (INTA) is also provided. HOLD, READY, and all Interrupts are synchronized with the processor's internal clock. The 80C85 also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the 80C85 has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

(c) INTERRUPT AND SERIAL I/O

The 80C85 has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is non-maskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 1.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a RESET IN to the 80C85. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and RESET IN.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP – highest priority, RST 7.5, RST 6.5, RST 5.5, INTR – lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 3 illustrates the TRAP interrupt request circuitry within the 8085. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

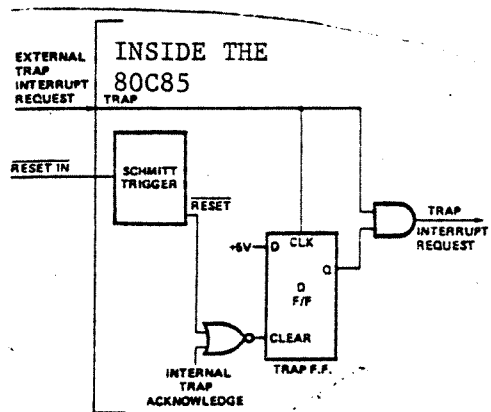


Fig.3 TRAP and RESET IN CIRCUIT

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5-7.5 will provide current Interrupt Enable status, revealing that Interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is ready by RIM, and SIM sets the SOD data.

(d) BASIC SYSTEM TIMING

The 80C85 has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Fig. 4 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines (IO/M, S₁, S₀) and the three control signals (RD, WR, and INTA). (See Table 2.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the T₁ state, at the outset of each machine cycle. Control lines RD and WR become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OP CODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of READY or HOLD inputs). Any T state must be one of ten possible states, shown in Table 3.

MACHINE CYCLE	STATUS			CONTROL		
	IO/M	S1	S0	RD	WR	INTA
OPCODE FETCH (OF)	0	1	1	0	1	1
MEMORY READ (MR)	0	1	0	0	1	1
MEMORY WRITE (MW)	0	0	1	1	0	1
I/O READ (IOR)	1	1	0	0	1	1
I/O WRITE (IOW)	1	0	1	1	0	1
ACKNOWLEDGE OF INTR (INA)	1	1	1	1	1	0
BUS IDLE (BI): DAD ACK. OF RST, TRAP HALT	0 1 TS	1 1 0	1 1 0	1 1 TS	1 1 TS	1 1 1

Table 2 80C85 MACHINE CYCLE CHART

Machine State	Status & Buses				Control		
	S1, S0	IO/M	A ₈ -A ₁₅	AD ₀ -AD ₇	RD, WR	INTA	ALE
T ₁	X	X	X	X	1	1	1
T ₂	X	X	X	X	X	X	0
T _{WAIT}	X	X	X	X	X	X	0
T ₃	X	X	X	X	X	X	0
T ₄	1	0	X	TS	1	1	0
T ₅	1	0	X	TS	1	1	0
T ₆	1	0	X	TS	1	1	0
T _{RESET}	X	TS	TS	TS	TS	1	0
T _{HALT}	0	TS	TS	TS	TS	1	0
T _{HOLD}	X	TS	TS	TS	TS	1	0

Table 3 80C85 MACHINE STATE CHART

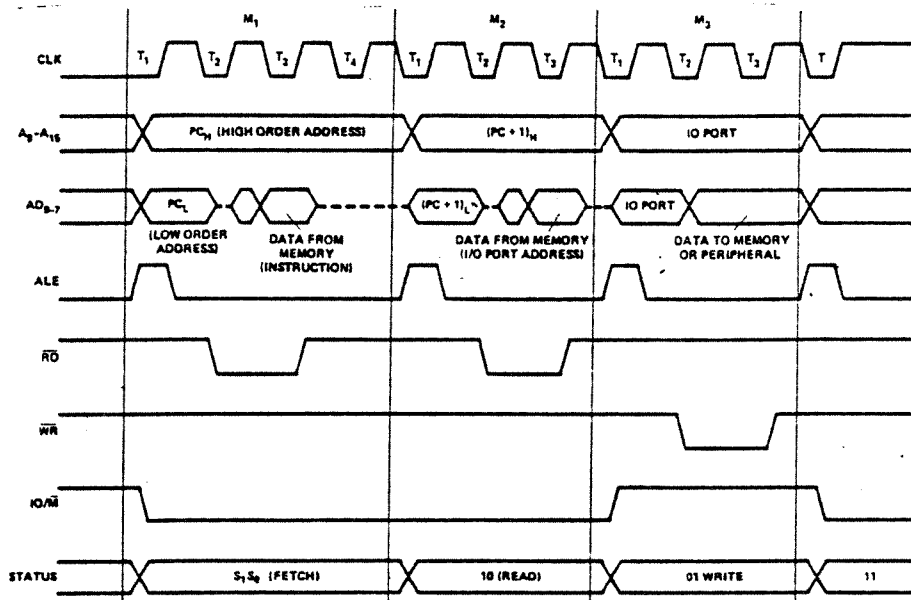


Fig. 4 80C85 Basic System Timing

Ambient Temperature Under Bias.....-40°C to +85°C
 Storage Temperature.....-55°C to +150°C
 Voltage on Any Pin
 With Respect to Ground.....-0.5°C to +7 V
 Power Dissipation.....1.0 Watt

Table 4 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.3	+0.8	V	
V_{IH}	Input High Voltage	2.2	$V_{CC}+0.3$	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2\text{mA}$
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\mu\text{A}$
I_{CC}	Power Supply Current		17	mA	$V_{CC}=4.75-5.25\text{ V}$
I_{IL}	Input Leakage		± 10	μA	$V_{in} = V_{CC}$
I_{LO}	Output Leakage		± 10	μA	$0.45\text{V} \leq V_{out} \leq V_{CC}$
V_{ILR}	Input Low Level, RESET	-0.3	+0.8	V	
V_{IHR}	Input High Level, RESET	2.2	$V_{CC}+0.3$	V	

Table 5 D.C. CHARACTERISTICS

t_{AL}	-	(1/2) T - 45	MIN
t_{LA}	-	(1/2) T - 60	MIN
t_{LL}	-	(1/2) T - 20	MIN
t_{LCK}	-	(1/2) T - 60	MIN
t_{LC}	-	(1/2) T - 30	MIN
t_{AD}	-	(5/2 + N) T - 225	MAX
t_{RD}	-	(3/2 + N) T - 180	MAX
t_{RAE}	-	(1/2) T - 10	MIN
t_{CA}	-	(1/2) T - 40	MIN
t_{OW}	-	(3/2 + N) T - 60	MIN
t_{WD}	-	(1/2) T - 60	MIN
t_{CC}	-	(3/2 + N) T - 80	MIN
t_{CL}	-	(1/2) T - 110	MIN
t_{ARY}	-	(3/2) T - 260	MAX
t_{HACK}	-	(1/2) T - 50	MIN
t_{HABF}	-	(1/2) T + 50	MAX
t_{HARE}	-	(1/2) T + 50	MAX
t_{AC}	-	(2/2) T - 50	MIN
t_1	-	(1/2) T - 80	MIN
t_2	-	(1/2) T - 40	MIN
t_{RV}	-	(3/2) T - 80	MIN
t_{LDR}	-	(4/2) T - 180	MAX

Table 6 Bus Timing Specification

TABLE 7 A.C. CHARACTERISTICS
T_A = 40°C to +85°C; V_{CC} = 5V ±10%; V_{SS} = 0V

Symbol	Parameter	Min.	Max.	Units
t _{CYC}	CLK Cycle Period	320	2000	ns
t ₁	CLK Low Time — Standard 150 pF Loading	80		ns
t ₂	CLK High Time — Standard 150 pF Loading	120		ns
t _{r, tf}	CLK Rise and Fall Time		30	ns
t _{XKR}	X ₁ Rising to CLK Rising	30	120	ns
t _{XKF}	X ₁ Rising to CLK Falling	30	150	ns
t _{AC}	A ₈₋₁₅ Valid to Leading Edge of Control ⁽¹⁾	270		ns
t _{ACL}	A ₀₋₇ Valid to Leading of Control	240		ns
t _{AD}	A ₀₋₁₅ Valid to Valid Data In		575	ns
t _{AFR}	Address Float after Leading Edge of READ (INTA)		0	ns
t _{AL}	A ₈₋₁₅ Valid before Trailing Edge of ALE ⁽¹⁾	115		ns
t _{ALL}	A ₀₋₇ Valid before Trailing Edge of ALE	90		ns
t _{ARY}	READY Valid from Address Valid		220	ns
t _{CA}	Address (A ₈ -A ₁₅) Valid after Control	120		ns
t _{CC}	Width of Control Low (RD, WR, INTA) Edge of ALE	400		ns
t _{CL}	Trailing Edge of Control to Leading Edge of ALE	50		ns
t _{DW}	Data Valid to Trailing Edge of WRITE	420		ns
t _{HABE}	HLDA to Bus Enable		210	ns
t _{HABF}	Bus Float after HLDA		210	ns
t _{HACK}	HLDA Valid to Trailing Edge of CLK	110		ns
t _{HDH}	HOLD Hold Time	0		ns
t _{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		ns
t _{INH}	INTR Hold Time	0		ns
t _{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160		ns
t _{LA}	Address Hold Time after ALE	100		ns
t _{LC}	Trailing Edge of ALE to Leading Edge of Control	130		ns
t _{LCK}	ALE Low during CLK High	100		ns
t _{LDR}	ALE to Valid Data during Read		460	ns
t _{LDW}	ALE to Valid Data during Write		200	ns
t _{LL}	ALE Width	140		ns
t _{LRY}	ALE to READY Stable		110	ns
t _{RAE}	Trailing Edge of READ to Re-Enabling of Address	150		ns
t _{RD}	READ (or INTA) to Valid Data		300	ns
t _{RV}	Control Trailing Edge to Leading Edge of Next Control	400		ns
t _{RDH}	Data Hold Time After READ INTA ⁽⁷⁾	0		ns
t _{RYH}	READY Hold Time	0		ns
t _{RYS}	READY Setup Time to Leading Edge of CLK	110		ns
t _{WD}	Data Valid After Trailing Edge of WRITE	100		ns
t _{WDL}	LEADING Edge of WRITE to Data Valid		40	ns

Notes:

- 1. A₈-A₁₅ address Specs apply to IO/M, S₀, and S₁ except A₈-A₁₅ are undefined during T₄-T₆ of OF cycle whereas IO/M, S₀, and S₁ are stable.
- 2. Test conditions: t_{CYC} = 320ns C_L = 150 pF
- 3. All timings are measured at output voltage V_L = 0.8V, V_H = 2.2V and 1.5V with 20ns rise and tail time on inputs.

(e) WAVEFORM

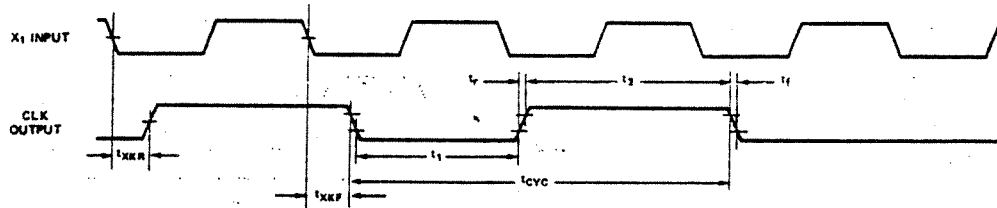
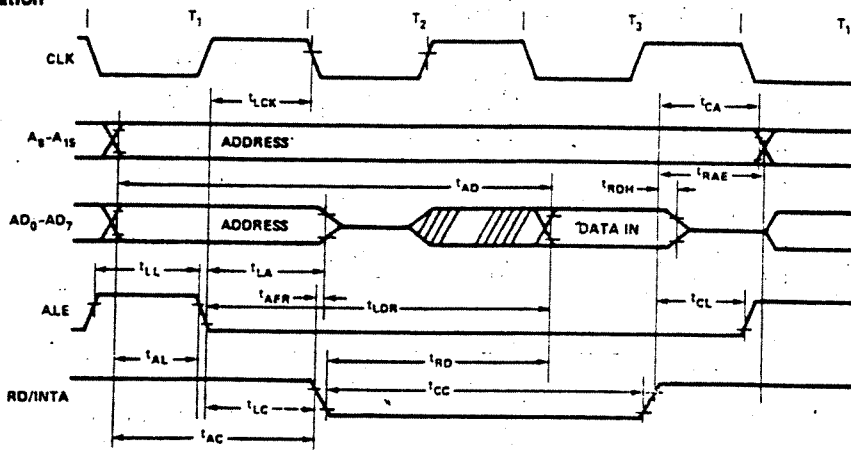
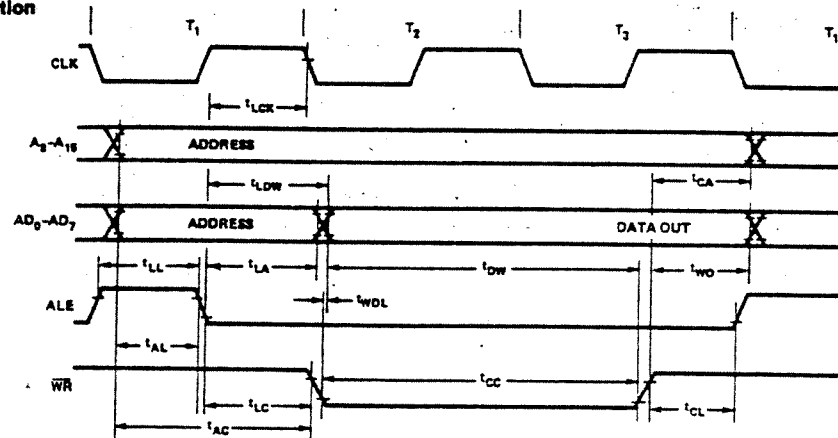


Fig . 5 Clock Timing Waveform

Read Operation



Write Operation



Read operation with Wait Cycle (Typical) — same READY timing applies to WRITE operation.

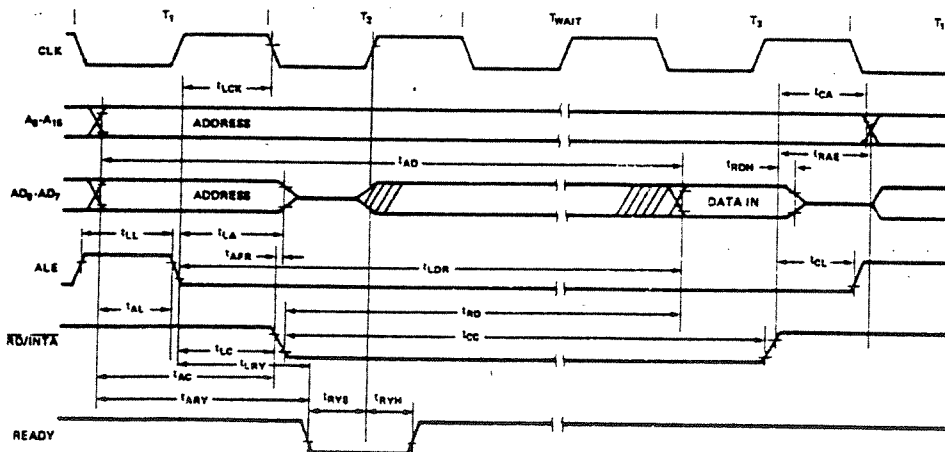


Fig. 6 80C85 Bus Timing

Hold Operation

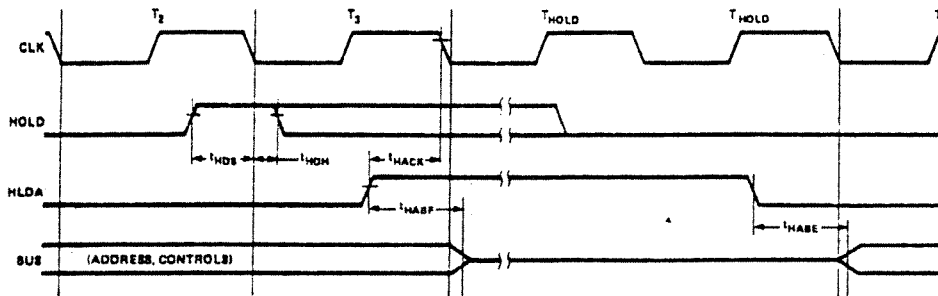


Fig. 7 Hold Timing

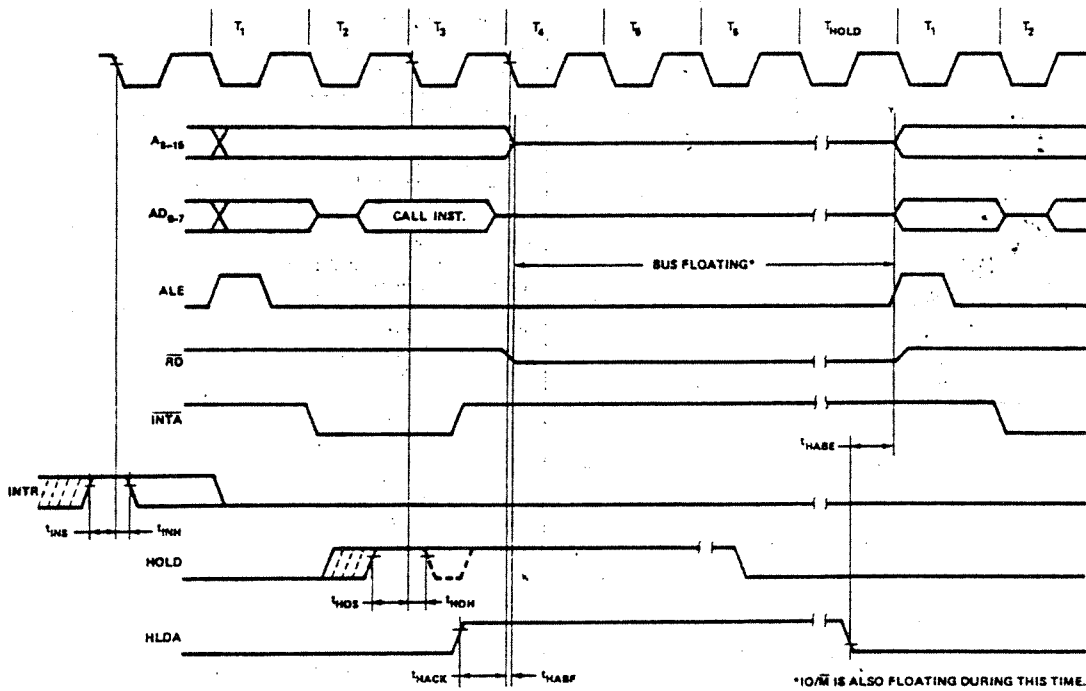


Fig. 8 80C85 Interrupt and Hold Timing

(2) MSM81C55RS (PIO)

C-MOS, 2048-bit STATIC RAM with i/o PORTS and TIMER
 The i/o portion consists of three general purpose i/o ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on the chip to provide either a square wave or terminal count pulse for the CPU system, depending on the timer mode.

The 81C55 RAM is not used in Model 100. A timer/counter is used as the clock generator necessary for communication and to generate the melody.

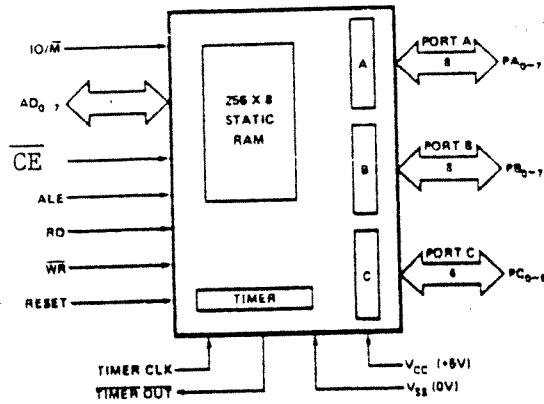
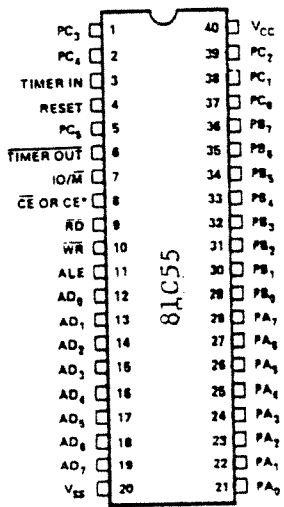


Fig 9 Pin Configuration and Block Diagram

(a) 81C55 PIN FUNCTIONS

Symbol	Function
RESET (Input)	Pulse provided by the 80C85 to initialize the system (connect to 80C85 RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 80C85 clock cycle times.
AD ₀₋₇ (Input)	3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 81C55 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/M input. The 8-bit data is either written into the chip or read from the chip, depending on the WR or RD input signal.
CE (Input)	Chip Enable: CE is ACTIVE LOW.
RD (Input)	Read control: Input low on this line with the Chip Enable active enables and AD ₀₋₇ buffers. If O/M pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
WR (Input)	Write control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register depending on IO/M.
ALE	Address Latch Enable: This control signal latches both the address on the AD ₀₋₇ lines and the state of the Chip Enable and IO/M into the chip at the falling edge of ALE.
IO/M (Input)	Selects memory if low and I/O and command/status registers if high.

PA₀₋₇ (8)
(Input/Output)

These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.

PB₀₋₇ (8)
(Input/Output)

These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.

PC₀₋₅ (6)
(Input/Output)

These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC₀₋₅ are used as control signals, they will provide the following:

- PC₀ - A INTR (Port A Interrupt)
- PC₁ - ABF (Port A Buffer Full)
- PC₂ - A STB (Port A Strobe)
- PC₃ - B INTR (Port B Interrupt)
- PC₄ - B BF (Port B Buffer Full)
- PC₅ - B STB (Port B Strobe)

TIMER IN
(Input)

Input to the counter-timer.

TIMER OUT
(Output)

Timer output. This output can be either a square wave or a pulse depending on the timer mode.

Vcc

+5 volt supply.

Vss

Ground Reference.

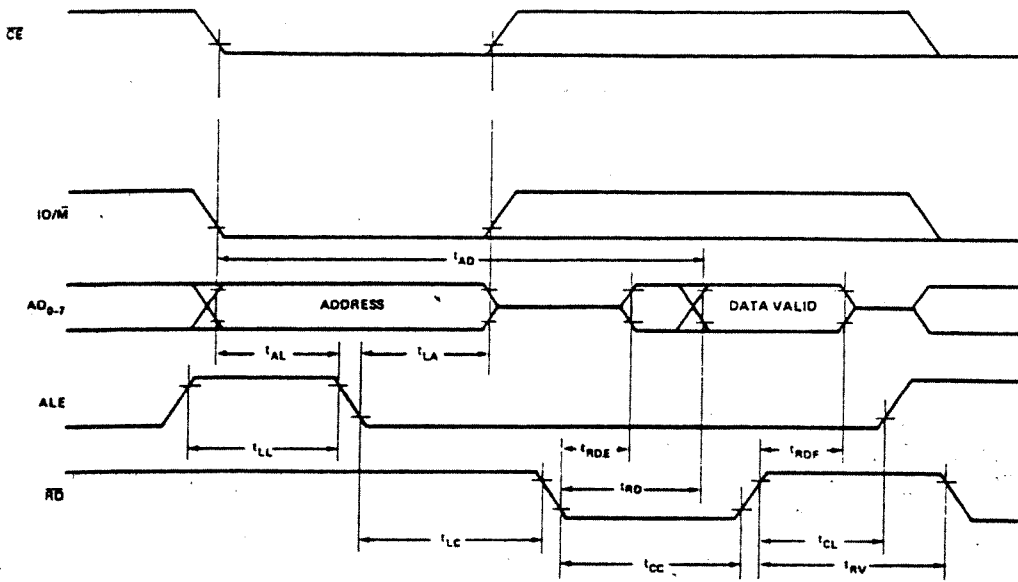
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V _{IL}	Input Low Voltage	-0.3V	0.8	V	
V _{IH}	Input High Voltage	2.2	V _{CC} - 0.3	V	
V _{OL}	Output Low Voltage		0.45	V	I _{OL} = 2mA
V _{OH}	Output High Voltage	2.4		V	I _{OH} = -400μA
I _{IH}	Input Leakage		±10	μA	V _{IN} = V _{CC} to 0V
I _{LO}	Output Leakage Current		±10	μA	0.45V < V _{OUT} < V _{CC}
I _{CC}	V _{CC} Supply Current		5	mA	

Table 8 D.C. characteristics

		nsec	
SYMBOL	PARAMETER	MIN.	MAX.
t _{AL}	Address to Latch Set Up Time	50	
t _{LA}	Address Hold Time after Latch	80	
t _{LC}	Latch to READ/WRITE Control	100	
t _{RD}	Valid Data Out Delay from READ Control		170
t _{AD}	Address Stable to Data Out Valid		400
t _{LL}	Latch Enable Width	100	
t _{RDF}	Data Bus Float After READ	0	100
t _{CL}	READ/WRITE Control to Latch Enable	20	
t _{CC}	READ/WRITE Control Width	250	
t _{OW}	Data In to WRITE Set Up Time	150	
t _{WD}	Data In Hold Time After WRITE	0	
t _{RV}	Recovery Time Between Controls	300	
t _{WP}	WRITE to Port Output		400
t _{PR}	Port Input Setup Time	70	
t _{RP}	Port Input Hold Time	50	
t _{SBF}	Strobe to Buffer Full		400
t _{SS}	Strobe Width	200	
t _{RBE}	READ to Buffer Empty		400
t _{SI}	Strobe to INTR On		400
t _{ROI}	READ to INTR Off		400
t _{PSS}	Port Setup Time to Strobe Strobe	50	
t _{PHS}	Port Hold Time After Strobe	120	
t _{SBE}	Strobe to Buffer Empty		400
t _{WBF}	WRITE to Buffer Full		400
t _{WI}	WRITE to INTR Off		400
t _{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low		400
t _{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ High		400
t _{RDE}	Data Bus Enable from READ Control	10	
t ₁	TIMER-IN Low Time	80	
t ₂	TIMER-IN High Time	120	

Table 9 A.C. characteristics

a. Read Cycle



b. Write Cycle

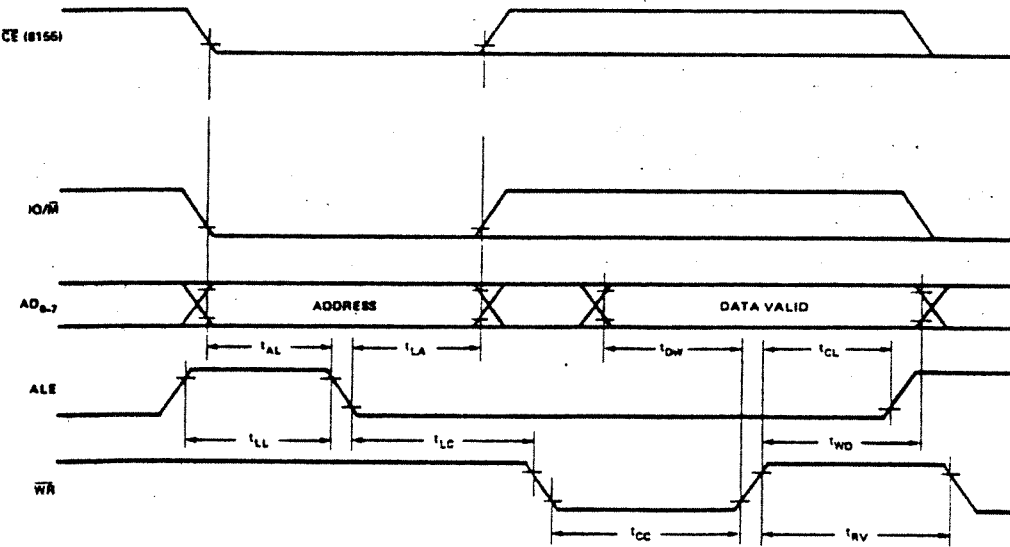
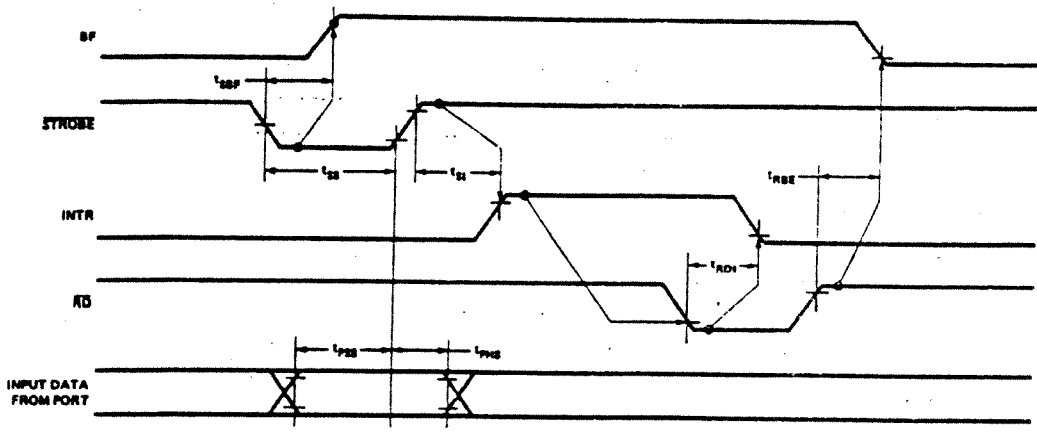


Fig. 10 81C55 Read/Write Timing Diagram

a. Strobed Input Mode



b. Strobed Output Mode

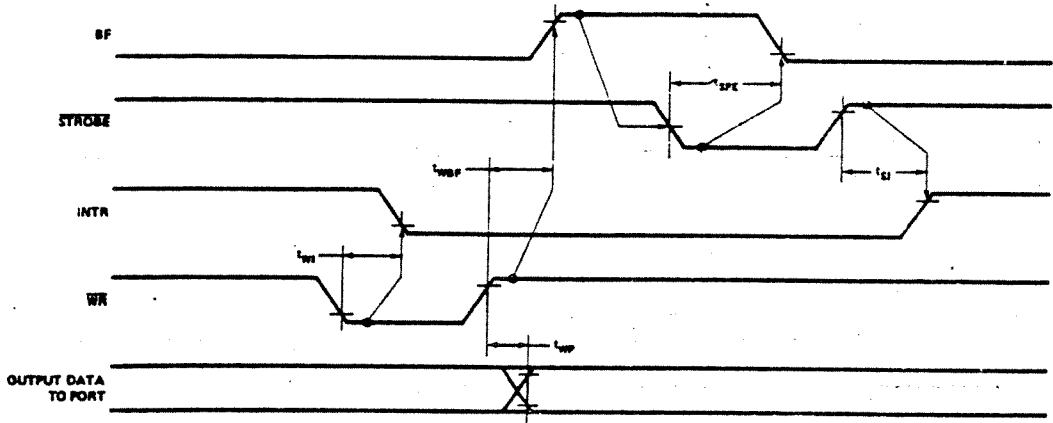
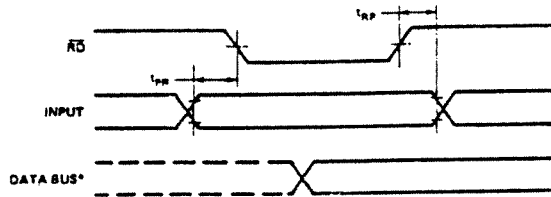
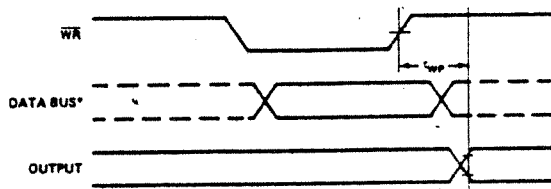


Fig. 11 Strobed I/O Timing

a. Basic Input Mode



b. Basic Output Mode



*DATA BUS TIMING IS SHOWN IN FIGURE 7.

Fig. 12 Basic I/O Timing

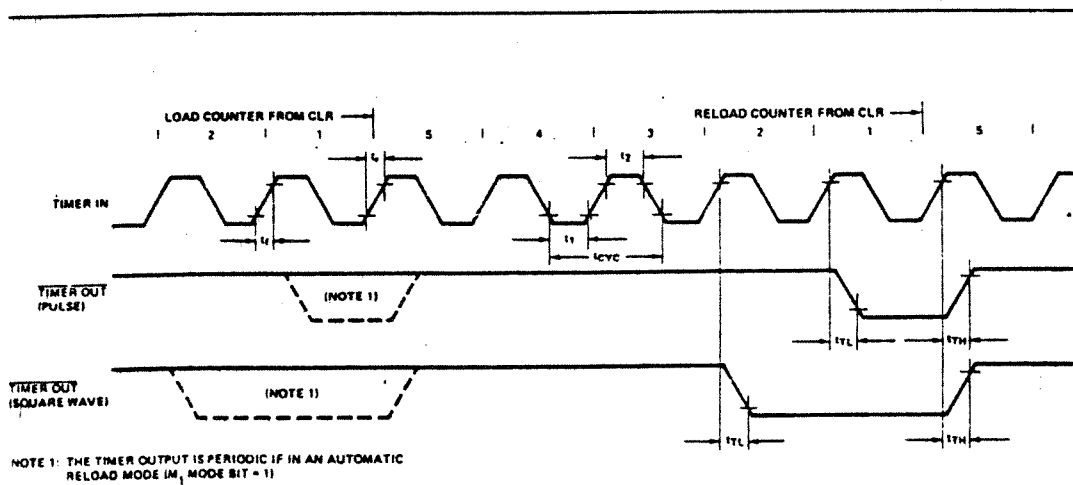


Fig 13 Timer output Waveform Countdown from 5 to 1

(3) HD6402 (UART)
 C-MOS UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

(a) Description

The HD-6402 is a CMOS/LSI subsystem for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5 bit code.

The HD-6402 can be used in a wide range of applications including modems, printers, peripherals and remote data aquisition systems. CMOS/LSI technology permits operation clock frequencies up to 2.0 MHz (125K Baud) an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 300 mW to 10 mW. Status logic increases flexibility and simplifies the user interface.

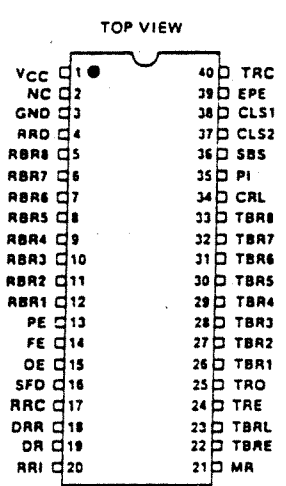


Fig.14 Pin Layout

CONTROL WORD					CHARACTER FORMAT								
C	C	L	L	P	S	S	I	P	B	START	DATA	PARITY	STOP
2	1	E	S	B	BIT	BITS	BIT	BITS	BIT	BITS	BIT	BITS	
0	0	0	0	0	1	5	ODD	1					
0	0	0	0	1	1	5	ODD	1.5					
0	0	0	1	0	1	5	EVEN	1					
0	0	0	1	1	1	5	EVEN	1.5					
0	0	1	X	0	1	5	NONE	1					
0	0	1	X	1	1	5	NONE	1.5					
0	1	0	0	0	1	6	ODD	1					
0	1	0	0	1	1	6	ODD	2					
0	1	0	1	0	1	6	EVEN	1					
0	1	0	1	1	1	6	EVEN	2					
0	1	1	X	0	1	6	NONE	1					
0	1	1	X	1	1	6	NONE	2					
1	0	0	0	0	1	7	ODD	1					
1	0	0	0	1	1	7	ODD	2					
1	0	0	1	0	1	7	EVEN	1					
1	0	0	1	1	1	7	EVEN	2					
1	0	1	X	0	1	7	NONE	1					
1	0	1	X	1	1	7	NONE	2					
1	1	0	0	0	1	8	ODD	1					
1	1	0	0	1	1	8	ODD	2					
1	1	0	1	0	1	8	EVEN	1					
1	1	0	1	1	1	8	EVEN	2					
1	1	1	X	0	1	8	NONE	1					
1	1	1	X	1	1	8	NONE	2					

Table 10 Control Word Format

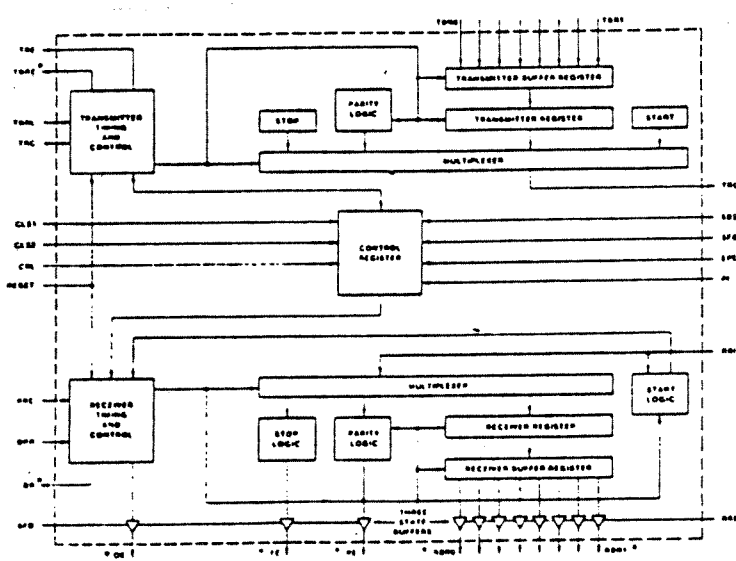


Fig. 15 Function Diagram

Supply Voltage +8.0V
 Input or Output Voltage Applied GND -0.3V to VCC +0.3V
 Storage Temperature Range -65°C to +150°C
 Operating Temperature Range (Industrial -9) -40°C to +85°C

Table 11 Absolute Maximum Rating

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
V _{IH}	Logical "1" Input Voltage	70% V _{CC}			V	0V ≤ V _{IN} ≤ V _{CC} I _{OH} = -0.2mA I _{OL} = 2.0mA 0V ≤ V _O ≤ V _{CC} V _{IN} = GND or V _{CC} V _{CC} = 5.25V Output Open
V _{IL}	Logical "0" Input Voltage			20% V _{CC}	V	
I _{IL}	Input Leakage	-10.0		+10.0	μA	
V _{OH}	Logical "1" Output Voltage	2.4			V	
V _{OL}	Logical "0" Output Voltage			0.45	V	
I _O	Output Leakage	-10.0		+10.0	μA	
I _{CC}	Supply Current		1.0	800	μA	
C _{IN}	Input Capacitance*		7.0	8.0	pF	
C _O	Output Capacitance*		8.0	10.0	pF	

Table 12 Electrical Characteristics (D.C.)

SYMBOL	PARAMETER	V _{CC} = 5.0V ① T _A = 25°C			V _{CC} = 5.0V ± 5% T _A = Industrial			UNITS	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
f _{clock}	Clock Frequency	D.C.		2.0	D.C.		1.0	MHz	C _L = 50pF See Switching Time Waveforms 1, 2, 3
t _{pw}	Pulse Widths CRL, DR, TBRL	200			225			ns	
t _{MR}	Pulse Width MR	500			600			ns	
t _{SET}	Input Data Setup Time	60			75			ns	
t _{HOLD}	Input Data Hold Time	75			90			ns	
t _{EN}	Output Enable Time			150			190	ns	

Table 13 Electrical Characteristics

(b) Receiver Operation

Data is received in serial form at the RInput. When no data is being received, RInput must remain high. The data is clock through the RRClock. The clock rate is 16 times the data rate. (A) A low level on DRReset clears the DReady line. (B) During the first stop bit data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBRI. A logic high on OError indicates overruns. An overrun occurs when DReady has not been cleared before the present character was transferred to the RBRegister. (C) 1 clock cycle later DReady is reset to a logic high, and FError is evaluated. A logic high on FError indicates an invalid stop bit was received, a framing error. A logic high on PError indicates a parity error.

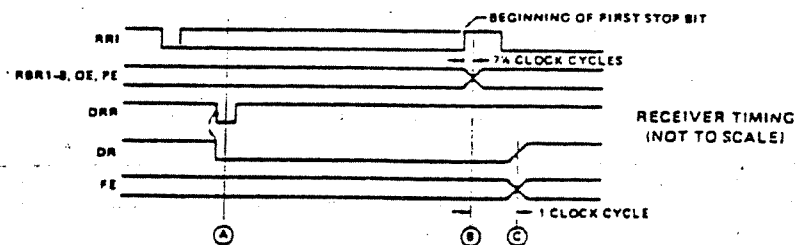


Fig. 16

(c) START Bit Detection

The receiver uses a 16X clock for timing. (A) The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7-1/2. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within $\pm 1/2$ clock cycle, $\pm 1/32$ bit or 3.125% giving a receiver margin of 46.875%. The receiver begins searching for the next start bit at the center of the first stop bit.

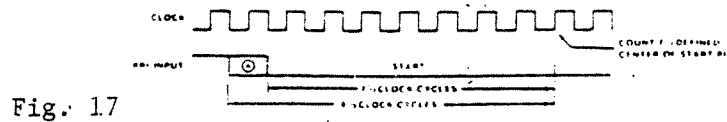


Fig. 17

(d) IM6402 Pin Functions

Symbol	Description
Vcc	Positive Voltage Supply
NC	No Connection
GND	Ground
RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding outputs RBR1–RBR8 to a high impedance state.
RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.

Symbol	Description
RBR7	See Pin 5 – RBR8
RBR6	See Pin 5 – RBR8
RBR5	See Pin 5 – RBR8
RBR4	See Pin 5 – RBR8
RBR3	See Pin 5 – RBR8
RBR2	See Pin 5 – RBR8
RBR1	See Pin 5 – RBR8
PE	A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited this output is low.
FE	A high level on FRAMING ERROR indicates the first stop bit was invalid.
OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the received buffer register.
SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
RRC	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
DRR	A low level on DATA RECEIVED RESET clears the data received output DR to a low level.
DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
MR	A high level on MASTER RESET clears PE, FE, GE, and DR to a low level and sets the transmitter output to a high level after 18 clock cycles. MR does not clear the receiver buffer register. This input must be pulsed at least once after power up.

Symbol	Description
TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
TBRL	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1–TBR8 into the transmitter buffer register. A low to high transition on TBRL indicates data transfer to the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1–TBR8. For character formats less than 8 bits the TBR8, 7 and 6 inputs are ignored corresponding to the programmed word length.
TBR2	See Pin 26 – TBR1
TBR3	See Pin 26 – TBR1
TBR4	See Pin 26 – TBR1
TBR5	See Pin 26 – TBR1
TBR6	See Pin 26 – TBR1
TBR7	See Pin 26 – TBR1
TBR8	See Pin 26 – TBR1
CRL	A high level on CONTROL REGISTER LOAD loads the control register.
PI	A high level on PARITY INHIBIT inhibits parity generation. Parity checking and forces PE output low.
SBS	A high level on STOP BIT SELECT selects 1.5 stop bits for 5 character format and 2 stop bits for other lengths.

Symbol	Description
CLS2	These inputs program the CHARACTER LENGTH SELECTED (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits).
CLS1	See Pin 37 – CLS2.
EPE	When P1 is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

BLOCK DIAGRAM

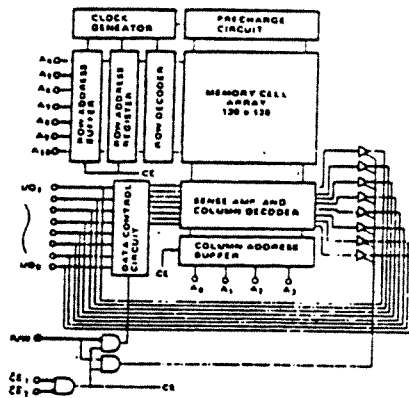


Fig. 18

Read Cycle (1)

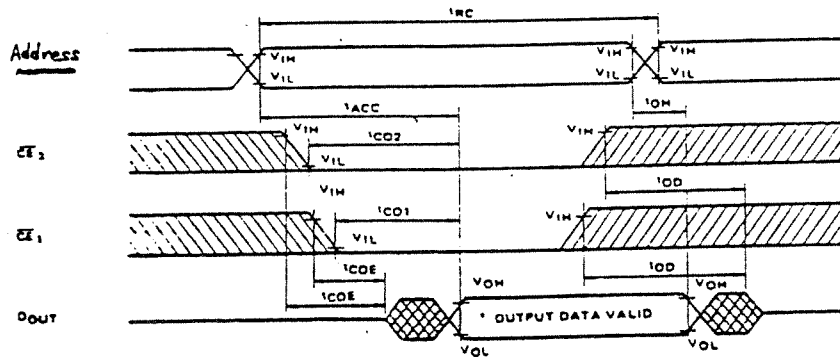
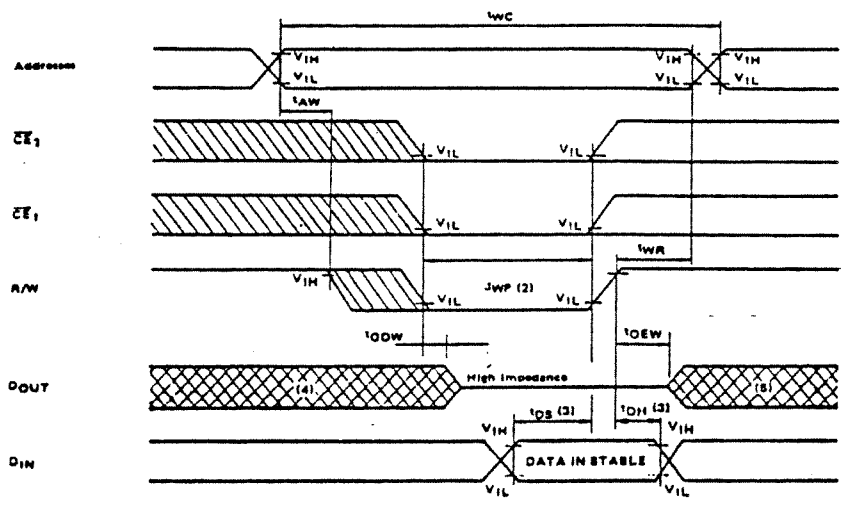
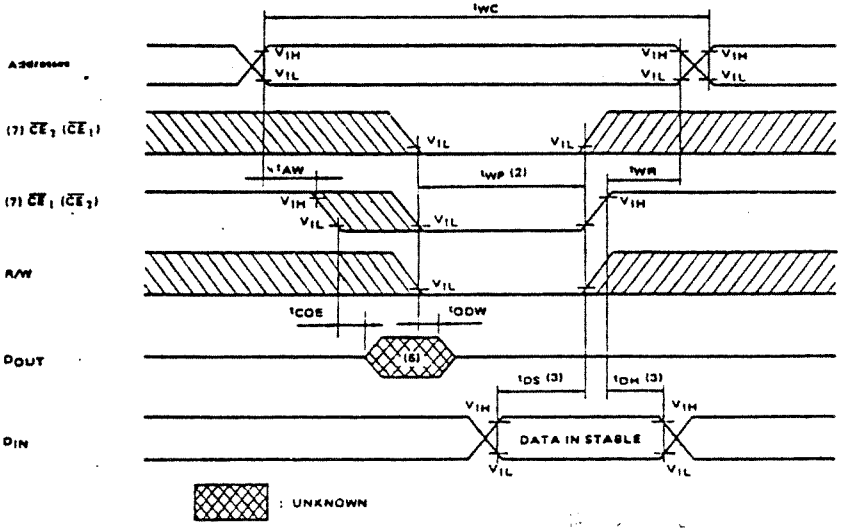


Fig. 19 Timing Waveform

Write Cycle 1.



Write Cycle 2.



- Note:
- (1) R/W is high for a Read Cycle.
 - (2) t_{WP} is specified as the logical "AND" of \overline{CE}_1 , \overline{CE}_2 and R/W. t_{WP} is measured from the latter of \overline{CE}_1 , \overline{CE}_2 or R/W going low to the earlier of \overline{CE}_1 , \overline{CE}_2 or R/W going high.
 - (3) t_{DH} , t_{DS} are measured from the earlier of \overline{CE}_1 , \overline{CE}_2 or R/W going high.
 - (4) If the \overline{CE}_1 , or \overline{CE}_2 low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
 - (5) If the \overline{CE}_1 or \overline{CE}_2 high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
 - (6) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the \overline{CE}_1 or \overline{CE}_2 low transition, the output buffers remain in a high impedance state in this period.
 - (7) A write occurs during the overlap of a low \overline{CE}_1 , low \overline{CE}_2 and low R/W. In write cycle 2, write is controlled by either \overline{CE}_1 or \overline{CE}_2 .

Fig. 20

$A_0 \sim A_{16}$	Address Inputs
R/W	Read/Write Control Input
CE_1, CE_2	Chip Enable Inputs
$I/O_1 \sim I/O_2$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

Table 14 Pin Names

MODE	CE_1	CE_2	R/W	$A_0 \sim A_{16}$	$I/O_1 \sim I/O_2$	POWER
Read	L	L	H	Stable	Data Out	I_{DD0}
Write	L	L	L	Stable	Data In	I_{DD0}
** Standby 1	*	H	*	*	High Impedance	I_{DPS}
** Standby 2	H	*	*	*	High Impedance	I_{DPS}

Table 15 Operation Mode

Note: *: H or L **: Data Retention Mode

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	-0.3V ~ 7.0V
V_{IN}	Input Voltage	-0.3V ~ $V_{DD}+0.3V$
$V_{I/O}$	Input/Output Voltage	-0.3V ~ $V_{DD}+0.3V$
P_D	Power Dissipation ($T_a = 85^\circ C$)	0.8W (0.45W)*
T_{STG}	Storage Temperature	$-55^\circ C \sim 150^\circ C$
T_{OPR}	Operating Temperature	$-30^\circ C \sim 85^\circ C$
T_{SOLDER}	Soldering Temperature - Time	$260^\circ C \cdot 10 \text{ sec}$

Plastic FP = 0.45W

Table 16 Absolute Maximum Rating

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	$V_{DD}+0.3$	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{DR}	Data Retention Voltage	2.0	-	5.5	V

Table 17 Recommended D.C. operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MIN.	UNIT	
I_{IL}	Input Leakage Current	$0 \leq V_{IN} \leq V_{DD}$	-	-	± 1.0	μA	
I_{LO}	I/O Leakage Current	$CE_2 = V_{IH}, 0V \leq V_{IO} \leq V_{DD}$	-	-	± 5.0	μA	
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-1.0	-2.0	-	mA	
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	2.0	3.0	-	mA	
I_{DPS1}	Standby Current	$CE_2 = 2.2V$ or $CE_1 = 2.2V$	-	1.0	3.0	mA	
I_{DPS2}		$CE_2 = V_{DD} - 0.5V$ or $CE_1 = V_{DD} - 0.5V$	-	-	0.2	mA	
		$V_{DD} = 2 \sim 5.5V$	TC5518BPL /BDL/BFL	$T_a = 25^\circ C$	-	-	1.0
			TC5518BP/ BD/BF	$T_a = 60^\circ C$	-	-	5.0
I_{DD01}	Operating Current	$t_{cycle} = 200ns, CE_1 = CE_2 = 0V, I_{OUT} = 0mA$	$V_{IN} = V_{IH}/V_{IL}$	-	-	30	
I_{DD02}			$V_{IN} = V_{DD}/GND$	-	-	25	
I_{DD03}			$t_{cycle} = 1\mu s, CE_1 = CE_2 = 0V, I_{OUT} = 0mA$	$V_{IN} = V_{IH}/V_{IL}$	-	-	10
I_{DD04}			$V_{IN} = V_{DD}/GND$	-	-	5	

Table 18 D.C. Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C _{IN}	Input Capacitance	—	5	10	pF
C _{IO}	Input/Output Capacitance	—	5	10	pF

Table 19 Capacitance

Read Cycle

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t _{RC}	Read Cycle Time	200	—	—	ns
t _{ACC}	Access Time	—	—	200	ns
t _{CO1}	CE ₁ to Output Valid	—	—	200	ns
t _{CO2}	CE ₂ to Output Valid	—	—	200	ns
t _{COE}	CE ₁ or CE ₂ to Output Active	10	—	—	ns
t _{OD}	Output High-Z from Deselection	—	—	60	ns
t _{OH}	Output Hold from Address Change	20	—	—	ns

Write Cycle

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t _{WC}	Write Cycle Time	200	—	—	ns
t _{WP}	Write Pulse Width	150	—	—	ns
t _{AW}	Address Set up Time	0	—	—	ns
t _{WR}	Write Recover Time	0	—	—	ns
t _{ODW}	Output High-Z from R/W	—	—	60	ns
t _{OEW}	Output Active from R/W	10	—	—	ns
t _{DS}	Data Set up Time	90	—	—	ns
t _{DH}	Data Hold Time	0	—	—	ns

Table 20 A.C. Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	
V _{DR}	Data Retention Power Supply Voltage	2.0	—	6.6	V	
I _{DOS2}	standby current	TC5518BP/BDL/BFL	T _A = 25°C	—	0.2	μA
			T _A = 60°C	—	1.0	
		TC5518BP/BD/BP	T _A = 25°C	—	1.0	
			T _A = 60°C	—	4.0	
			T _A = 85°C	—	4.1	
t _{CDR}	From Chip Deselection to Data Retention Mode	0	—	—	μs	
t _R	Recover Time	t _{RC} (1)	—	—	μs	

Note (1) t_{RC} : Read Cycle Time

Table 21 Data retention Characteristics

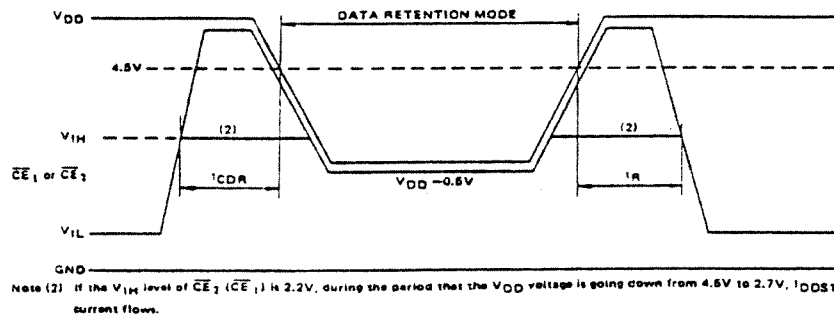


Fig. 21

2 . MEMORY

The memory of Model 100 consists of a 32-KB ROM and a 32-KB RAM (standard 8 KB with 8 KB increments each) , and a 32-KB BANK ROM (optional)

(1) RAM (Random Access Memory)

Model 100 has a RAM Pack consisting of four 2 KB RAMs (each 2048 X 8 bit) mounted on the ceramicmother board , for a total of 8 KB (8192 X 8 bit) .

the standard equipment RAM pack is the M9 ,with the M8 , M7 and M6 providing increased capacity.

The internal wiring diagram of the RAM pack is shown in Fig. 22 .

The specifications for the 2 KB S-RAM used are given below.

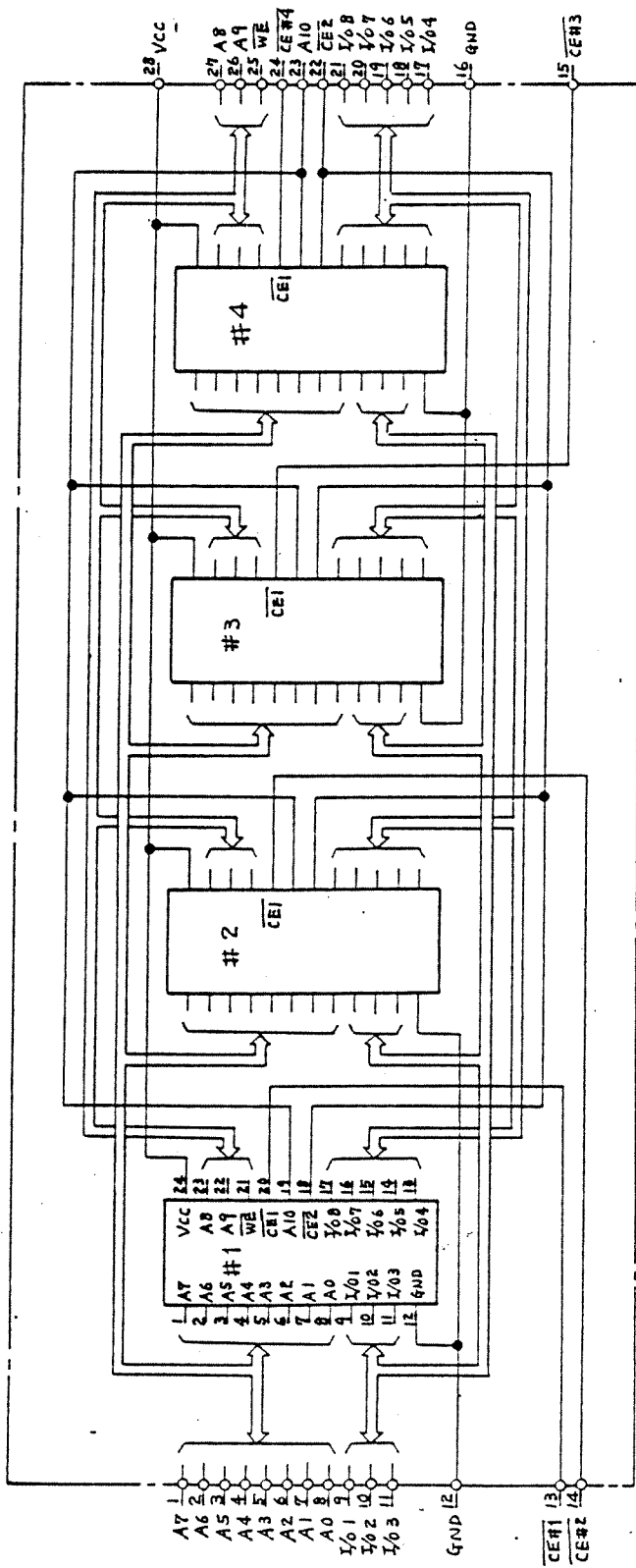


Fig 22

(2) ROM (Read Only Memory)

The ROM used in Model 100 is a synchronous 32-KB (256 K bit) memoly. Operated by a single 5V power supply, the access time is 600nsec (max).

The ALE (Address Latch Enable) is used as the synchronous signal with CPU.

The BASIC program is included in the standard ROM.

Also, the BIOS program is included in the standard ROM for operation of the LCD, printer, etc.

An optional ROM can be connected to the special IC socket by removing the ROM cover on the case under the Model 100.

Various type of application program can be entered in the optional ROM.

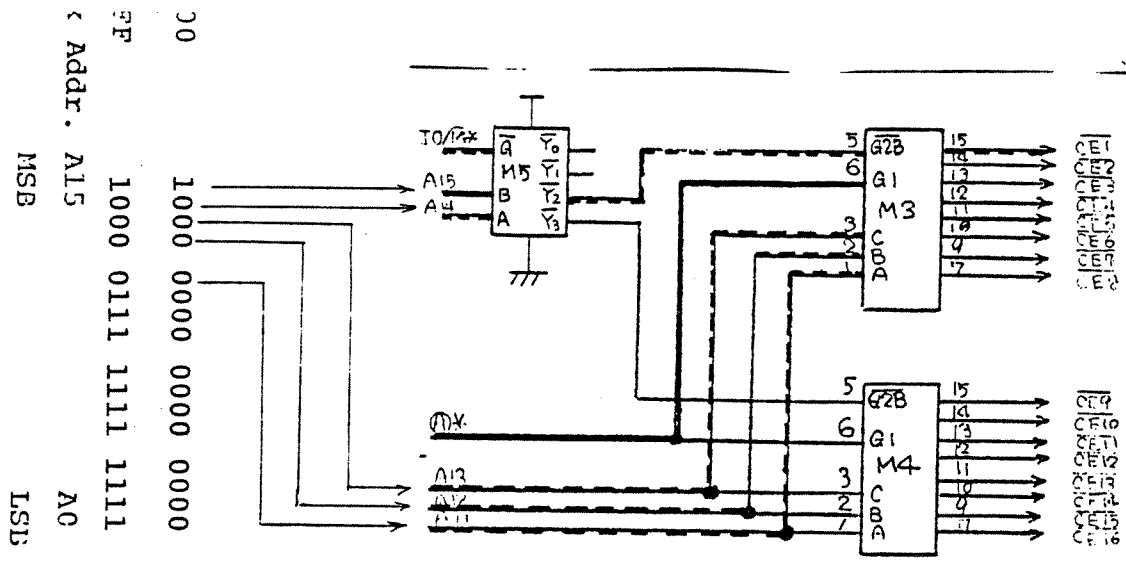
3. ADDRESS DECOING AND BANK SELECTION

(1) Address decoding for RAM chip selection

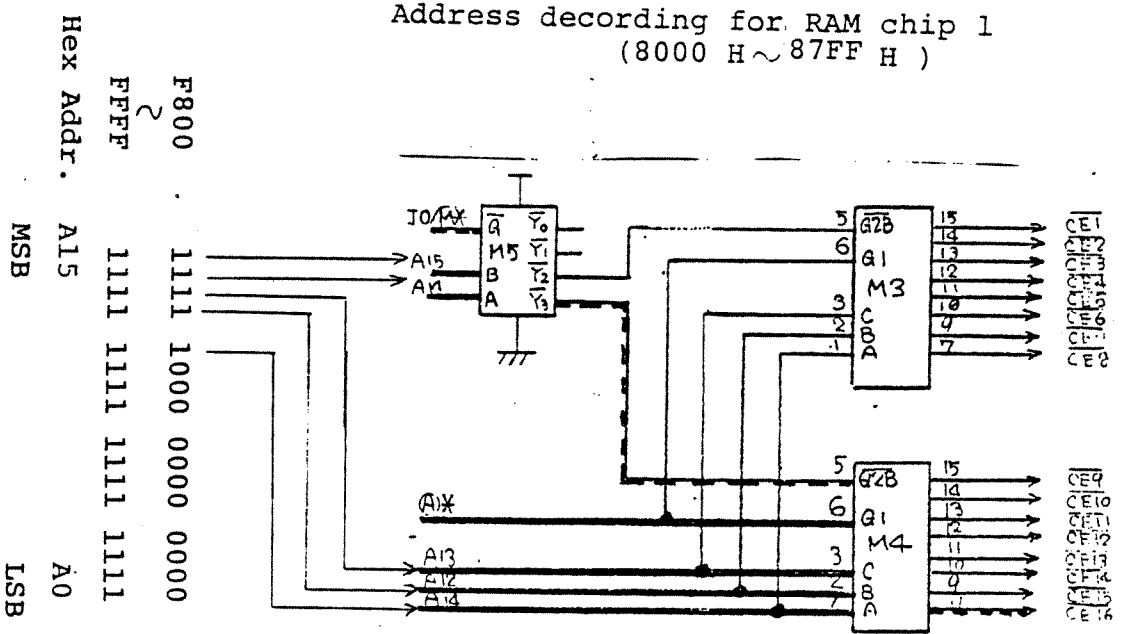
Although four 8-KB RAM packs are attached to Model 100, 16 chip select signals are necessary because 16X2 KB RAMs are actually used.

Moreover ,because the RAM area is positioned from 8000H to FFFFH (see memory map), the control signal is formed by $\overline{IO/M}$,A15 and A14 , as shown in Fig.23, and the 16 chip-select signals are formed by A13 ,A12 and A11.

M5 (TC40H139:dual 2 to 4 line decoder /demultiplexer) is used to make the control signal, and M3 and M4 (TC40H133: 3 to 8 line decoder /demultiplexer) are used to make the 16 chip select signals.



Address decoding for RAM chip 1
(8000 H ~ 87FF H)



Address decoding for RAM chip 16
(F800 H ~ FFFF H)

— Active line with high-level
- - - Active line with low-level

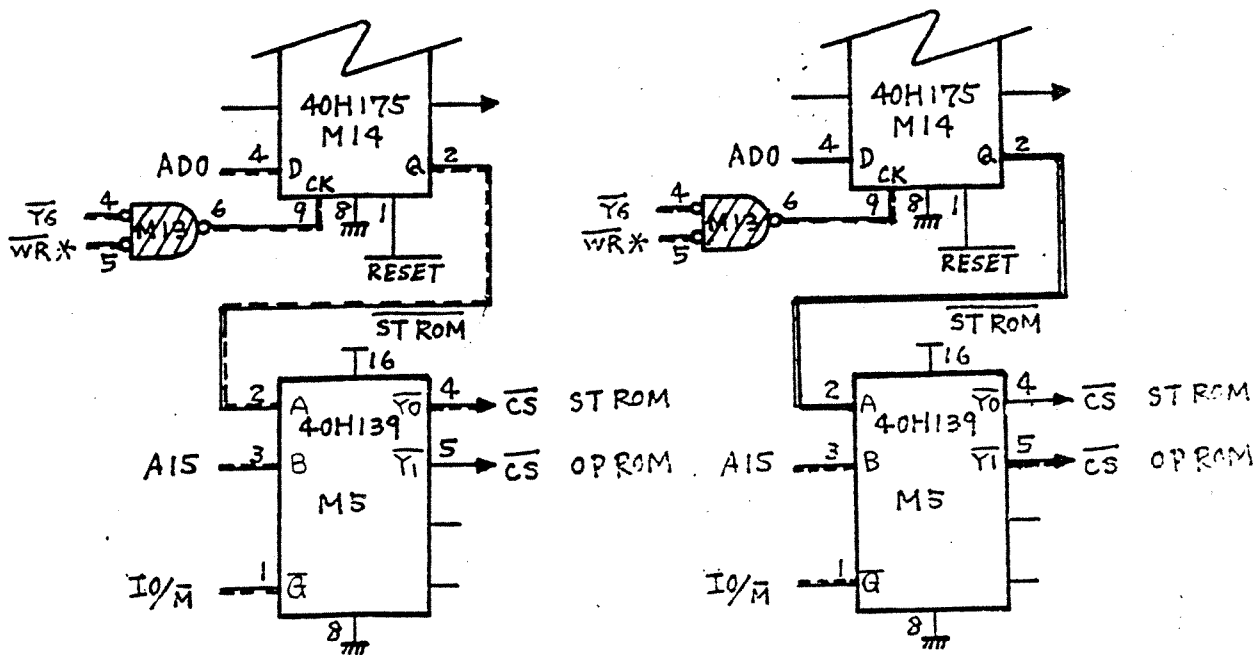
Fig .23

(2) ROM chip selection and BANK selection

The ROMs (both standard and optional)used in Model 100 are the 32-KB 1-chip type. And , as can be seen on the memory map ,the address space is positioned from 0000H to FFFFH. Consequently ,the A15 signal and bank selection signal (\overline{STROM}) are formed by the chip-select signals.

As shown in Fig.24,AD0 is latched by M14 (TC40H175: quad "D" type F/F),by using the \overline{WR} signal and $\overline{Y6}$ signal (see I/O port description),forming the \overline{STROM} signal, and the chip-select signal of each ROM is formed from the $\overline{IO/\overline{M}}$ signal by M5 (TC40H139).

The standard ROM is selected by the L \overline{STROM} signal, and the optional ROM by the H \overline{STROM} signal.



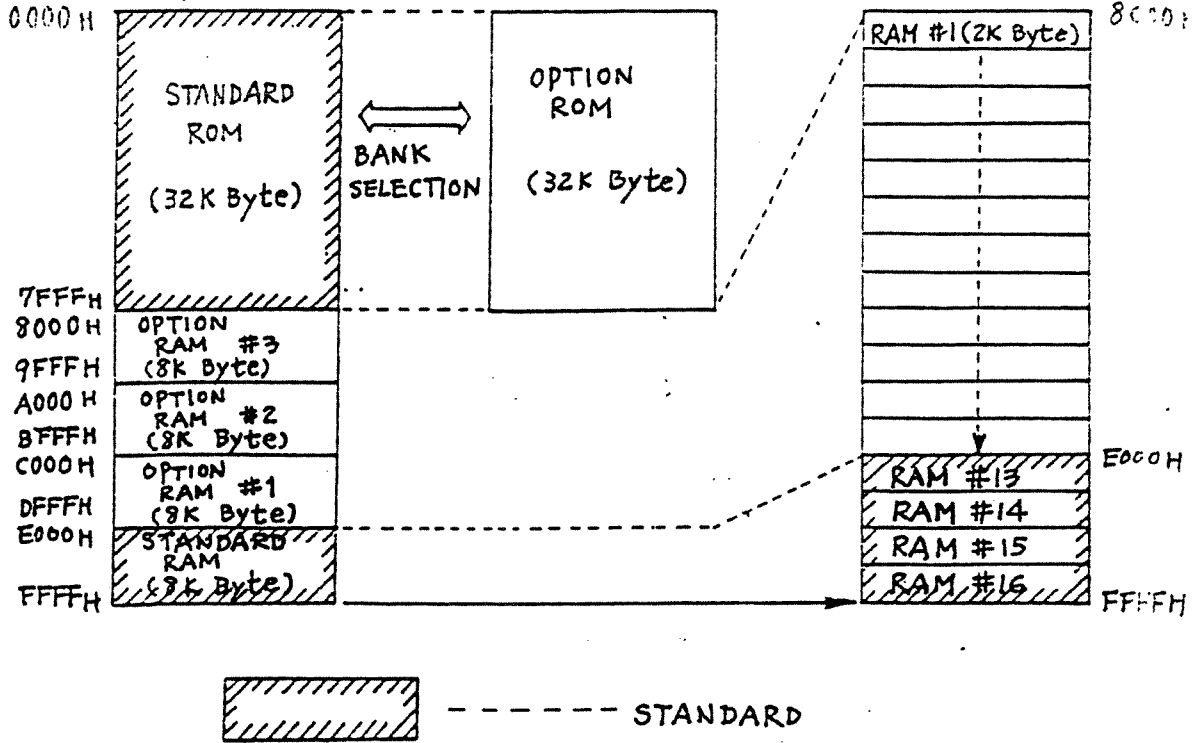
Standard ROM chip selection

Optional ROM chip selection

- Active line with high-level
- - - Active line with low-level

Fig.24 Standard and Optional ROM selection

4 Memory Map



Additional of optional RAMs are from the upper address

Fig . 25

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5. I/O Map and I/O Port Description

As shown in Fig. 26, the I/O address decode circuit decodes address signals A12 to A15 and the IO/M signal by the 3 + 8 decoder IC (40H138). Because the LCD driver select signal Y7 is active "H", the output of 40H138 is inverted by 40H000. The uses of the select signals ($\bar{Y}0$ to $\bar{Y}6$ and Y7) of the I/O device and the I/O addresses are shown in Table 22

Address	Signal	Active level	Application
7FH	---	---	Free area for RAM file (optional) and other select signals of circuits made by user
8FH	$\bar{Y}0$	L	Device-select signal for optional I/O controller unit
9FH	$\bar{Y}1$	L	Device-select signal for optional answering telephone unit
AFH	$\bar{Y}2$	L	Bit 0: for ON/OFF of relay for signal selection of telephone unit Bit 1: used for generation of ENABLE signal of LSI (MC14412) for MODEM
BFH	$\bar{Y}3$	L	PIO (81C55) chip-select signal
CFH	$\bar{Y}4$	L	ENABLE signal for data input/output port of UART (IM6402)
DFH	$\bar{Y}5$	L	ENABLE signal for each status set and read port of UART
EFH	$\bar{Y}6$	L	ENABLE signal for \bar{STROM} , and \bar{REMOTE} ; and input data from Keyboard . Also, strobe signal for printer and clock.
FFH	Y7	H	ENABLE signal for LCD driver LSI (HD14403)

TABLE 22

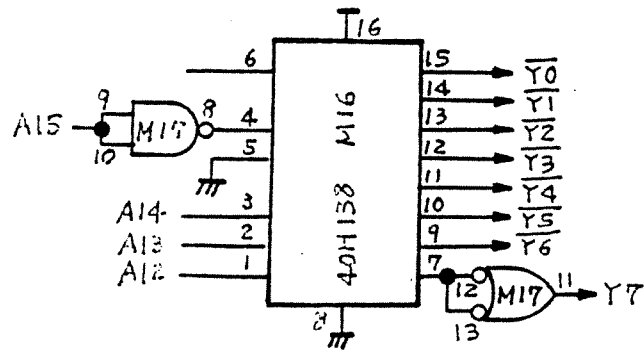


Fig. 26

The I/O address of each port of PIO (81C55) in Table 22 is shown in Table 23 below.

Address	Port or resistor
B0H or B8H	Command/status (internal)
B1H or B9H	Port A
B2H or BAH	Port B
B3H or BBH	Port C
B4H or BCH	Timer lower byte
B5H or BDH	Timer upper byte
B6H, B7H, B8H and B9H	Not used

Table 23

6. Keyboard

Key strobe signals are emitted from PB0 and PA0 - PA7 of 81C55, and the return signals from the keyboard pass through the octal bus buffer IC (40H244) to the CPU. The data input port I/O address at this time is E0H - EFH.

Condition of pressing T key is shown in Fig .27

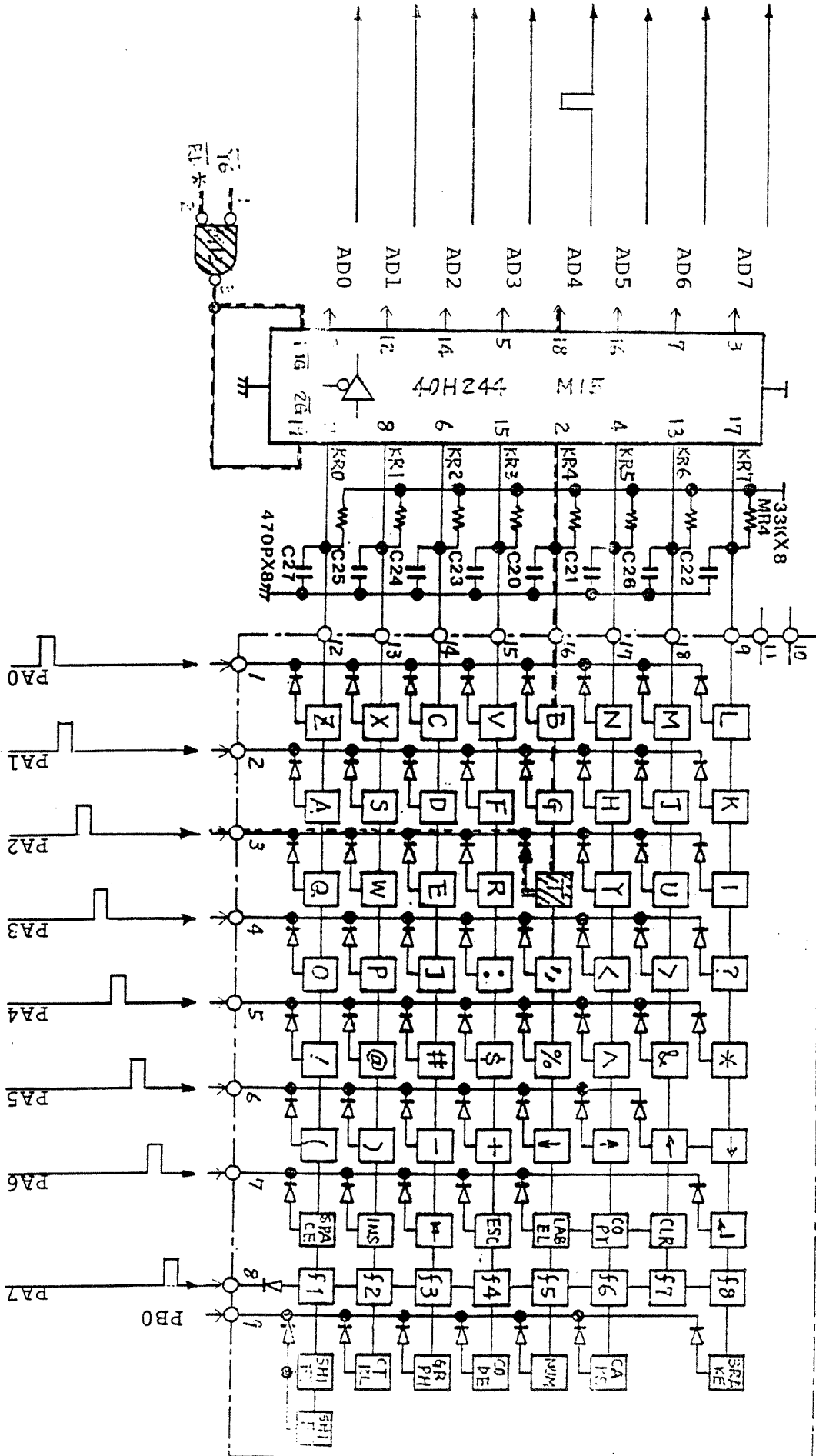


Fig. 27 Condition of pressing T key

7. Casstte Interface

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The cassette interface circuitry is divided into sections:the modulation section for modulation of the data into the recording signal , the demodulation section for return of the play back signal to data , and remote section for control of the cassette tape recorder.

(1) Modulation

After the serial data emitted from the SOD terminal of the CPU (80C85) is inverted by the inverter (M34), the DC component is cut by C63, the data passes through the integrator composed of R51 and C64, and, after voltage division to the cassette AUX input level by R54 and R55, it is input at the AUX terminal.(see Fig.28)

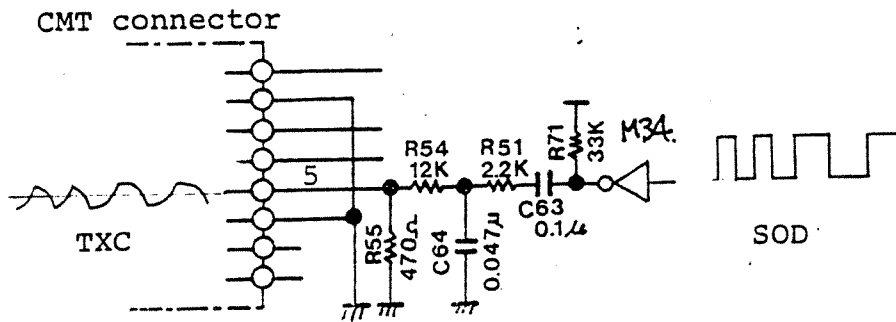
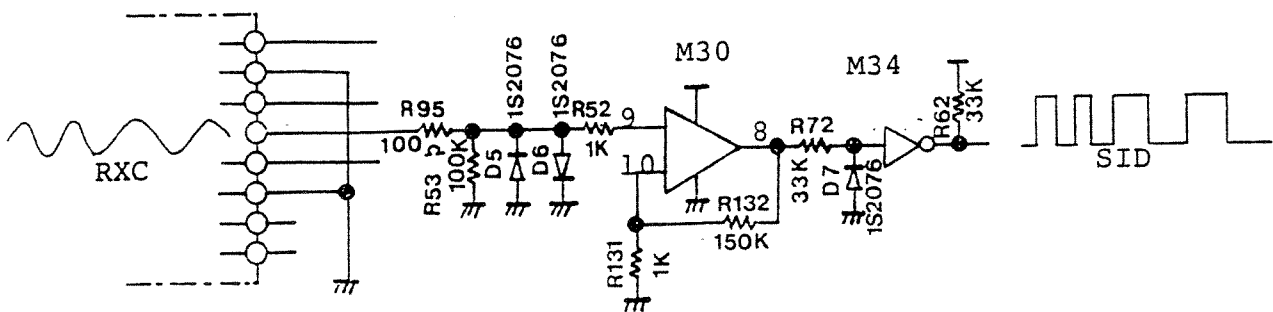


Fig.28

(2) Demodulation

The signal input from the cassette recorder's earphone jack passes through the D5 and D6 clamp circuit , is emitted from the comparator circuit composed of the operation-amplifier IC (TL64:M30), and then, after being subject to waveform shaping and inversion by the Schmitt trigger type inverter(M34), is input to the SID terminal of the CPU . Here D7 serves to clamp the negative voltage output of the comparator.(see Fig.29)



(3) Remote

The REMOTE signal output is changed to "L" level as a result of the write-in of data "1" to bit 3 of the output port (40H175: M14) specified by I/O addresses E0H - EFH, and, as a result of T6 switching ON, the relay (RY1) energized, and the cassette tape recorder operates. (See Fig.30)

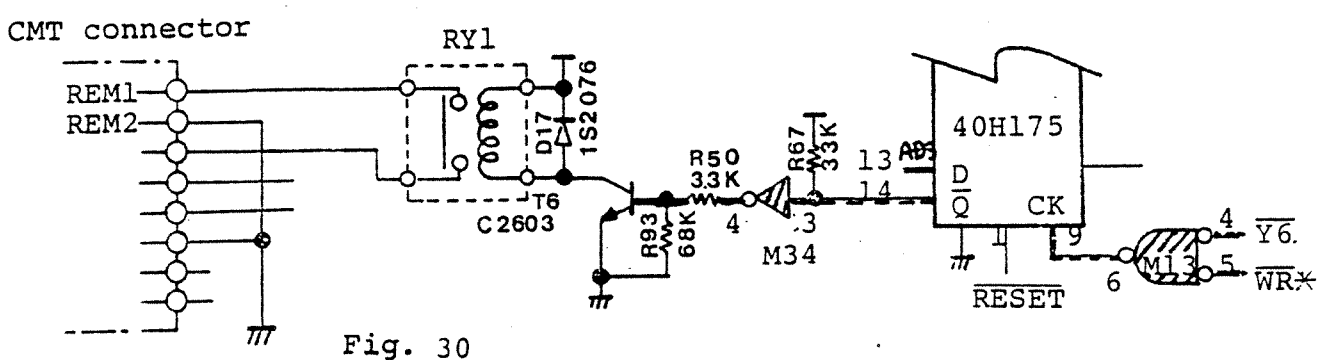


Fig. 30

8. Printer Interface

The printer interface circuit conforms to Centronics Standards.

As shown in Fig. 31, the BUSY signal from the printer is read from PC2 of 81C55. If the condition is NOT BUSY (PC2: "L" level), the 8-bit data is sent to PA0 - PA7 of 81C55, and then, as a result of data "1" write-in to bit 1 of the output port (40H175: M14) indicated by I/O address E0H - EFH, T8 is switched ON and an "L" level STROBE signal is sent to the printer.

When the printer receives this STROBE signal, the BUSY signal changes to "H" level, indicating that the printer is busy. The CPU then waits until this BUSY signal becomes "L" level.

When the BUSY signal becomes "L" level, the CPU ceases output of the PA0 - PA7 data of 81C55, and the output of 1 byte of print data is completed.

If the printer is in the ON-LINE condition, the BUSY signal is "H" level, and is "L" level if the printer is in the OFF-LINE condition, so that transmission of print data to the printer is prohibited.

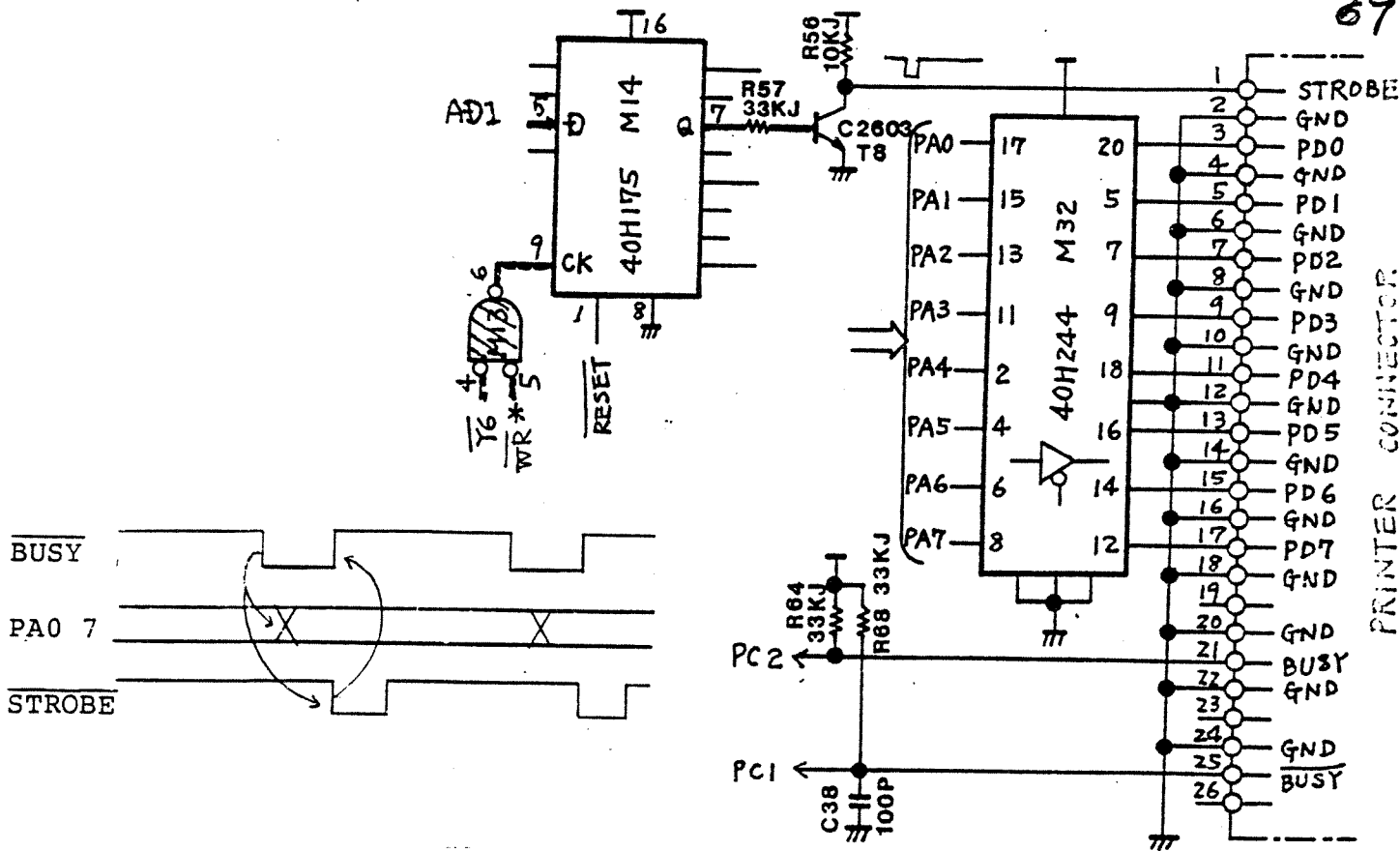
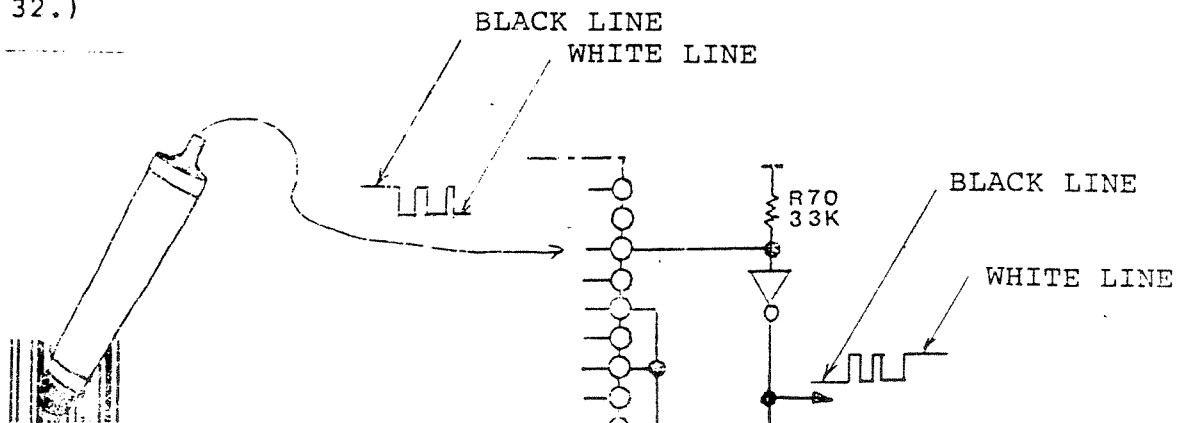


Fig.31

9. Bar Code Reader Interface

The input signal from the bar code reader is subjected to waveform shaping and inversion by the Schmitt type inverter (M34), and is input to the 81C55 PC3 and 80C85 RST 5.5 terminals. When the bar code reader reads the first white part of the bar code, an "L" signal from the bar code is input, and is then inverted by M34, after which RST 5.5 interruption occurs to indicate the start of data input. Then, when the bar code reader is moved on the bar code, the "H" signal (which corresponds to white bar codes) and the "L" signal (which corresponds to black) are input, and the inversion signal is input to PC3 of 81C55 as serial data. (See Fig. 32.)

Fig. 32



10. Buzzer Control Circuit

There are two ways in which the buzzer can be sounded by the buzzer control circuit. One is by emitting a signal from PB5 of 81C55 at a frequency which sounds the buzzer, and the other is by using the timer output of 81C55.

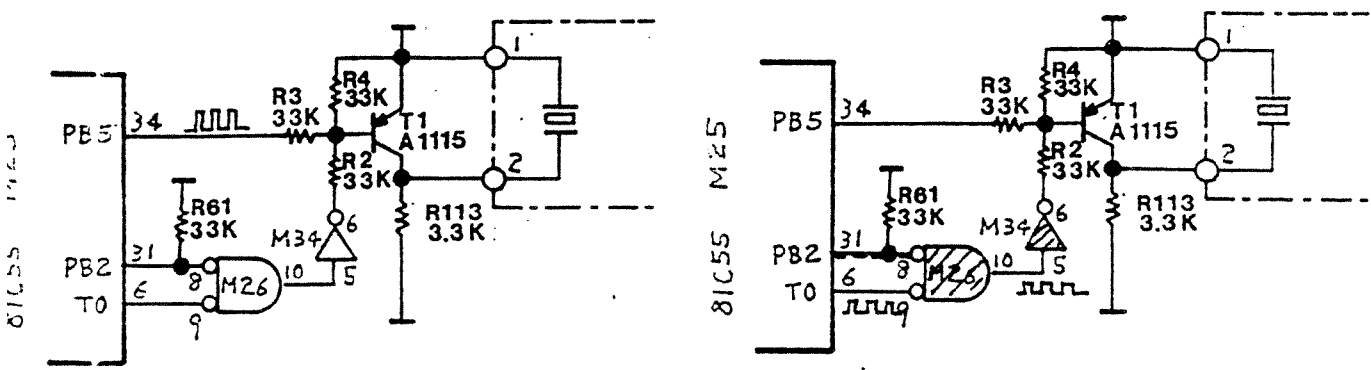
(1) Signal from PB5 of 81C55

With PB2 of 81C55 at "H" level in the circuit diagram (Fig. 33), the buzzer is sounded by the repeated OFF and ON switchings (of the transistor for buzzer drive) caused by the output from PB5 of "H", "L", "H", "L" . . signals synchronized with the frequency for sounding the buzzer.

(2) Using 81C55 timer output

With PB5 at "H" level in the circuit diagram (Fig. 33), the buzzer is sounded when, with the 81C55 timer in the square-wave output mode and set to the value corresponding to the frequency which will sound the buzzer, PB2 is switched to "L", causing the square-wave pulse emitted from the Timer Out (To) terminal of 81C55 to be applied to the base of the transistor for buzzer drive.

PB2 uses this as the buzzer ON/OFF control signal.



(1) Signal from PB5 of 81C55

(2) Using 81C55 timer output

Fig. 33

11. System Bus

In order to expand the use of external devices, the 40-pin system bus is made up of a 40-pin DIP type IC socket. As shown in Table 24, the 80C85 address bus, data bus and control bus can all be connected from the system bus to the external system, thus making system expansion easy. In addition, the optional I/O control unit and RAM file unit can be connected to this system bus.

Pin No.	Signal	Input or output	Pin No.	Signal	Input or output
1	VDD	---	40	VDD	---
2	GND	---	39	GND	---
3	AD0	In/output	38	AD1	In/output
4	AD2	In/output	37	AD3	In/output
5	AD4	In/output	36	AD5	In/output
6	AD6	In/output	35	AD7	In/output
7	A8	Output	34	A9	Output
8	A10	Output	33	A11	Output
9	A12	Output	32	A13	Output
10	A14	Output	31	A15	Output
11	GND	---	30	GND	---
12	\overline{RD}^*	Output	29	\overline{WR}^*	Output
13	$\overline{IO/M}^*$	Output	28	S0	Output
14	ALE*	Output	27	S1	Output
15	CLK	Output	26	Y0	Output
16	A^*	Output	25	RESET*	Output
17	INTR	Input	24	INTA	Output
18	GND	---	23	GND	---
19	RAM RST	Output	22	NC	---
20	NC	---	21	NC	---

Table 24 (Note: NC = no connection)

The following is an explanation of each signal in Table 24 except the CPU signal.

- . Ⓐ * signal (pin 16) . . . NAND output signal of the \overline{RD} signal and \overline{WR} signal; used by optional RAM file
- . RAM RST signal (pin 19) . . Enable signal (external C-MOS RAM); used by optional RAM file
- . Y0 signal (pin 26) . . . Device select signal of optional I/O controller unit

Table 25, below, shows the DC characteristic of each system bus signal.

	S0, S1, Y0, CLK	Signals other than at left
-level output voltage (VOH)	2.4 V min (IOH=-400 μ A)	4.95 V min (IOH=-1 μ A)
level output voltage (VOL)	0.45 V max (IOL=2mA)	0.05 V max (IOL=1 μ A)
-level output current (IOH)	-400 μ A min (VOH=2.4 V)	-0.8 mA min (VOH=4.5 V)
level output current (IOL)	2 mA min (VOL=0.45 V)	4.0 mA min (VOL=0.5 V)
-level input voltage (VIH)	---	4.0 V min
level input voltage (VIL)	---	1.0 V max

Table 25

Note: Values shown in Table 25 are at normal temperature (Ta = 25°C) and power (VDD = 5.0 V)

12. LCD Interface

The LCD interface circuit is the interface circuit between the LCD driver and the CPU. (See Fig. 34.)

The following signals are necessary for the interface with the LCD driver.

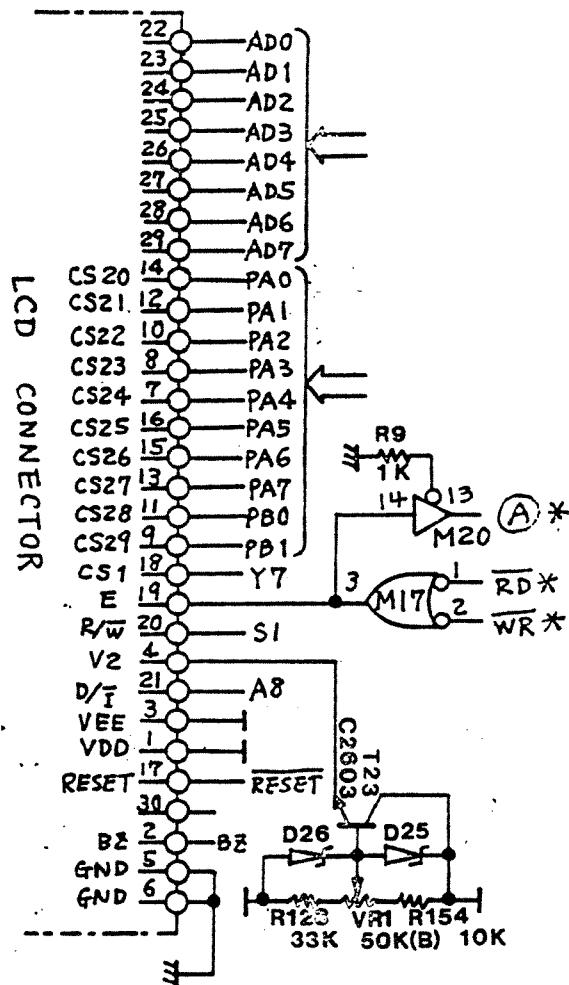


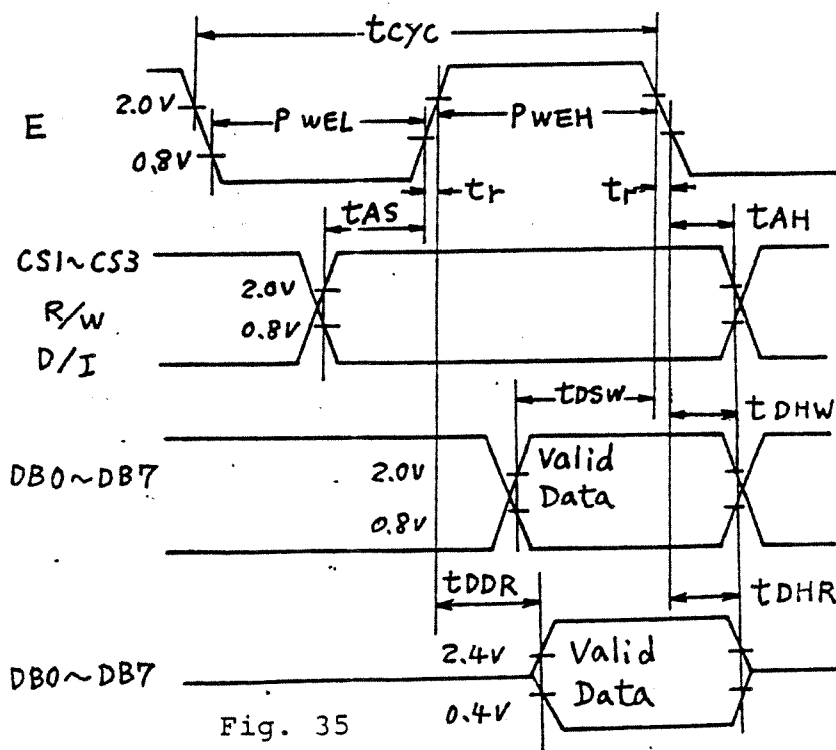
Fig. 34

- . AD0 - AD7 . . . For write-in of control data or display data to the LCD driver; signal line for read-out from driver
- . Y7 . . . LCD driver enable signal
- . PA0 - PA7, PB0, PB1 . . . Chip enable signal for each LCD driver
- . S1 . . . Indicates whether data is being written into (S1 = "L") the LCD driver or read out (S1 = "H")

- . A8 . . . Register-select signal in the LCD driver;
AD0-AD7 data are display data when A="H"
and are command or status data when
A8="L".
- . E . . . NAND output signal of \overline{RD} signal and \overline{WR} signal;
indicates the timing of the LCD driver data
read/write .
- . V2 . . . Voltage to keep the LCD driver voltage standard;
LCD display can be changed by changing the V2
voltage by VR2 .

Figure 35 shows the operating timing of each signal.

Refer to the LCD PWB Technical Description for detailed characteristics and operation of the LCD and LCD driver.



13. Clock Circuit

A clock LSI (μ PD1990AC) is used in the clock circuit so that the time can be set and read by BASIC command.

(1) Specification of μ PD1990AC

The μ PD1990AC is a C-MOS integrated circuit with a clock function which has been designed for connection to a microcomputer.

This IC independently measures the month, date, day of the week, hour, minute and second, and will output and input these time data freely upon command from the microcomputer. By employing this IC, the microcomputer is freed from performing clock functions and can be devoted exclusively to other complex operations.

The μ PD1990C employs the oscillation of a 32.768-kHz crystal as a reference. All functions are enclosed in a 14-pin dual in-line package.

(a) Features

- . Marks time (hours, minutes & seconds) and calendar (months, date and day of the week).
- . Serial inputting and outputting of data (Input & output code: All digits are binary coded decimals, except the month, which is a hexa-decimal code)
- . The reference frequency is 32.768 kHz, which is generated by a crystal oscillator circuit.
- . Provided with timing pulse outputs. (Selection of 64 Hz, 256 Hz or 2048 Hz is possible.)
- . By using the CS (chip selection) terminal, multi-chip applications are possible.

(b) Function specifications

- . Reference frequency (X'tal osc.)
32.768 kHz
- . Data
Hours, minutes, seconds, months, date and days of the week ("hours" by 24 hour system) (automatic adjustment of long and short months)

- . Data input-output and clock
Serial input, serial output
Data input and output in synchronization with the clock input from CLK
- . Time pulse output
Either 64 Hz, 256 Hz or 2048 Hz can be selected by command.
- . Mode selection
Selected according to input to C0 - C2.
C2=0 Register control (control of data input-output)
C2-1 TP control (control of time pulses) & test control (control of test mode).
Commands are latched by the STB (strobe) input
- . Chip select
CLK and STB inputs prohibited by CS input
- . Prohibition of data output
DATA OUT terminal will become high impedance when the OUT ENABL is input. Has no relation with other actions.

(c) Terminals

- . Input terminals

DATA IN	Data input of 40-bit shift register
CLK	Shift clock input of 40-bit shift register
CO - C2	Command input (3 bit)
STB	Strobe input
CS	Chip select input (Prohibits CLS & STB)
OUT ENBL	Output control input (Makes the DATA OUT high impedance by inputting low level)
- . Output terminals

DATA OUT	Data output of 40-bit shift register
TP	Time pulse output
- . Oscillation terminals

XTAL 1	Oscillation inverter input (OSC IN)
XTAL 2	Oscillation inverter output (OSC OUT)
- . Power supply terminals

VDD	Plus power supply
GND (Vss)	Common line

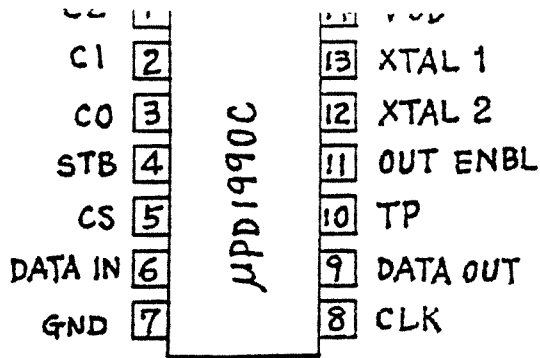
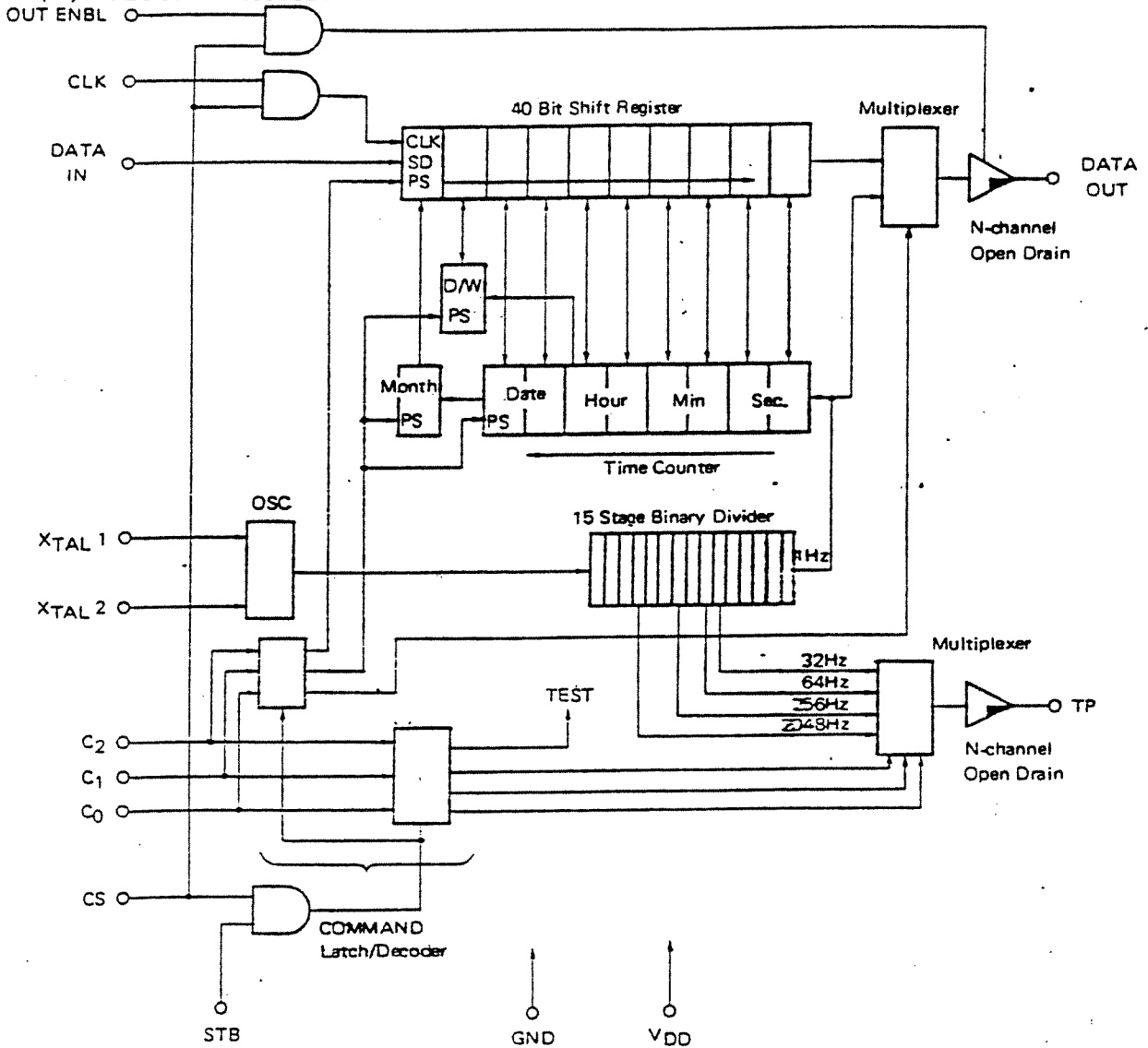


Fig. 36

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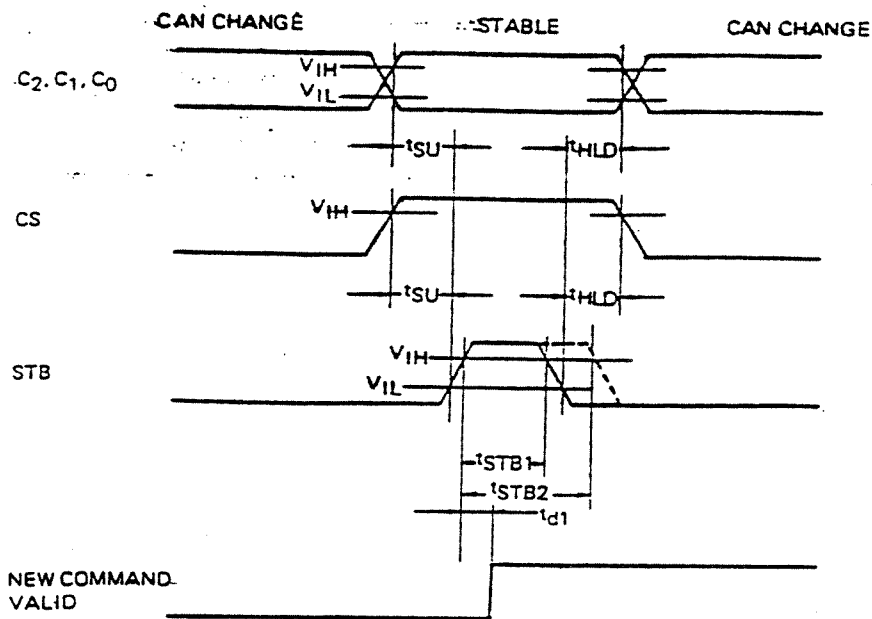
(d) BLOCK DIAGRAM



$f_{osc} = 32.768 \text{ kHz}$
 $V_{DD} = 2.0 \text{ to } 3.6 \text{ V}$

Fig. 37

(e) Command input timing diagram



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t_{STB1} : 5 μ s MIN. (t_{STB2} = 40 μ s MIN. When Time Read MODE)
 t_{SU} : 2 μ s MIN.
 t_{HLD} : 2 μ s MIN.
 t_d : 4 μ s MAX.

FOR REFERENCE

Fig.38

Commands designated by C_0, C_1 and C_2 will be written into the latch when the STB terminal becomes high level, and will be held until a different command of the same group is written-in.

(f) Data input/output timing diagram

Register Mode (C_2, C_1, C_0) set to [001]. (Shift Mode)
 $CS = \text{"H"}$

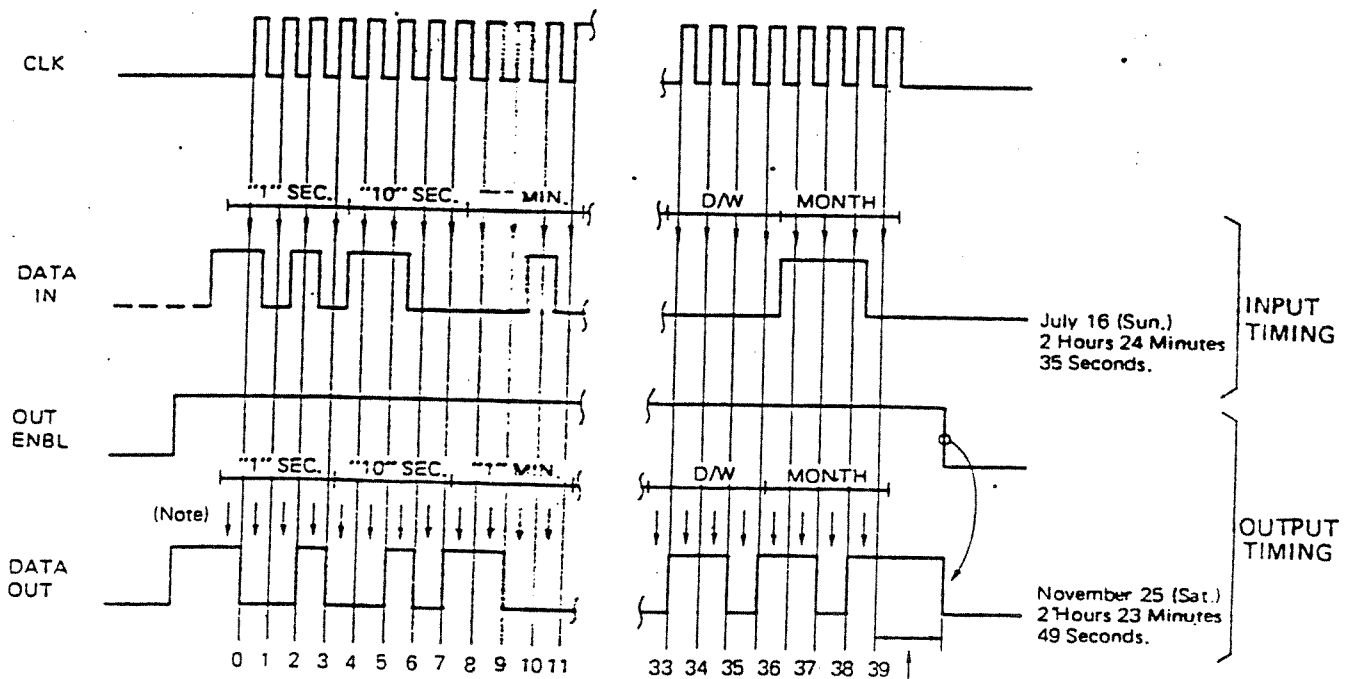


Fig.39

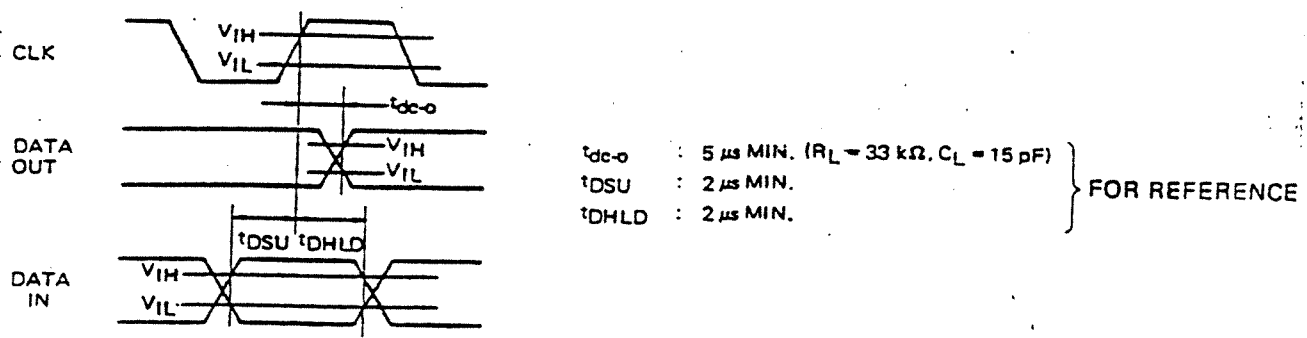


Fig. 40

(2) Clock Control Circuit

As shown in Fig. 41, when Model 100 is in the operable condition ($\overline{\text{RESET}}$ is "H" level), commands and data can be input to uPD1990AC (M18) from , and output to , the CPU at will.

In addition , because battery voltage V_B is applied to the uPD1990AC power supply, the clock functions even when the Model 100 power switch is OFF.

The clock LSI C0-C2 terminals and DATA IN and CLK terminals are connected to the 81C55 PA0-PA4 terminals , and the DATA OUT terminal is connected to the 81C55 PC0 terminal. The STB signal is provided from bit 2 of the output port made by M14 (40H175). The TP output signal is connected to the RST7.5 interruption input terminal of the CPU. Square waves are output from the TP (4 ms cycle), and one key scan occurs every 4 ms because of the RST7.5 interruption to the CPU.

(a) Time Set Sequence

The CPU sets uPD1990AC to the data input mode with "100" pattern of C0-C2 and strobe signal which is generated by AD2, $\overline{Y6}$ and \overline{WR} signals passing through M14. Then, the CPU sends the data of time and date information to the DATA IN terminal of uPD1990AC with timing clock (PA3).

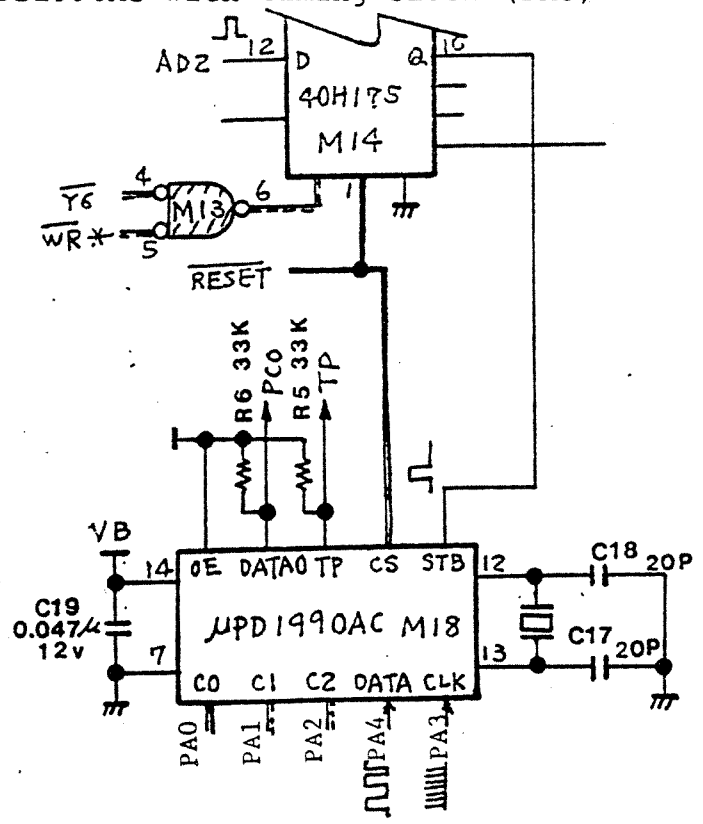


Fig. 41-1 Data Input

At last, The CPU sets to the timer set mode with "010" pattern of C0-C2, and strobe signal.

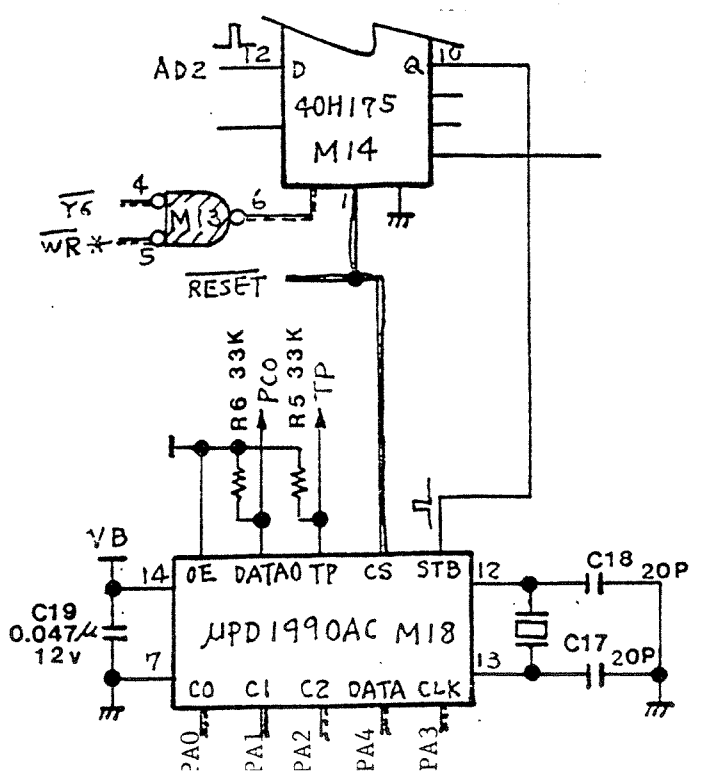


Fig.41-2 Counter set

(b) Time Read Sequence

The CPU sets uPD1990AC to the counter mode with "110" pattern of C0-C2, and strobe signal.

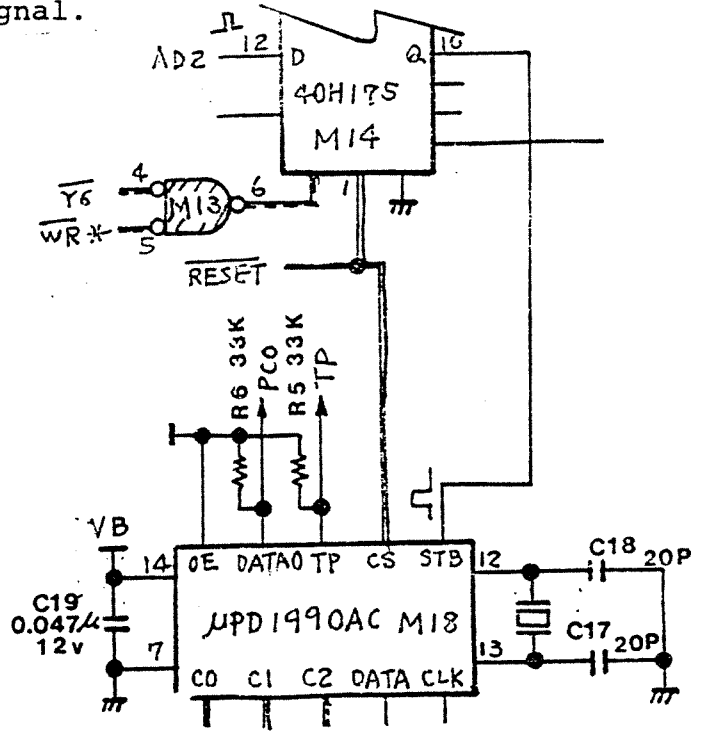


Fig.41-3 Counter Read

Then the CPU sets to the data output mode with "100" pattern of C0-C2, and reads the data of time and date information from the DATA OUT terminal. At the same time, the CPU sends the PA3 signal passing through 81C55 for the timing clock.

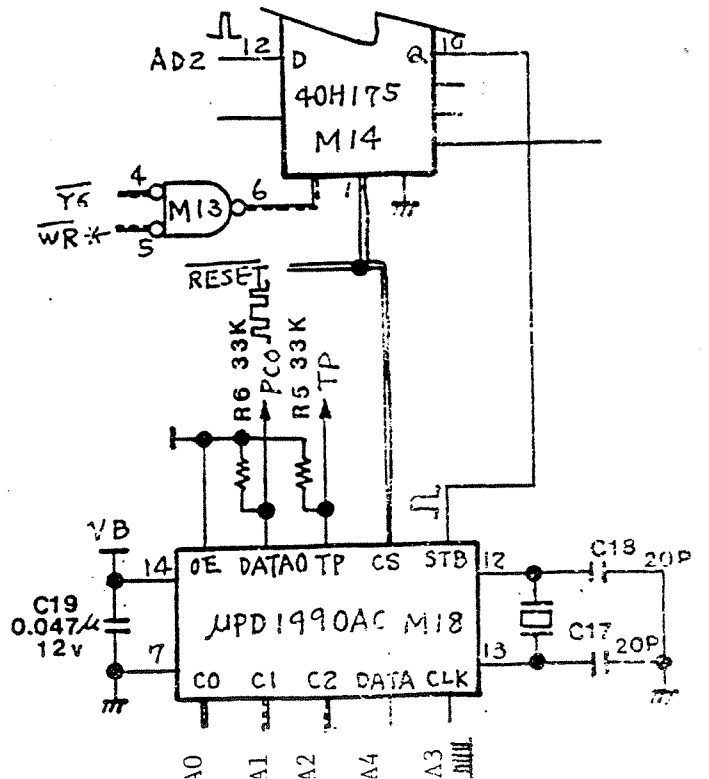
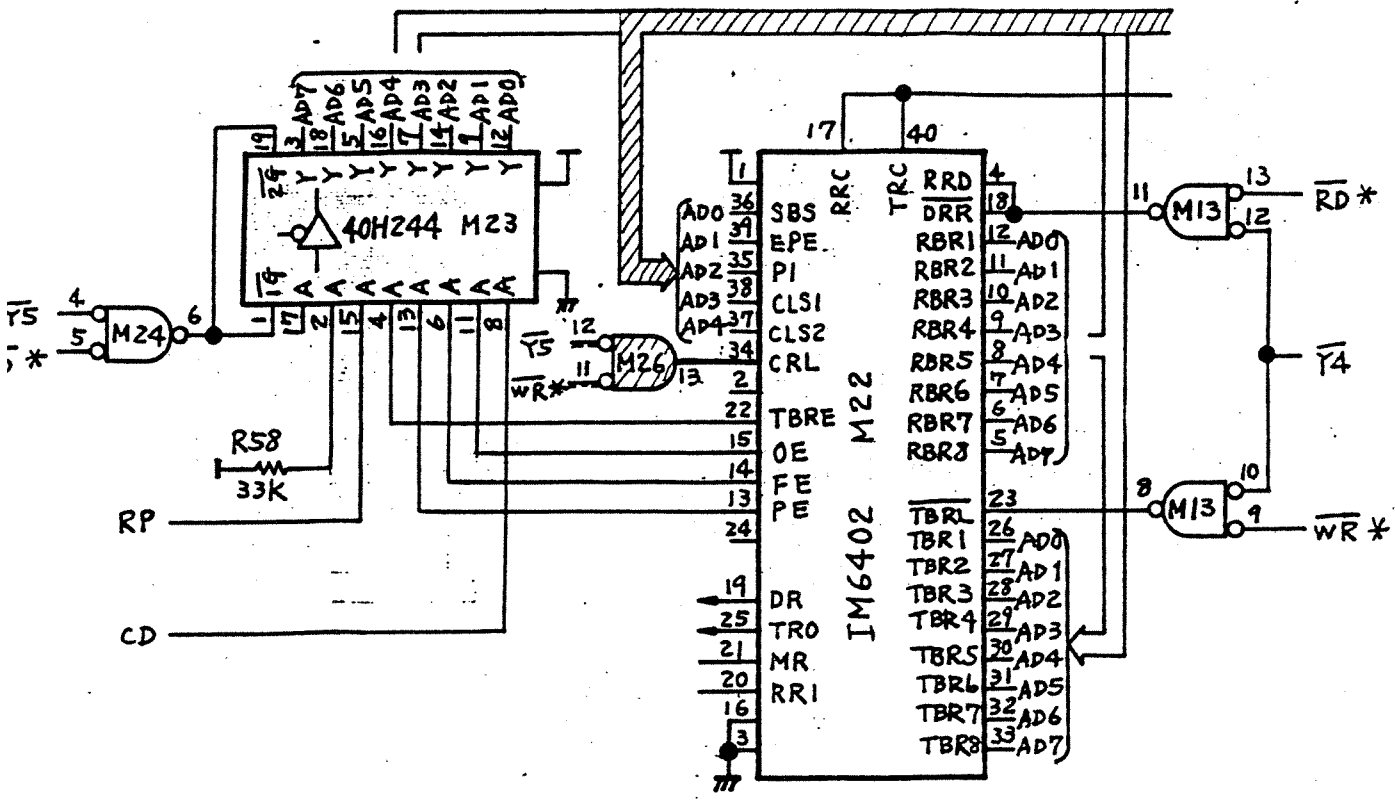


Fig. 41-1 Data Output

The serial interface circuitry is divided into three parts. One is the serial control circuitry, which controls the changes and transmission/reception of data (parallel data and serial data) between the CPU and the MODEM and RS-232C circuits, the second is RS-232C interface circuit, and the third is MODEM circuit.

(1) Serial Control Circuit

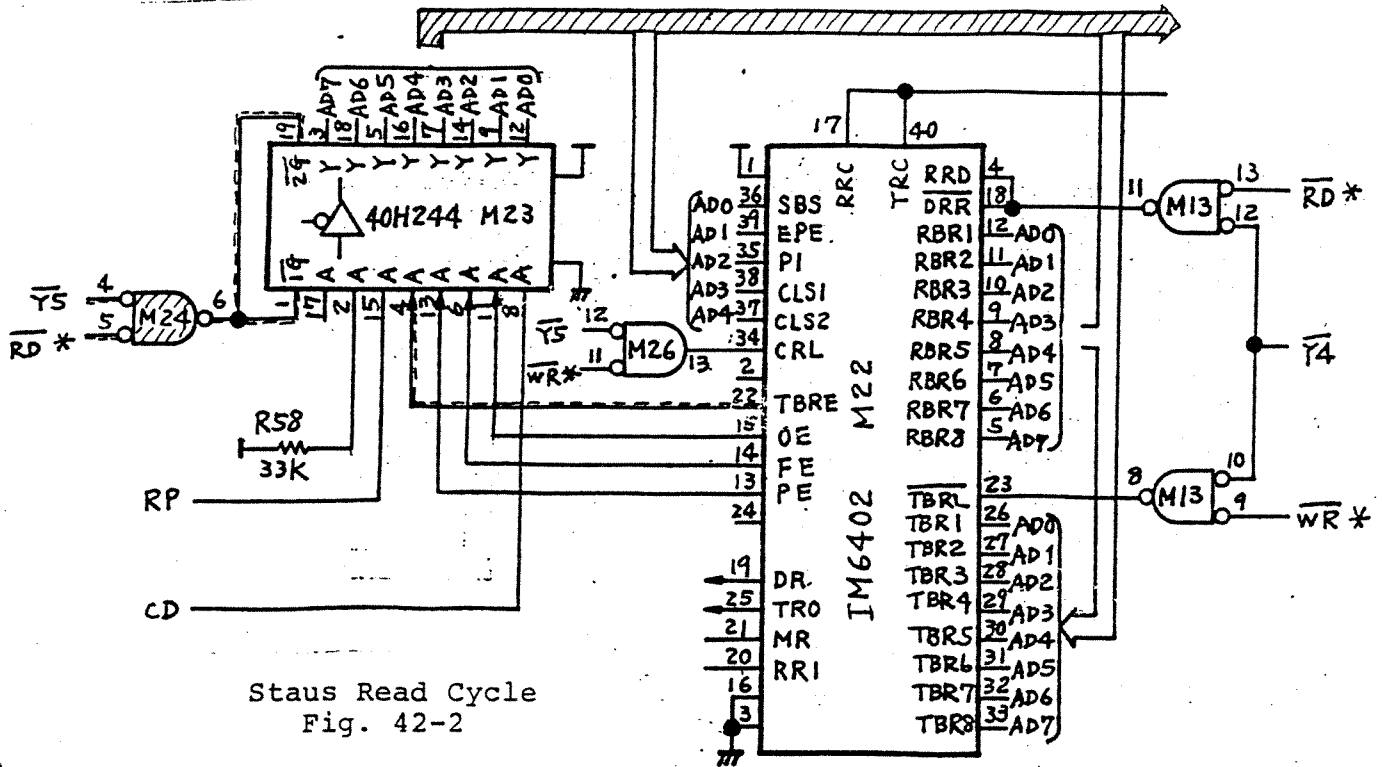
As shown in Fig.42-1, serial control of the Model 100 is done by the UART LSI (IM6402), and the CPU begins data transmission/reception after the control word, which determines the mode (transmission/reception), is written into the control register selected by the $\overline{Y5}$ signal.



Control Register Load Cycle

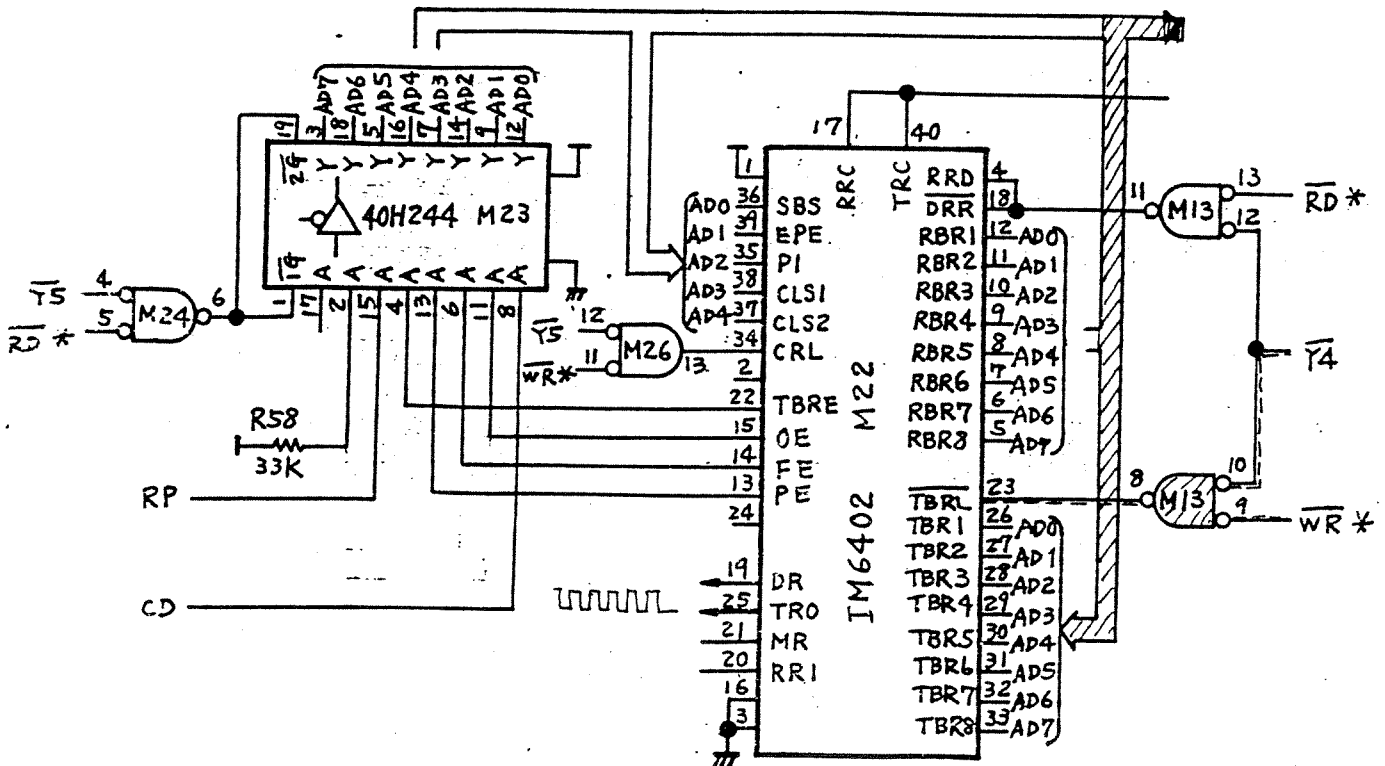
Fig.42-1

For transmission , the conditio of IM6402 TBRE signal from bit 4of the status input port (M23) selected by the Y5 signal is read, and ,if it is "L" ,it waits until it is "H". (shown in Fig.42-2)



Status Read Cycle Fig. 42-2

When the TBRE signal becomes "H" , data transmission is then possible , so that if the transmission data is written into the transmitter buffer register (TBR1-TBR8) , the data is output as serial data ,including the start ,parity and stop bits from the TRO terminal . (shown in Fig42-3)

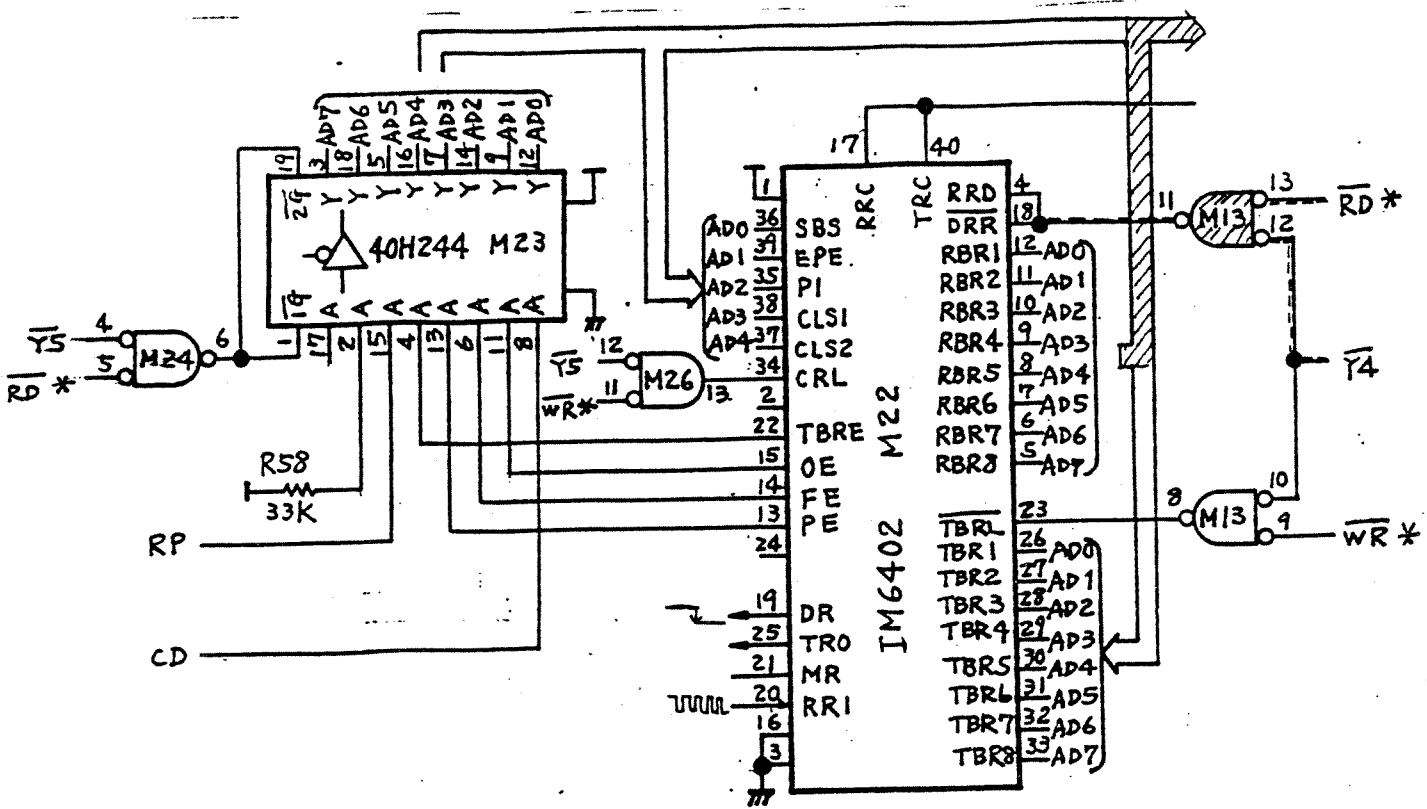


Data Transmission Cycle

For reception ,when the reception data enters the RRI terminal , the DR terminal changes from "L" to "H",and the RST6.5 interruption notifies the CPU that reception data has entered IM6402, as shown in Fig.42-4.

The CPU read the OE, FE and PE signals from the status input port (M23) ,and ,if there is no error when the serial data is received , the reception data from the receive buffer register selected by $\overline{Y4}$ can be read as 8-bit parallel data.

The IM6402 serial transmission/reception reference clock signal is taken from the T0 terminal by setting the 81C55 timer.



Data Reception Cycle

Fig.42-4

In addition , the status input port bit 5 RP signal is held as an option for MODEM operation.

Table 26 below shows the signal correspondence between the data bus and status bit and control register of IM6402.

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TABLE 26

Data Bus	Control Register	Status Bit
AD0	SBS (Stop Bit Select)	
AD1	EPE (Even Parity Enable)	OE (Overrun Error)
AD2	P1 (Parity Inhibit)	FE (Framing Error)
AD3	CLS1 (Character Length Selected 1)	PE (Parity Error)
AD4	CLS2 (Character Length Selected 2)	TBRE (Transmitter Buffer Empty)
AD5	_____	_____
AD6	_____	_____
AD7	_____	_____

Then ,because the serial input/output port which forms IM6402 is one channel only, the circuit shown in Fig. 43 is multiplexed to RS-232C and the MODEM. RS-232C signal (PB3 terminal of 81C55) determines whether the serial port is to be used as RS-232C or as MODEM. When the RS-232C signal is "L",the serial port is used as RS-232C ,when it is "H", the port is used as MODEM. The reception signal , including the control signal , is demultiplexed at M3 and the transmission signal is multiplexed at M24 and M26.

The CTS and DSR signals (as the serial port)are input to PC4 and PC5 of 81C55,and the CD signal is input from bit 0 of the status input port (M23). Output signals DTR and RTS are output from PB6 and PB7 of 81C55.

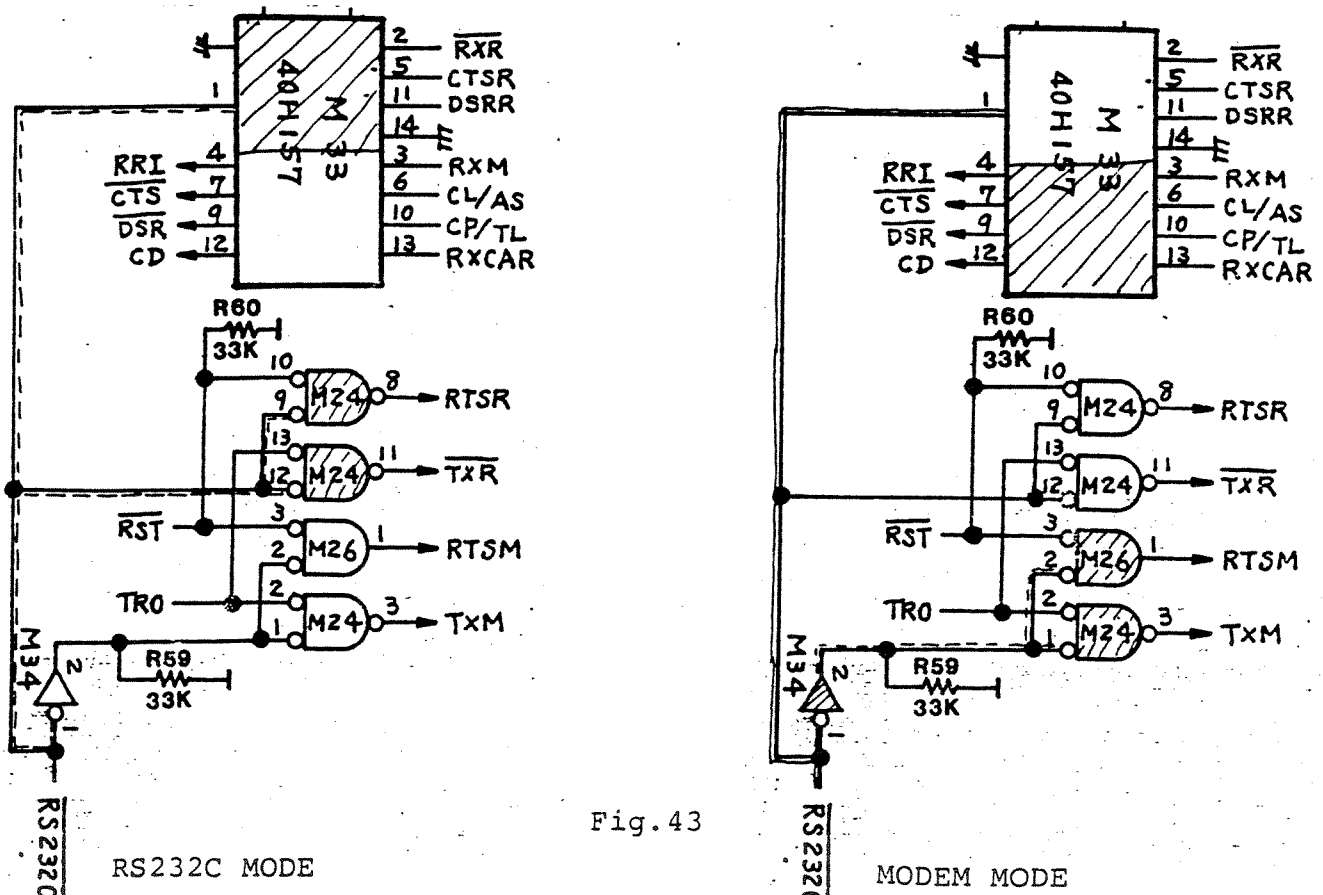


Fig.43

(2) RS-232C Circuits

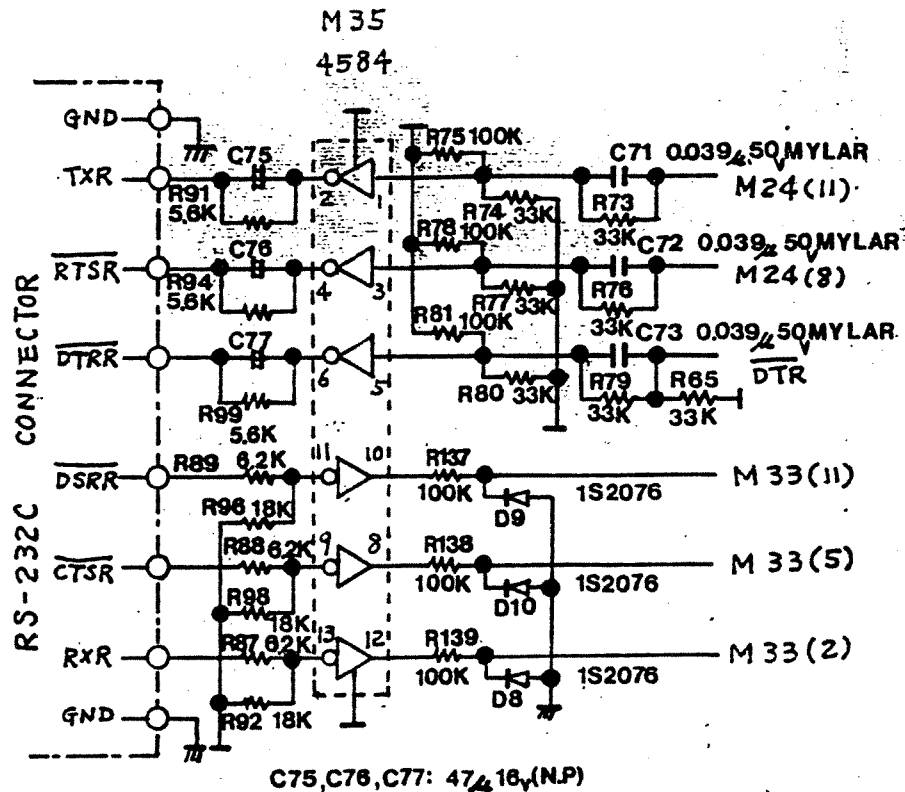


Fig. 44

In the RS-232C transmission circuit, after the DC component is removed from the IM6402 TRO signal and the RTS signal and from the DTR signal by the coupling capacitor (0.039 μ F 50 V), the signals are leveled to ± 5 V signals by the Schmitt trigger type inverter IC (M35), and are output as RS-232C transmission signals.

In the RS-232C reception circuit, the DSRR, CTSR and R x R signals from the external RS-232C line are subjected to waveform shaping and inversion by M35 and the diode (IS1535), and then converted to +5 V GND level signals, after which they are demultiplexed by 40H157 (M33) and converted to CTS, DSR and RRI signals which can be

controlled by the CPU.

Table 27 shows the application of each signal of the RS-232C circuits.

Table 27

Symbol	Name	Application
TXR	Transmit Data	Data Output from RS-232C
RXR	Receive Data	Data input to RS-232C
RTSR	Request to Send	
CTSR	Clear To Send	
DSRR	Data Set Ready	
DTRR	Data Terminal Ready	

The information below concerns the RS-232C driver and receiver.

- . Maximum distance transmission 5 M
- . Driver maximum output voltage . . . ±5 V
- . Driver minimum output voltage . . . ±3.5 V
- . Receiver maximum input voltage . . . ±18 V
- . Receiver minimum input voltage . . . ±3 V
- . In conformity to EIA standard RS-232C

5) MODEM CIRCUITRY

The modem circuitry consists of the modulation/demodulation LSI, the transmission filter, the reception filter, and other circuits.

(a) Modulation/demodulation LSI

The MC14412 contains a complete FSK (Frequency-Shift Keying) modulator and demodulator compatible with both foreign (C.C.I.T.T. standards) and U.S.A. low speed (0 to 600 (bps) communication networks.

- On Chip Crystal Oscillator
- Echo Suppressor Disable Tone Generator
- Originate and Answer Modes
- Simplex, Half-Duplex, and Full Duplex Operation
- On Chip Sine Wave Generator
- Modem Self Test Mode
- Single Supply: $V_{DD} = 4.75$ to 15 Vdc MC14412FP, MC14412FL
 $V_{DD} = 4.75$ to 8.0 Vdc MC14412VP, MC14412VL
- Selectable Data Rates: 0-200, 0-300, 0-600 bps
- Post Detection Filter
- TTL or CMOS Compatible Inputs and Outputs

TYPICAL APPLICATIONS:

- Stand Alone Low-Speed Modems
- Built-In Low Speed Modems
- Remote Terminals, Acoustical Couplers
- Credit Verification
- Point of Sale
- Remote Data Collection
- Remote Process Control
- Radio Data Transmission

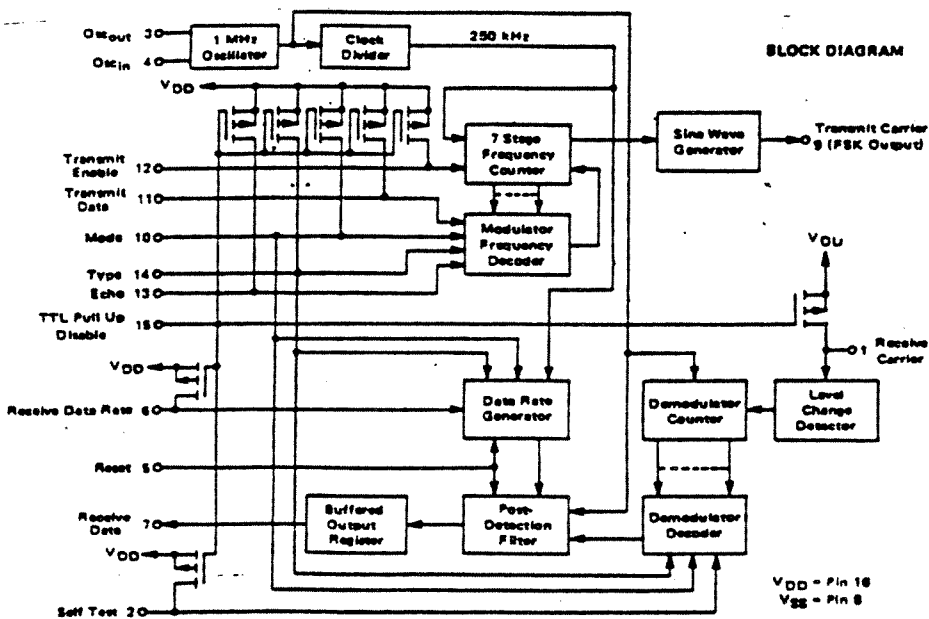


Fig. 45

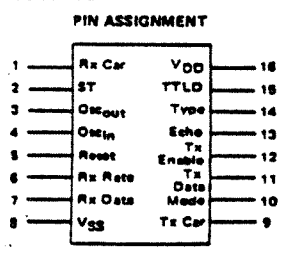


Fig .46 Pin Assignment

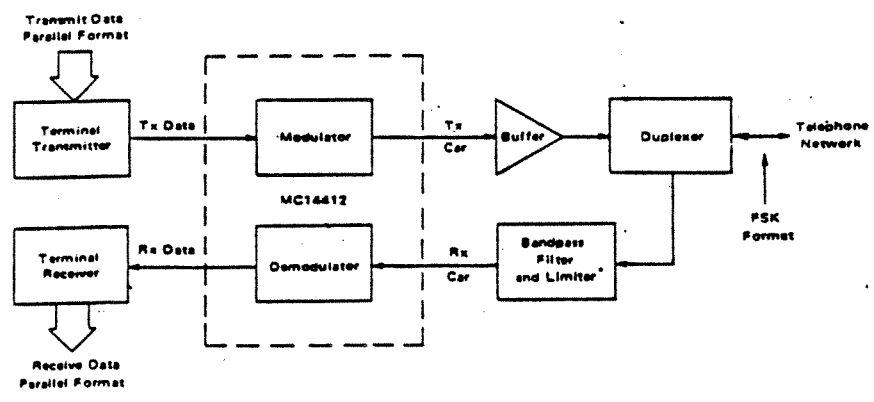


Fig.47 Application

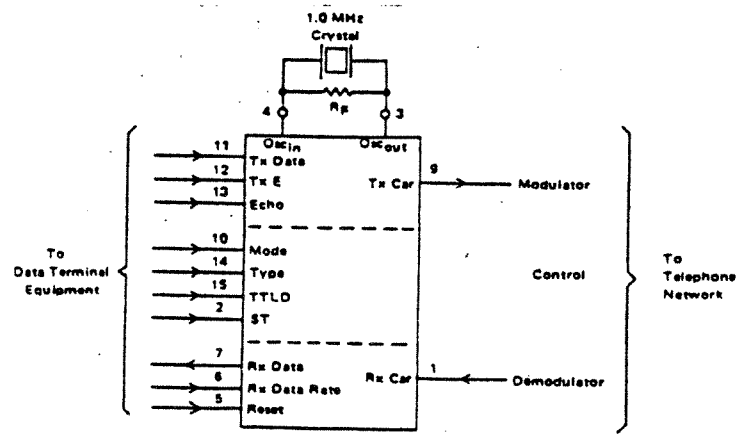


Fig.48 Input Output Signals

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltages MC14412FP MC14412VP	V _{DD}	-0.5 to 15 -0.5 to 6.0	Vdc
Input Voltages, All Inputs	V _{in}	V _{DD} + 0.5 to V _{SS} - 0.5	Vdc
DC Current Drain per Pin (except Pin 8, 7)	I	10	mAdc
DC Current Drain (Pin 8, 7)	I	35	mAdc
Operating Temperature Range	T _A	-40 to +85	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD} ** Vdc	-40°C		+24°C			+85°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	V _{OL}	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
		10	-	0.05	-	0	0.05	-	0.05	
		15	-	0.05	-	0	0.05	-	0.05	
	V _{OH}	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
		10	9.95	-	9.95	10	-	9.95	-	
		15	14.95	-	14.95	15	-	14.95	-	
Input Voltage* (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc) Pins 12,15	V _{IL}	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc
		10	-	3.0	-	4.50	3.0	-	3.0	
		15	-	4.0	-	6.75	4.0	-	4.0	
	V _{IH}	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
		10	7.0	-	7.0	5.50	-	7.0	-	
		15	11.0	-	11.0	8.25	-	11.0	-	
Output Drive Current (Pin 7) (V _{OH} = 2.5) (V _{OH} = 9.5) (V _{OH} = 13.5) (V _{OL} = 0.4) (V _{OL} = 0.5) (V _{OL} = 1.5)	I _{OH}	5	-0.62	-	-0.5	-1.5	-	-0.35	-	mAdc
		10	-0.62	-	-0.5	-1.0	-	-0.35	-	
		15	-1.8	-	-1.5	-2.5	-	-1.1	-	
	I _{OL}	4.75	2.3	-	2.0	4.0	-	1.6	-	mAdc
		10	5.3	-	4.5	10	-	3.6	-	
		15	15	-	13	35	-	10	-	
Input Current (Pin 15 = V _{DD})	I _{in}	-	-	-	±0.00001	±0.1	-	-	μAdc	
Input Pull-Up Resistor Source Current (Pin 15 = V _{SS} , V _{in} = 2.4 Vdc) Pins 1,2,5,6,10,11,12,13,14	I _p	5	285	-	250	460	-	205	-	μAdc
Input Capacitance	C _{in}	-	-	-	-	5.0	-	-	-	pF
Total Supply Current (Pin 15 = V _{DD})	I _T	5	-	4.5	-	1.1	4.0	-	3.5	mAdc
		10	-	13	-	4.0	12	-	11	
		15	-	27	-	8.0	25	-	23	
Modulator/Demodulator Frequency Accuracy (Excluding Crystal)	ACC	5 to 15	-	-	-	0.5	-	-	-	%
Transmit Carrier Output 2nd Harmonic	V _{2H}	5 to 10	-	-	-20	-26	-	-	-	dB
		10 to 15	-	-	-25	-32	-	-	-	
Transmit Carrier Output Voltage (R _L = 100 kΩ) (Pin 9)	V _{out}	5	-	-	0.2	0.30	-	-	-	VRMS
		10	-	-	0.5	0.65	-	-	-	
		15	-	-	1.0	1.5	-	-	-	
Receive Carrier Rise and Fall Times (Pin 1)	t _{TLH} , t _{THL}	5	-	15	-	-	15	-	15	ns
		10	-	5.0	-	-	5.0	-	5.0	
		15	-	4.0	-	-	4.0	-	4.0	

Table 28

General

Fig.50 shows the MODEM in a system application .The data to be transmitted is presented in serial format to the modulatorfor conversion to FSK signals for transmission over the telephone network. The modulator output is buffered/amplified dividing the 600 ohm telephone line.

The FSK signal from the remote MODEM is received via the telephone line and filtered to remove extraneous signals such as the local Transmit Carrier . This filtering can be either a bandpass which passes only the desired band of frequencies or a notch which rejects the known interfering signal. the desired signal is then limited to preserve the axis crossings and fed to the demodulator where the data is recovered from the received FSK carrier.

Pin Functions

<u>symbol</u>	<u>function</u>
TYPE	The type input selects either the U.S. or C.C.I.T.T. operational frequencies for both transmitting and receiving data . When the type input ="1" , the U.S. standard is selected and when the type input ="0", the C.C.I.T.T. standard is selected.
Tx Data	Transmit data is the binary informationinput. Data entered for transmission is modulated using FSK techniques. When operating the U.S.standard (TYPE="1") a logic "1" input level represents a Mark When operating in the C.C.I.T.T. standard (TYPE="0") a logic "1" input level represents a Mark.
Tx Car	The transmit carrier is a digital -synthesized sine wave derived from a 1.0MHz oscillator reference. The frequency characteristics are as follows:

United States Standard TYPE="1"		
Transmit Frequency		ECHO ="0"
Mode	Tx Data	Tx Car
Originate "1"	Mark "1"	1270Hz
Originate "1"	Space "0"	1070Hz
Answer "0"	Mark "1"	2225Hz
Answer "0"	Space "0"	2025Hz
C.C.I.T.T. Standard TYPE="0"		
Transmit Frequency		ECHO="0"
Mode	Tx Data	Tx Car
Channel No.1 "1"	Mark "1"	980Hz
Channel No.1 "1"	Space "0"	1180Hz
Channel No.2 "0"	Mark "1"	1650Hz
Channel No.2 "0"	Space "0"	1850Hz

Table 29

Echo Suppressor TYPE="0"
 Disable Tone ECHO="1"
 Mode Tx Data Tx Car
 Chan. No.2"0" "1" 2100Hz

92

Table 30

symbol

function

Tx Enable The transmit carrier output is enabled when the Tx enable input ="1" . No output tone can be transmitted when Tx enable ="0".

MODE The mode input selects the pair of transmitting and receive frequencies used during modulation and demodulation . When mode="1", the U.S. originate is selected (type input ="1") or the C.C.I.T.T. channel No. 1 (type="0"). When mode ="0", the U.S. answer mode is selected (type ="1") or the C.C.I.T.T. channel No.2 (type input ="0").

ECHO When the Echo input ="1" (type ="0",Mode ="0", Tx Data ="1") the demodulator will transmit a 2100 Hz tone for the disabling line echo suppressors. During normal data transmission, this input should be low="0".

Rx Data The receive data output is digital data resulting from demodulation the Receive Carrier.

Rx Car The receive carrier is the FSK input to the demodulation . This input must have either C mos or TTL compatible logic level input (see TTL pull up disable) at a duty cycle of 50%±4%, that is a square wave resulting from the signal limiter.

Rx Rate The demodulator has been optimized for signal to noise performance at 200,300, and bps. The receive carrier must change frequency for more than half of the selected data rate period before the receive data output will change.

Data Rate	Rx rate	Type
0-200bps	"1"	"0"
0-300bps	"1"	"1"
0-600bps	"0"	"1"

SELF TEST When a high level (ST="1") is placed on this input , the demodulator is switched to the modulator frequency.

Reset This input is provided to decrease the time of the chip. In normal operation , this input may be used to disable the demodulator (Reset="1") - otherwise it should be tied low="0".

symbol

Osc in, Osc out

function

A 1.0 MHz crystal is required to utilize the on chip oscillator . A 1.0MHz square wave clock can also be applied to the Osc in input to satisfy the clock requirement. When utilizing the 1.0 MHz crystal, external parasitic capacitance , including crystal shunt capacitance , must be < 9PF at the crystal input

TTL

To improve TTL interface compatibility, all of the inputs to the MODEM have controllable P-channel devices which act as pull-up resistors when TTL input is low ("0" . when the input is taken high ("1") the pull up is disabled, thus reducing power dissipation when interfacing with C-MOS.

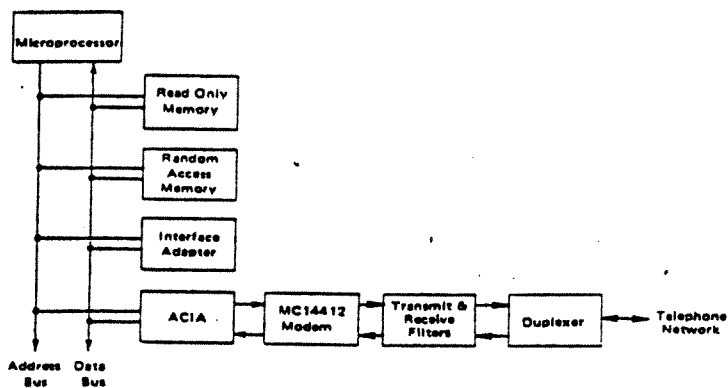


Fig. 49 System Block Diagram

(d) Reception filter and comparator circuitry

As shown in Fig.52, the reception circuit input signal passes through the coupling capacitor (C40) , is then amplified, passes through the 3-stage band-pass filter (composed of an active filter), is then amplified once again , passes through the comparator, and, then after being changed to a square wave, is input at the RX CAR terminal of MCl4412.

The intermediate frequencies of the 3-stage active filter are shown in the chart below.

The switching of the intermediate frequency for the originate mode and the answer mode is accomplished by switching T2, T3 and T5 ON or OFF according to the ORIG-ANS switch setting, thus changing the value of R16, R28 and R25.

The transmit carrier signal output from the TX CAR terminal is DC by C61, and the signal level is adjusted to -26.5 dB by the control (VR2). The signal then passes through the transmission filter (band-pass filter) and is sent to the telephone line or the acoustic coupler.

The transmission filter is composed of an active filter consisting of an operation amplifier , and the intermediate frequency must be switched according to the mode (originate or answer).

Depending on the ORIG-ANS switch setting , the transistor T4 is ON or OFF, so that R42 is 2.3K for the answer mode, and the synthesis resistance of the R42 and R45 value determines the originate mode .

The intermediate frequency of the active filter is 1170Hz for the originate mode , and 2125Hz for the answer mode.

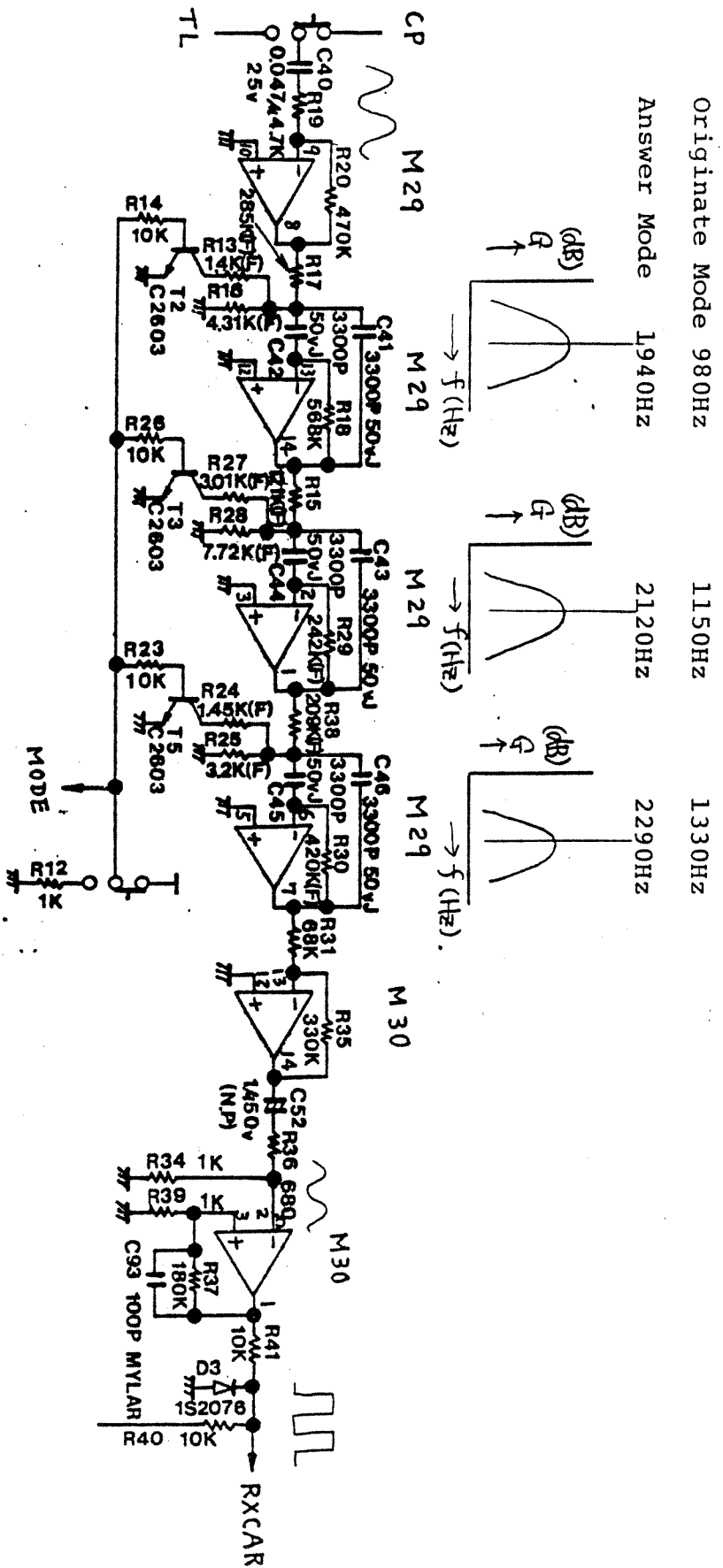


Fig. 52

(e) Other circuits

The transmission signal and the reception signal are directly connected to the connector (TxM, RxM) during the acoustic coupler mode, but, during the direct telephone mode, are connected to the secondary side of the driver transformer, and the primary side of this transformer is connected to the telephone line via the connector. (TxMD, RxMD)

The ACP-DIR switch is used for selection of the acoustic coupler or telephone line.

RY3 is a relay that, when the Model 100 is used in the terminal mode, avoids interference from the audio input signal from the telephone receiver by separating the signal (TL) from the telephone receiver. RY2 separates the modem circuit and the telephone at the conclusion of use in the terminal mode and is used as an automatic dialer.

T26 is switched OFF when the optional answering phone is used, and it separates the pull-up resistor R100 (in the input signal line of the acoustic coupler) from the V_{DD} line.

The other signals (WR and RD) of the modem connector are used when the optional answering telephone is used.

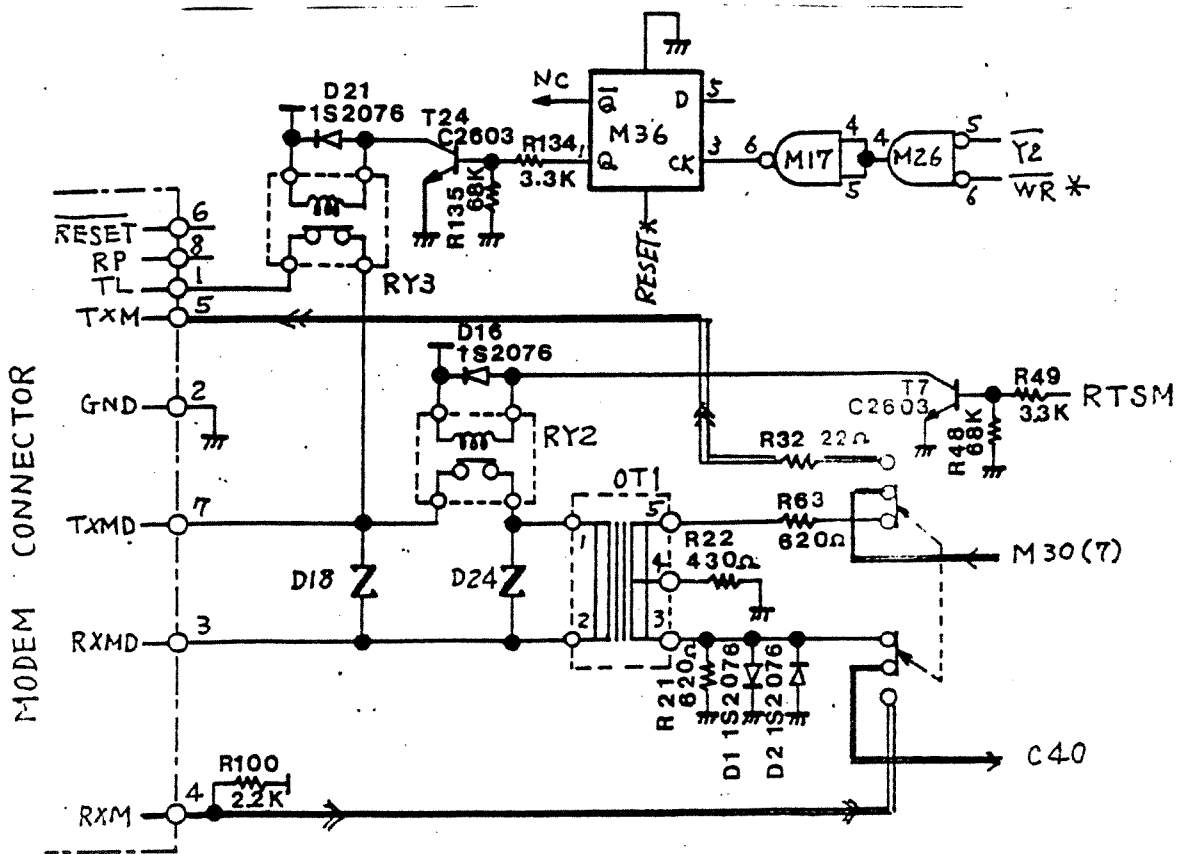


Fig.53-1 Acoustic Coupler Mode

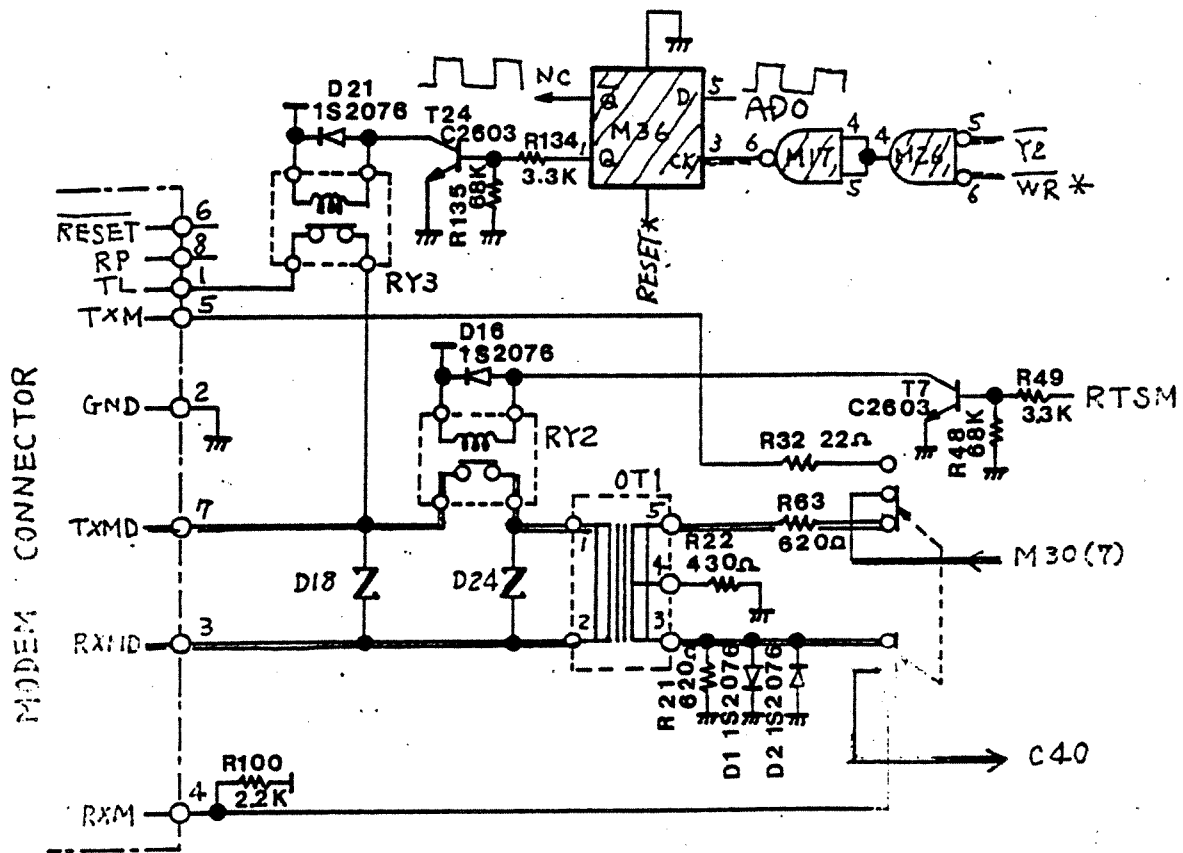


Fig. 53-2 Direct Telephone and Terminal Mode

15. Power Supply and Auto Power OFF Circuit

For Model 100, ± 5 V is the power supply of the logic. This power is supplied by the DC/DC converter. In addition, a special feature of Model 100 is the Automatic Power OFF function.

This circuit is shown in Fig. 54.

The circuits will be described by dividing them into the circuit which supplies the power, and the low-power detection and automatic power OFF circuits.

(1) DC/DC Converter Circuit

OT2 is a converter transformer which oscillates T21 and T22 and generates voltage at the secondary side of the transformer.

At the same time the power is switched ON, a very slight collector current flows to T21 and T22. A voltage between pins 7 and 9 of the converter transformer is generated, and the T22 base potential becomes positive; in other words, the base polarity becomes biased in the forward direction. This voltage causes the T21 and T22 base current to flow, and the collector current is increased. Although the collector current is increased in this way, when it can longer increase, because of transistor saturation resistance and converter coil resistance, the voltage between pins 7 and 9 begins to attenuate, and, as a result, the base current and collector current attenuate, causing T21 and T22 to be cut off all at once because of the reverse playback action.

Until immediately before the transistor is cut off, excitation current flows to the transformer.

Because the current is suddenly cut off as a result of the transistor cut-off, a counter voltage is generated, the distributed capacity of the coil is charged, and, as a result, an oscillation voltage is generated at the base coil.

Then, when the base potential progresses to a half cycle of the oscillation voltage, it is biased in the forward direction, T21 and T22 are switched ON once again, and oscillation such as that shown in Fig.55 occurs.

In this way, AC voltage corresponding to the number of windings is generated at the secondary side of the converter, and this voltage is rectified and smoothed by D13, D15, C84 and C85.

Moreover, the voltage fluctuations of VDD (+5 V) are fed back to the primary side of the oscillation transistor by T13, D4, R121 and C92 in order to improve stability. C81 and R126 are a differentiation circuit designed to make the playback operation of the oscillation transistor easier. AC short circuits the circuit, so that the oscillation frequency is affected by the time-constant of this C and R.

In this circuit, because feedback is applied by VDD, which makes stability difficult, VEE (-5 V) is stabilized by R97 and D14. (The voltage at both ends of C85 is about -7 V.)

(2) Low-Power Detection and Automatic Power OFF Circuitry

The low-power detection circuit illuminates an LED warning lamp when the battery voltage decreases. If it continues to decrease, the system power will be switched OFF just before the voltage becomes so low that the converter cannot operate.

There is more than 20 minutes between the time when the LED lamp illuminates and the system is switched OFF (if no I/O devices are connected).

Battery voltage is detected by splitting the resistance of R144, R108, R105 and R116. When battery voltage (V_L) becomes $4\text{ V} \pm 0.1\text{ V}$, T16 is switched OFF, T17 is switched ON, T19 is driven, and the LED illuminates. (The LED is located on the LCD PWB.)

When V_L becomes $3.7\text{ V} \pm 0.1\text{ V}$, T14 is switched OFF, T15 is switched ON, and LPS changes from "H" to "L." This signal is inverted by M27, and is fed to the TRAP terminal of 80C35. If the CPU acknowledges this signal, sends the P.C.S. signal passing through the PB4 of 81C55 after the internal operations.

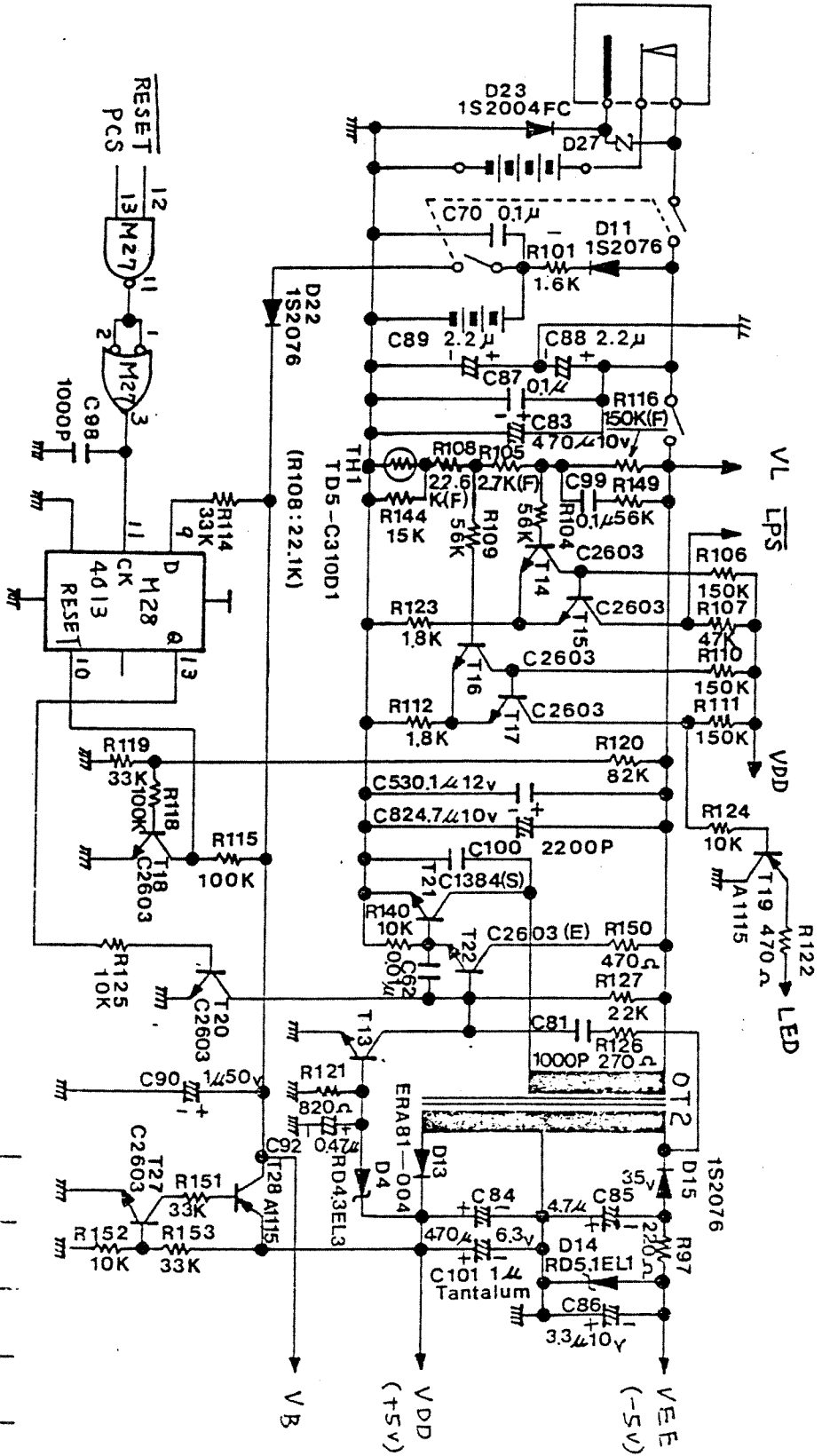
The P.C.S. signal is active "H".

When P.C.S. becomes "H", the Q output of M28 (4013: "D" type F/F) becomes "H", T20 operates, and the oscillation of the converter is stopped.

If there is no operation for 10 minutes or more (awaiting a command for 10 minutes or more), P.C.S. is output from PB4 of 81C55.

When the power switch is switched OFF, T18 is switched OFF, the M28 RESET terminal becomes "L" and oscillation is resumed by switching the power switch ON. If, however, the power is reduced by the L.P.S. signal, battery replacement is necessary. R123 and R112 are resistors to provide hysteresis.

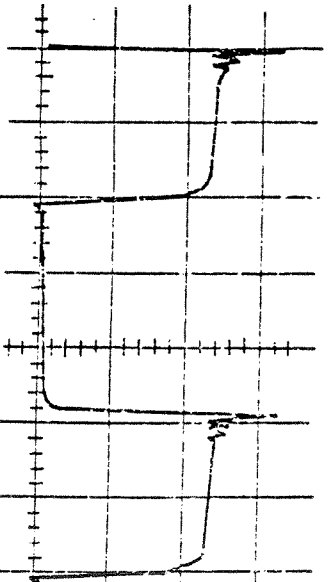
Fig. 54



T13: C2603(E)

5V/DIV
5usec/div

Fig. 55



16. Reset Circuit

This circuit supplies the CPU $\overline{\text{RESET}}$ signal and also the RAM RST signal as the RAM protecting signal when the power decreases.

The circuit diagram is shown in Fig. 56 .

R103 and C78 delay the introduction of input power so that T11 is switched ON and T10 is switched OFF about msec after VDD is activated, with the result that the $\overline{\text{RESET}}$ signal changes from "L" to "H". This $\overline{\text{RESET}}$ waveform is inverted by T9 and is the RAM RST signal. R141 provides hysteresis to the $\overline{\text{RESET}}$ signal. Thermistor THz suppresses $\overline{\text{RESET}}$ signal fluctuations due to temperature.

T25 receives the signal during automatic power OFF, short-circuiting both ends of C78, and resets the system.

The $\overline{\text{RESET}}$ signal is active "L", and the RAM RST signal is active "H."

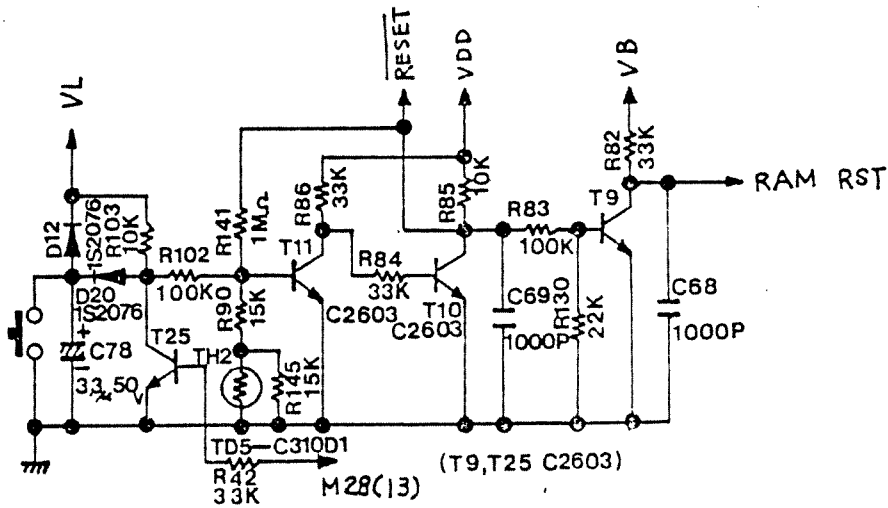


Fig. 56 RESET circuit diagram

MAIN P.W.B ASSY PARTS LIST (cont'd)

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SYMBOL	DESCRIPTION	MANUFAC Turer'S PART NUMBER	RADIO SHACK PART NUMBER
M1	TC40H373P CMOS LOGIC IC	QQ040373AT	
M2	TC40H245P CMOS LOGIC IC	QQ040245AT	
M3	TC40H138P CMOS LOGIC IC	QQ040138AT	
M4	TC40H138P CMOS LOGIC IC	QQ040138AT	
M5	TC40H139P CMOS LOGIC IC	QQ040139AT	
M6	RAM PACK(OPTION)CMOS 8KB	QQHX1003A6	
M7	RAM PACK(OPTION)CMOS 8KB	QQHX1003A6	
M8	RAM PACK(OPTION)CMOS 8KB	QQHX1003A6	
M9	RAM PACK CMOS 8KB	QQHX1001A6	
M10	SYSTEM BUS IC SOCKET		
M11	OPTION ROM CMOS 32KB		
M12	ROM CMOS 32KB		
M13	TC40H032P CMOS LOGIC IC	QQ040032AT	
M14	TC40H175P CMOS LOGIC IC	QQ040175AT	
M15	TC40H244P CMOS LOGIC IC	QQ040244AT	
M16	TC40H138P CMOS LOGIC IC	QQ040138AT	
M17	TC40H000P CMOS LOGIC IC	QQ040000AT	
M18	uPD1990AC CMOS TIMER	QQ001990BA	
M19	80C85 CMOS CPU	QQ008085A5	
M20	TC40H367P CMOS LOGIC IC	QQ040367AT	
M21	TC40H244P CMOS LOGIC IC	QQ040244AT	
M22	IM6402 CMOS UART	QQ006402AZ	
M23	TC40H244P CMOS LOGIC IC	QQ040244AT	
M24	TC40H032P CMOS LOGIC IC	QQ040032AT	
M25	81C55 CMOS PIO	QQ008155A5	
M26	TC40H002P CMOS LOGIC IC	QQ040002AT	
M27	4011 CMOS LOGIC IC	QQ004011AT	
M28	4013 CMOS LOGIC IC	QQ004013AT	
M29	TL064CN O.P AMP	QQM00064Au	
M30	TL064CN O.P AMP	QQM00064Au	
M31	MCI4412 CMOS MODEM	QQ014412AM	
M32	TC40H244P CMOS LOGIC IC	QQ040244AT	
M33	TC40H157P CMOS LOGIC IC	QQ040157AT	
M34	HD14584 CMOS LOGIC IC	QQ014584AT	
M35	HD14584 CMOS LOGIC IC	QQ014584AT	
M36	4013 CMOS LOGIC IC	QQ004013AA	
M37	1S2076 SILICON DIODE	QDSS2076#B	

MAIN P.W.B ASSY PARTS LIST(cont'd)

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SYMBOL	DESCRIPTION	MANUFACTURE'S	RADIO SHACK PART NUMBER
D2	1S2076 SILICON DIODE	QDSS2076#B	
D3	1S2076 SILICON DIODE	QDSS2076#B	
D4	RD4.3EL3 ZENER DIODE	QDZ4R3EL3A	
D5	1S2076 SILICON DIODE	QDSS2076#B	
↓	↓	↓	
D12	1S2076 SILICON DIODE	QDSS2076#B	
D13	ERA81-004 SILICON DIODE	QDS81004XZ	
D14	RD5.1EL1 ZENER DIODE	QDZ5R1EL1A	
D15	1S2076 SILICON DIODE	QDSS2076#B	
D16	1S2076 SILICON DIODE	QDSS2076#B	
D17	1S2076 SILICON DIODE	QDSS2076#B	
D18	ERZ-C10K201 ZNR	QNHDK201AN	
D19	1S2076 SILICON DIODE	QDSS2076#B	
↓	↓	↓	
D22	1S2076 SILICON DIODE	QDSS2076#B	
D23	1S2004FC SILICON DIODE	QDSS2004X4	
T1	2SA1115 TRANSISTOR	QTA1115XAE	
T2	2SC2603 TRANSISTOR	QTC2603XAE	
↓	↓	↓	
T11	2SC2603 TRANSISTOR	QTC2603XAE	
T12	2SA1115 TRANSISTOR	QTA1115XAE	
T13	2SC2603 E-RANK TRANSISTOR	QTC2603XCE	
↓	↓	↓	
T17	2SC2603 E-RANK TRANSISTOR	QTC2603XCE	
T18	2SC2603 TRANSISTOR	QTC2603XAE	
T19	2SA1115 TRANSISTOR	QTA1115XAE	
T20	2SC2603 TRANSISTOR	QTC2603XAE	
T21	2SC1384 S-RANK TRANSISTOR	QTC1384XHN	
T22	2SC2603 E-RANK TRANSISTOR	QTC2603XCE	
T23	2SC2603 TRANSISTOR	QTC2603XAE	
T24	2SC2603 TRANSISTOR	QTC2603XAE	
T25	2SC2603 TRANSISTOR	QTC2603XAE	
T26	2SA1115 TRANSISTOR	QTA1115XAE	
T27	2SC2603 TRANSISTOR	QTC2603XAE	
T28	2SA1115 TRANSISTOR	QTA1115XAE	
X1	32.768KHZ CRYSTAL	XTR1A1001X	
X2	4.9152MHZ CRYSTAL	XBRLA1003X	
X3	1.0MHZ CRYSTAL	XAZ1C2001X	

MAIN P.W.B ASSY PARTS LIST(cont'd)

106

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
OT1	E6732B DRIVER TRANS	TDZ19A002K	
OT2	TN22A CONVERTOR TRANS	TC12RZ001B	
TH1	TD5-C310D1 THERMISTOR	QHQ5C310ZP	
TH2	TD5-C310D1 THERMISTOR	QHQ5C310ZP	
RY1	FBR2011CD005M RELAY	ZRA265101Z	
RY2	764D5/1AS-T RELAY	ZRA164102Z	
RY3	764D5/1BS-T RELAY	ZRA164101Z	
MR1	100KX8 RESISTOR NETWORK	RAB104M08X	
MR2	100KX8 RESISTOR NETWORK	RAB104M08X	
MR3	100KX8 RESISTOR NETWORK	RAB104M08X	
MR4	33KX8 RESISTOR NETWORK	RAB333M08X	
MR5	100KX8 RESISTOR NETWORK	RAB104M08X	
MR6	100KX8 RESISTOR NETWORK	RAB104M08X	
MR7	100KX8 RESISTOR NETWORK	RAB104M08X	
VR1	K091A 50K (B) VOLUME	RV9A503B01	
VR2	VM6CK-PV(1s) 50K(B) VOLUME	RPSNB50303	
R1	1K 1/4W 5% CARBON FILM	RD25PJ102X	
R2	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R3	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R4	33K 1/4W 5% CARBON FILM	RD25PJ333X	
↓		↓	
R7	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R8	1K 1/4W 5% CARBON FILM	RD25PJ102X	
↓		↓	
R12	1K 1/4W 5% CARBON FILM	RD25PJ102X	
R13	1.4K 1/4W 1% M-OXIDE FILM	RQBPF1401X	
R14	10K 1/4W 5% CARBON FILM	RD25PJ103X	
R15	121K 1/4W 1% M-OXIDE FILM	RQBPF1213X	
R16	4.31K 1/4W 1% M-OXIDE FILM	RQBPF4311X	
R17	285K 1/4W 1% M-OXIDE FILM	RQBPF2853X	
R18	568K 1/4W 1% M-OXIDE FILM	RQBPF5683X	
R19	7.5K 1/4W 5% CARBON FILM	RD25PJ752X	
R20	470K 1/4W 5% CARBON FILM	RD25PJ474X	
R21	620 OHM 1/4W 5% CARBON FILM	RD25PJ621X	
R22	430 OHM 1/4W 5% CARBON FILM	RD25PJ431X	
R23	10K 1/4W 5% CARBON FILM	RD25PJ103X	
R24	1.45K 1/4W 1% M-OXIDE FILM	RQBF1451X	
R25	3.2K 1/4W 1% M-OXIDE FILM	RQBF3201X	
R26	10K 1/4W 1% CARBON FILM	RD25PJ102X	

MAIN P.W.B ASSY PARTS LIST (cont'd)

107

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
R27	3.01K 1/4W 1% M-OXIDE FILM	RQBF3011X	
R28	7.72K 1/4W 1% M-OXIDE FILM	RQBF7721X	
R29	242K 1/4W 1% M-OXIDE FILM	RQBF2423X	
R30	421K 1/4W 1% M-OXIDE FILM	RQBF4213X	
R31	68K 1/4W 5% CARBON FILM	RD25PJ683X	
R32	22 OHM 1/4W 5% CARBON FILM	RD25PJ220X	
R33	10K 1/4W 5% CARBON FILM	RD25PJ103X	
R34	1K 1/4W 5% CARBON FILM	RD25PJ102X	
R35	330K 1/4W 5% CARBON FILM	RD25PJ334X	
R36	680 OHM 1/4W 5% CARBON FILM	RD25PJ681X	
R37	180K 1/4W 5% CARBON FILM	RD25PJ184X	
R38	209K 1/4W 1% M-OXIDE FILM	RQBP2093X	
R39	1K 1/4W 5% CARBON FILM	RD25PJ102X	
R40	10K 1/4W 5% CARBON FILM	RD25PJ103X	
R41	560 OHM 1/4W 5% CARBON FILM	RD25PJ561X	
R42	3.01K 1/4W M-OXIDE FILM	RQBPF3011X	
R43	10K 1/4W 1% M-OXIDE FILM	RQBPF1002X	
R44	242K 1/4W 1% M-OXIDE FILM	RQBPF2423X	
R45	7.72K 1/4W 1% M-OXIDE FILM	RQBPF7721X	
R46	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R47	15M 1/4W 5% CARBON FILM	RD25PJ156X	
R48	68K 1/4W 5% CARBON FILM	RD25PJ683X	
R49	3.3K 1/4W 5% CARBON FILM	RD25PJ332X	
R50	3.3K 1/4W 5% CARBON FILM	RD25PJ332X	
R51	2.2K 1/4W 5% CARBON FILM	RD25PJ222X	
R52	1k 1/4W 5% CARBON FILM	RD25PJ102X	
R53	100K 1/4W 5% CARBON FILM	RD25PJ104X	
R54	12K 1/4W 5% CARBON FILM	RD25PJ123X	
R55	470 OHM 1/4W 5% CARBON FILM	RD25PJ471X	
R56	10K 1/4W 5% CARBON FILM	RD25PJ103X	
R57	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R62	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R63	620 OHM 1/4W 5% CARBON FILM	RD25PJ621X	
R64	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R68	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R69	NOT USED		
R70	33K 1/4W 5% CARBON FILM	RD25PJ333X	

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
R71	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R72	1K 1/4W 5% CARBON FILM	RD25PJ102X	
R73	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R74	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R75	100K 1/4W 5% CARBON FILM	RD25PJ104X	
R76	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R77	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R78	100K 1/4W 5% CARBON FILM	RD25PJ104X	
R79	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R80	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R81	100K 1/4W 5% CARBON FILM	RD25PJ104X	
R82	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R83	100K 1/4W 5% CARBON FILM	RD25PJ104X	
R84	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R85	10K 1/4W 5% CARBON FILM	RD25PJ103X	
R86	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R87	6.2K 1/4W 5% CARBON FILM	RD25PJ622X	
R88	6.2K 1/4W 5% CARBON FILM	RD25PJ622X	
R89	6.2K 1/4W 5% CARBON FILM	RD25PJ622X	
R90	15K 1/4W 5% CARBON FILM	RD25PJ153X	
R91	5.6K 1/4W 5% CARBON FILM	RD25PJ562X	
R92	18K 1/4W 5% CARBON FILM	RD25PJ183X	
R93	68K 1/4W 5% CARBON FILM	RD25PJ683X	
R94	5.6K 1/4W 5% CARBON FILM	RD25PJ562X	
R95	100 OHM 1/4W 5% CARBON FILM	RD25PJ101X	
R96	18K 1/4W 5% CARBON FILM	RD25PJ183X	
R97	270 OHM 1/4W 5% CARBON FILM	RD25PJ271X	
R98	18K 1/4W 5% CARBON FILM	RD25PJ183X	
R99	5.6K 1/4W 5% CARBON FILM	RD25PJ562X	
R100	2.2K 1/4W 5% CARBON FILM	RD25PJ222X	
R101	4.3K 1/4W 5% CARBON FILM	RD25PJ432X	
R102	100K 1/4W 5% CARBON FILM	RD25PJ104X	
R103	10K 1/4W 5% CARBON FILM	RD25PJ103X	
R104	56K 1/4W 5% CARBON FILM	RD25PJ563X	
R105	2.7K 1/4W 1% M-OXIDE FILM	RQBPF2701X	
R106	150K 1/4W 5% CARBON FILM	RD25PJ154X	
R107	68K 1/4W 5% CARBON FILM	RD25PJ683X	
R108	22.6K 1/4W 1% M-OXIDE FILM	RQBPF2262X	

MAIN P.W.B ASSY PARTS LIST(cont'd)

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SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
R109	56K 1/4W 5% CARBON FILM	RD25PJ563X	
R110	150K 1/4W 5% CARBON FILM	RD25PJ154X	
R111	150K 1/4W 5% CARBON FILM	RD25PJ154X	
R112	1.8K 1/4W 5% CARBON FILM	RD25PJ182X	
R113	10K 1/4W 5% CARBON FILM	RD25PJ103X	
R114	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R115	100K 1/4W 5% CARBON FILM	RD25PJ104X	
R116	150K 1/4W 1% M-OXIDE FILM	RQBPF1503X	
R117	100K 1/4W 5% CARBON FILM	RD25PJ104X	
R118	100K 1/4W 5% CARBON FILM	RD25PJ104X	
R119	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R120	82K 1/4W 5% CARBON FILM	RD25PJ823X	
R121	5.6K 1/4W 5% CARBON FILM	RD25PJ562X	
R122	470 OHM 1/4W 5% CARBON FILM	RD25PJ471X	
R123	1.8K 1/4W 5% CARBON FILM	RD25PJ182X	
R124	10K 1/4W 5% CARBON FILM	RD25PJ103X	
R125	10K 1/4W 5% CARBON FILM	RD25PJ103X	
R126	270 OHM 1/4W 5% CARBON FILM	RD25PJ271X	
R127	22K 1/4W 5% CARBON FILM	RD25PJ223X	
R128	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R129	10K 1/4W 5% CARBON FILM	RD25PJ103X	
R130	22K 1/4W 5% CARBON FILM	RD25PJ223X	
R131	1K 1/4W 5% CARBON FILM	RD25PJ102X	
R132	150K 1/4W 5% CARBON FILM	RD25PJ154X	
R133	NOT USED		
R134	3.3K 1/4W 5% CARBON FILM	RD25PJ332X	
R135	68K 1/4W 5% CARBON FILM	RD25PJ683X	
R136	62K 1/4W 5% CARBON FILM	RD25PJ623X	
R137	100K 1/4W 5% CARBON FILM	RD25PJ104X	
R138	100K 1/4W 5% CARBON FILM	RD25PJ104X	
R139	100K 1/4W 5% CARBON FILM	RD25PJ104X	
R140	10K 1/4W 5% CARBON FILM	RD25PJ103X	
R141	1M 1/4W 5% CARBON FILM	RD25PJ105X	
R142	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R143	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R144	15K 1/4W 5% CARBON FILM	RD25PJ153X	
R145	15K 1/4W 5% CARBON FILM	RD25PJ153X	

MAIN P.W.B ASSY PARTS LIST(cont'd)

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SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
R146	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R147	180 OHM 1/2W 5% CARBON FILM	RD50TJ181X	
R148	180 OHM 1/2W 5% CARBON FILM	RD50TJ181X	
R149	56K 1/4W 5% CARBON FILM	RD25PJ563X	
R150	470 OHM 1/4W 5% CARBON FILM	RD25PJ471X	
R151	33K 1/4W 5% CARBON FILM	RD25PJ333X	
R152	10K 1/4W 5% CARBON FILM	RD25PJ103X	
R153	33K 1/4W 5% CARBON FILM	RD25PJ333X	
C1	0.047uF 12V CERMIC CAPACITOR	CBD1B473Mu	
↓		↓	
C4	0.047uF 12V CERMIC CAPACITOR	CBD1B473Mu	
C5	1uF 10V TANTALUM CAPACITOR	CS5C010MDC	
↓		↓	
C8	1uF 10V TANTALUM CAPACITOR	CS5C010MDC	
C9	0.1uF 12V CERMIC CAPACITOR	CBG1B104MM	
C10	0.1uF 12V CERMIC CAPACITOR	CBG1B104MM	
C11	0.1uF 12V CERMIC CAPACITOR	CBG1B104MM	
C12	0.047uF 12V CERMIC CAPACITOR	CBD1B473Mu	
↓		↓	
C16	0.047uF 12V CERMIC CAPACITOR	CBD1B473Mu	
C17	20pF 50V CERMIC CAPACITOR	CCGB200KCT	
C18	20pF 50V CERMIC CAPACITOR	CCGB200KCT	
C19	0.047uF 12V CERMIC CAPACITOR	CBD1B473Mu	
C20	500pF 50V CERMIC CAPACITOR	CCGB501kCT	
C21	500pF 50V CERMIC CAPACITOR	CCGB501KCT	
C22	500pF 50V CERMIC CAPACITOR	CCGB501KCT	
C23	500pF 50V CERMIC CAPACITOR	CCGB501KCT	
↓		↓	
C27	500pF 50V CERMIC CAPACITOR	CCGB501KCT	
C28	0.047uF 12V CERMIC CAPACITOR	CBD1B473Mu	
C29	10pF 50V CERMIC CAPACITOR	CCGB100DCT	
C30	10pF 50V CERMIC CAPACITOR	CCGB100DCT	
C31	0.047uF 12V CERMIC CAPACITOR	CBD1B473Mu	
↓		↓	
C35	0.047uF 12V CERMIC CAPACITOR	CBD1B473Mu	
C36	0.1uF 12V CERMIC CAPACITOR	CBG1B104MM	
C37	0.1uF 12V CERMIC CAPACITOR	CBG1B104MM	

MAIN P.W.B ASSY PARTS LIST(cont'd)

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SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
C38	100pF 50V CERMIC CAPACITOR	CCGB101JLT	
C39	0.047uF 12V CAPACITOR	CBD1B473Mu	
C40	0.0047uF 50V 5% MYLAR CAPACITOR	CQMB472JTH	
C41	3300pF 50V 10% MYLAR CAPACITOR	CQMB332JTH	
↓	↓	↓	
C46	3300pF 50V 10% MYLAR CAPACITOR	CQMB332JTH	
C47	0.1uF 12V CERMIC CAPACITOR	CBG1B104MM	
C48	0.1uF 12V CERMIC CAPACITOR	CBG1B104MM	
C49	10uF 16V ELYT CAPACITOR	CEVD100ADN	
C50	10uF 16V ELYT CAPACITOR	CEVD100ADN	
C51	0.047uF 12V CERMIC CAPACITOR	CBD1B473Mu	
C52	1uF 50V N.P ELYT CAPACITOR	CEAD010NLN	
C53	0.1uF 12V CERMIC CAPACITOR	CBG1B104MM	
C54	10uF 16V ELYT CAPACITOR	CEVD100ADN	
C55	10uF 16V ELYT CAPACITOR	CEVD100ADN	
C56	0.1uF 12V CERMIC CAPACITOR	CBG1B104MM	
C57	0.1uF 12V CERMIC CAPACITOR	CBG1B104MM	
C58	0.1uF 12V CERMIC CAPACITOR	CBG1B104MM	
C59	3300pF 50V 10% MYLAR CAPACITOR	CQMB332JTH	
C60	3300pF 50V 10% MYLAR CAPACITOR	CQMB332JTH	
C61	0.0047uF 50V 5% MYLAR CAPACITOR	CQMB472JTH	
C62	0.01uF 25V 20% CERMIC CAPACITOR	CBD1E103MM	
C63	0.1uF 50V 10% MYLAR CAPACITOR	CQMB104KTH	
C64	0.047uF 50V 10% MYLAR CAPACITOR	CQMB473KTH	
C65	0.047uF 12V CERMIC CAPACITOR	CBD1B473Mu	
C66	0.047uF 12V CERMIC CAPACITOR	CBD1B473Mu	
C67	0.047uF 12V CERMIC CAPACITOR	CBD1B473Mu	
C68	1000pF 50V CERMIC CAPACITOR	CKGB102KBT	
C69	1000pF 50V CERMIC CAPACITOR	CKGB102KBT	
C70	0.1uF 12V CERMIC CAPACITOR	CBG1B104MM	
C71	0.039uF 50V 10% MYLAR CAPACITOR	CQMB393KTH	
C72	0.039uF 50V 10% MYLAR CAPACITOR	CQMB393KTH	
C73	0.039uF 50V 10% MYLAR CAPACITOR	CQMB393KTH	
C74	0.047uF 12V CERMIC CAPACITOR	CBD1B473Mu	
C75	47uF 16V N.P ELYT CAPACITOR	CEAD470NLX	
C76	47uF 16V N.P ELYT CAPACITOR	CEAD470NLX	
C77	47uF 16V N.P ELYT CAPACITOR	CEAD470NLX	
C78	3.3uF 50V ELYT CAPACITOR	CEVG3R3ALN	

MAIN P.W.B ASSY PARTS LIST(cont'd)

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SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
C79	0.047uF 12V CERMIC CAPACITOR	CBD1B473Mu	
C80	0.047uF 12V CERMIC CAPACITOR	CBD1B473Mu	
C81	1000pF 50V CERMIC CAPACITOR	CKGB102KBT	
C82	4.7uF 25V ELYT CAPACITOR	CEVE4R7ADN	
C83	470uF 10V ELYT CAPACITOR	CEAC471ACX	
C84	470uF 6.3V ELYT CAPACITOR	CEAB471ACX	
C85	4.7uF 35V ELYT CAPACITOR	CEAF4R7ACX	
C86	3.3uF 50V ELYT CAPACITOR	CEVG3R3ALN	
C87	0.1uF 12V CERMIC CAPACITOR	CBG1B104MM	
C88	500pF 50V CERMIC CAPACITOR	CCGB501KCT	
C89	500pF 50V CERMIC CAPACITOR	CCGB501KCT	
C90	1uF 50V ELYT CAPACITOR	CEVG010ADN	
C91	0.047uF 12V CERMIC CAPACITOR	CBD1B473Mu	
C92	0.47uF 50V ELYT CAPACITOR	CEVGR47ADN	
C93	100pF 50V 10% MICA CAPACITOR	CMDA101KXB	
C94	0.0047uF 25V CERMIC CAPACITOR	CBD1E472MM	
C95	0.1uF 250V 20% POLYESTER CAPACITOR	CQHD104MEN	
C96	0.1uF 250V 20% POLYESTER CAPACITOR	CQHD104MEN	
C97	1000pF 50V 10% CERMIC CAPACITOR	CKGB102KBT	
C98	1000pF 50V 10% CERMIC CAPACITOR	CKGB102KBT	
C99	0.1uF 12V CERMIC CAPACITOR	CBG1B104MM	
C100	2200pF 50V 10% CERMIC CAPACITOR	CBD1H222KM	
C101	1uF 10V TANTALUM CAPACITOR	CSSC010MDC	
SW1	SSP32201 SLIDE SWITCH	SS020259ZA	
SW2	SSB34204 SLIDE SWITCH	SS040213ZA	
SW3	SKM 22-03 SLIDE SWITCH	SS020260ZL	
SW4	SPJ312U PUSH SWITCH	SP01ABA06A	
SW5	SSP32201 SLIDE SWITCH	SS020259ZA	
CN1	5268-10A x2 CONNECTOR	YJF10S050Z	
CN2	A-7224 CONNECTOR	YJF09S039Z	
CN3	TCS4480 CONNECTOR	YJF08S033Z	
CN4	TCS4490 CONNECTOR	YJF08S034Z	
CN5	FRC2-C26-L13-ON CONNECTOR	YJF26S010Z	
CN6	DB-25S CONNECTOR	YJF25S007Z	

MAIN P.W.B ASSY PARTS LIST(cont'd)

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SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
CN7	HU-30P-2G-L13	YJF30S006Z	
	3-51FT Ni-cd BATTERY	ZBN036102Y	
	HEC0342-01-010 JACK	YJB03S001Z	
	A-8878A-28S-1H IC SOCKET	YSC28S002Z	
	IC SOCKET		
	IC SOCKET		
	IC SOCKET		
	BATTERY TERMINAL(A)	MW361SN001	
	BATTERY TERMINAL(B)	MW361SN002	
	BATTERY SUPPORT	VS118SB001	

SECTION IV
LCD P.W. BOARD

TECHNICAL DESCRIPTION

The technical description of the Model 100 LCD PWB is divided into the following 3 sections.

1. LCD PANNEL
2. LCD CONTROL CIRCUIT
3. LCD WAVE FORM

1. LCD PANEL

Liquid crystal is a substance midway between a liquid and a solid, although its appearance is much like a liquid. From an electrical and optical stand point, it possesses the properties of a crystal. Items which use this liquid crystal are liquid crystal display elements. The LCD used in Model 100 is a TN (Twisted Nematic) type of liquid crystal. Its basic construction is shown in Fig. 1.

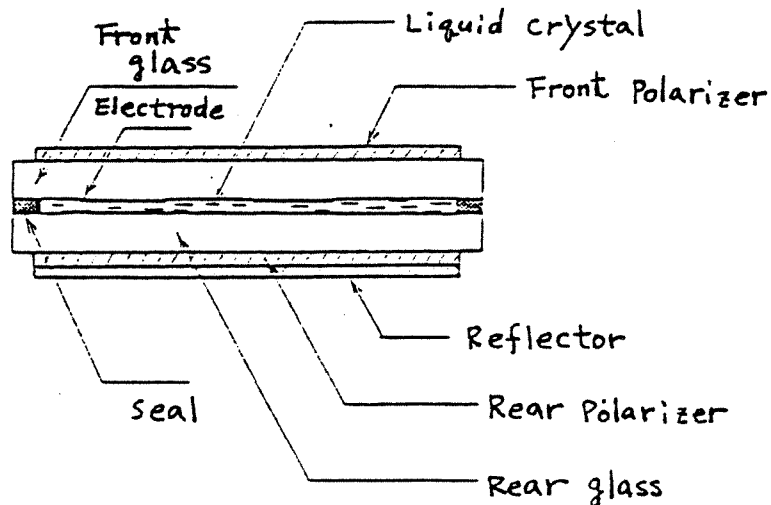


Fig. 1

The principle by which it functions can be briefly expressed as "an electric shutter with relation to light". In other words, if voltage is applied, the transmission of light is blocked, and, if voltage is not

applied, light is passed, so that letters and numbers are displayed.

The operation theory is shown in Fig. 2.

- (1) The optical activity (twisting) of light is used, and the liquid-crystal display element is sandwiched between the two polarization plates. The polarized axes of the upper and lower plates are placed at right angles to each other.
- (2) As shown in Fig. 2 (a), if voltage is not applied, the liquid-crystal molecules between the upper and lower plates twist 90° to distribute light. This results in a 90° optical movement of the light.
- (3) In other words, when voltage is not applied, light is transmitted, and when voltage is applied, light is interrupted.

(a) when voltage is OFF (b) when voltage is ON

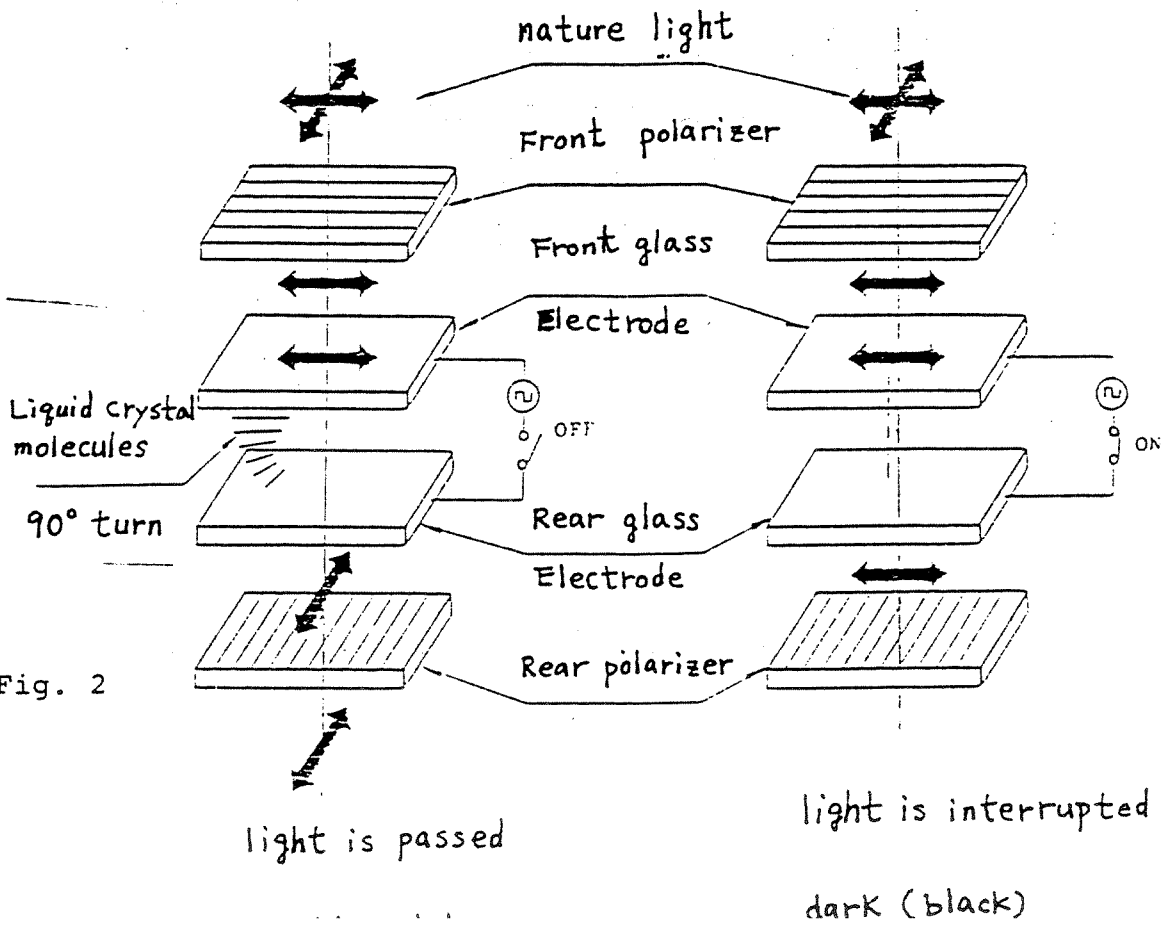


Fig. 2

The LCD used in Model 100 is composed of electrodes in a matrix arrangement (back scan 64, segments 480). Refer to Fig. 3.

Because this LCD operates on a 1/32 duty time-division drive, the upper 32 and lower 32 back scanning is performed by the same signal.

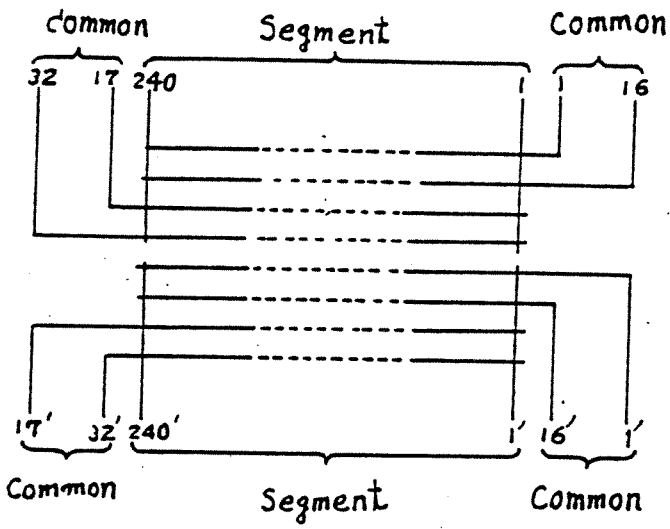
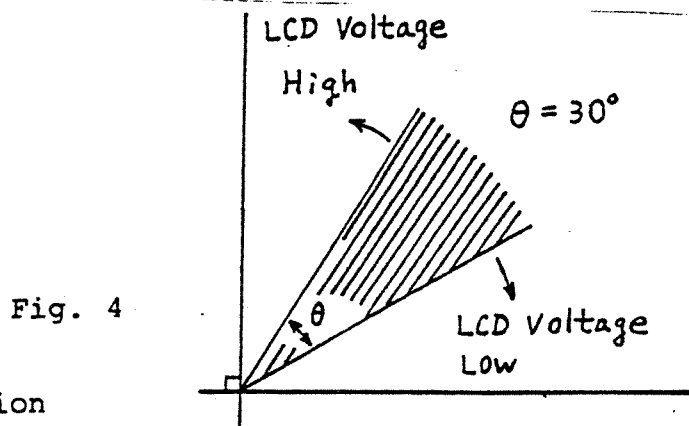


Fig. 3 LCD electrodes

The angle of the field of vision is 30° in the range that contrasts. $K = (\text{brightness of non-illuminated segment}) / (\text{brightness of illuminated segment})$ 1.4 or more.

This range can be set at will from 0° to 90° by setting the LCD drive voltage by using the DISP control.



Caution

The polarization plate attached to the surface of the LCD panel is scratched very easily, and so must be handled with great care.

To clean contacts or the display surface, slightly dampen a soft cloth with benzine and wipe gently. Do not use organic solvents such as alcohol.

2. LCD CONTROL CIRCUIT

Refer to the LCD-PWB circuit diagram while reading this section.

ICs M11 and M12 (HD44103) are back-scan driver ICs. The timing signal necessary for the display is generated by the built-in oscillator and by C5 and R10, and this timing signal is also supplied to the segment driver side for control of the display.

There are 16 HD44103 back-scan signal outputs. M11 and M12 are cascade connected, and a 1/32 duty back-scan signal is made. By using a C and R only at the M11 side, a timing signal is generated, and M12 is controlled by that signal. M11 can then be considered to be the master IC and M12 the slave. The basic oscillation frequency is about 430 kHz.

Fig. 5 shows the internal logic composition.

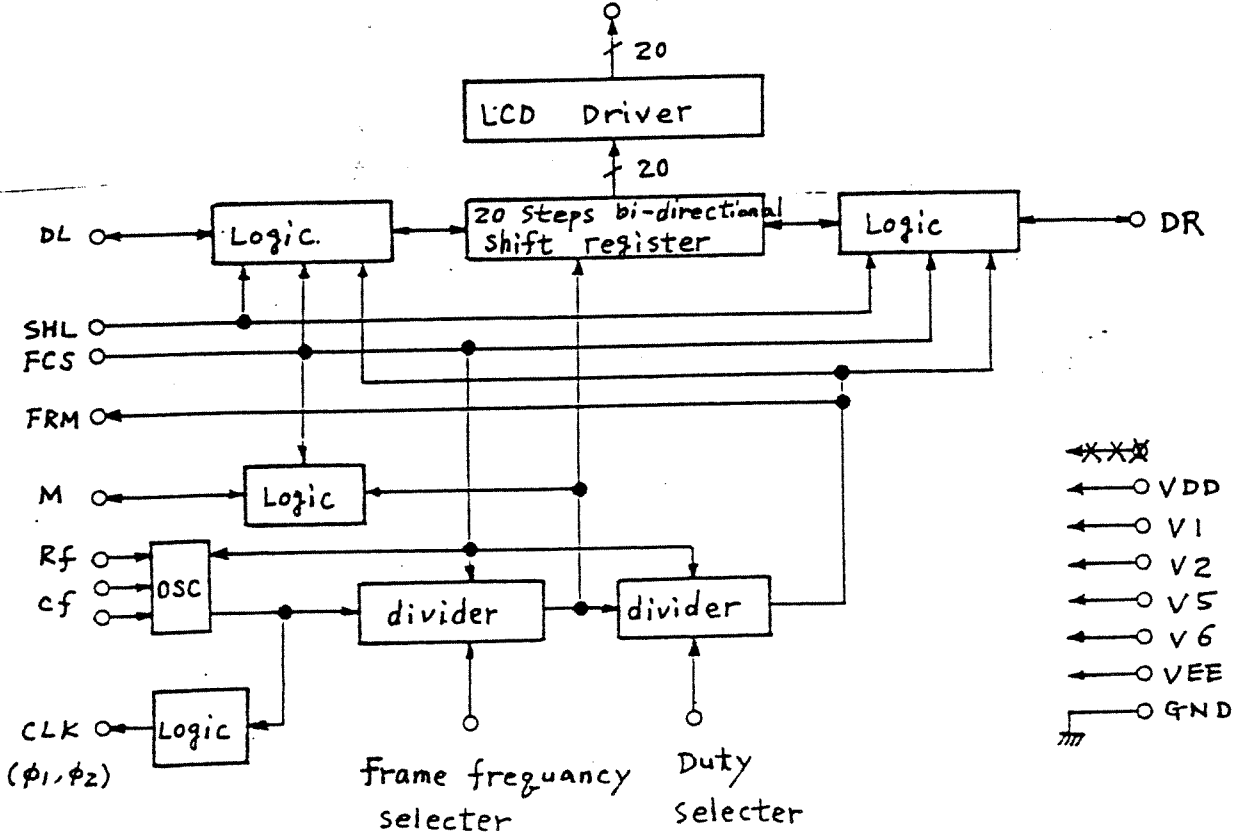


Fig. 5 HD44103 internal logic

The timing signals are M, FRM, O_1 , O_2 and CL. The M signal is the signal which inverts the LCD drive waveform one image at a time to change it to AC.

Because the continuous application of DC to the LCD would shorten the element life, an alternating electric field is applied to the liquid crystal surface during drive in order to make the waveforms symmetrical and make the DC component as small as possible.

The FRM signal is the display repeat frequency, the signal which sets the number of scans per second.

For Model 100, $FRM \cong 70$ Hz.

The O_1 and O_2 signals are the locks for HD44102 RAM operation.

The CL signal is the shift lock for the shift register. ICs M1 - M10 (HD44102) are segment driver ICs that cause the display data sent from the CPU board to be memorized in the built-in RAM and automatically generate the liquid-crystal drive signal.

One bit of data from the built-in RAM corresponds to one dot of illumination or non-illumination on the display.

The driver output is 50.

The transfer of the display data is accomplished by 8-bit parallel data. This IC has several types of commands, and the D/I (H: data, L: command) signal distinguishes between commands and data.

Fig. 6 shows the internal logic composition.

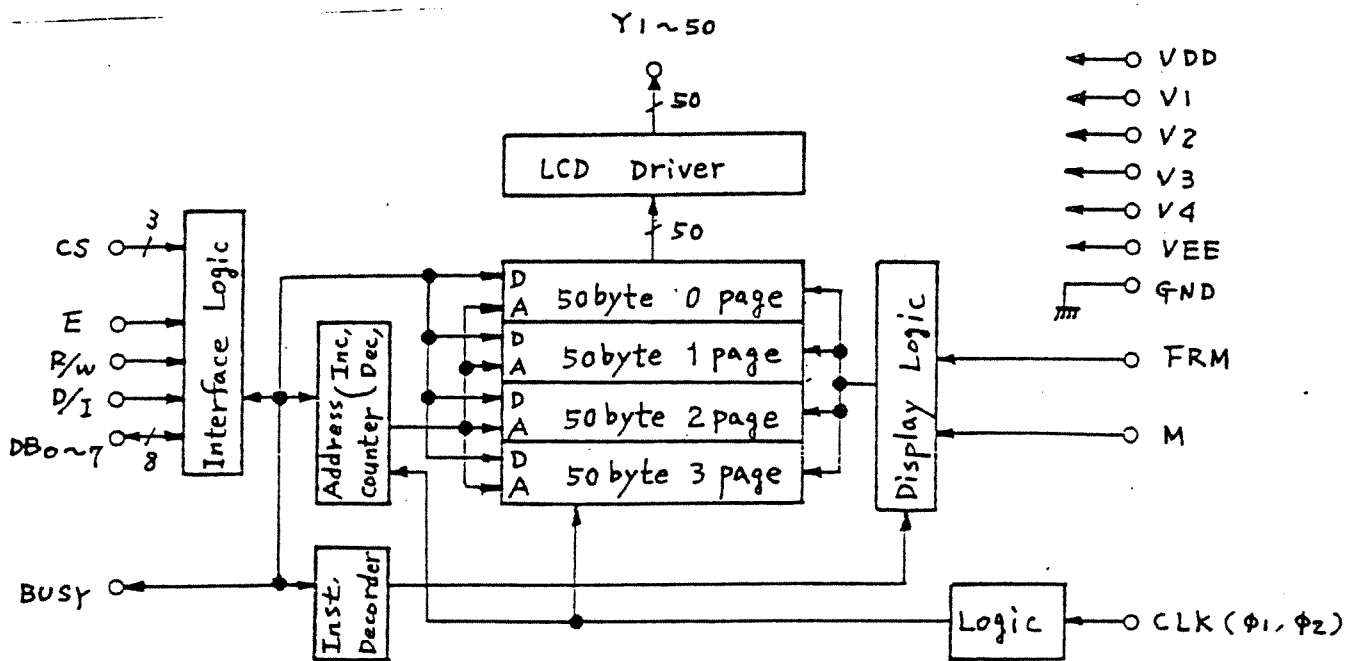


Fig. 6 HD44102 internal logic

Because Model 100 has 240 segments each (upper and lower), the M5 and M10 segment output Y41 - Y50 becomes NOCONNECTION. The power supplied to these ICs, in addition to V_{DD} (+5 V) and V_{EE} (-5 V), also includes V1 - V6.

V_{DD} and V_{EE} are the power supplies which operate the IC logic, and V1 - V6 make the LCD signal.

V1 - V6 are made by the resistance splitting of R1, R2, R3, R4 and R5, and, by passing through operation amplifier M13 (HA17902), lessen the output impedance of the power supply.

C3, C4, C6, C7 and C8 augment the peak current during LCD illumination.

R11, R12 and R13 are resistors for IC latch-up prevention.

This board also includes a low-power detection LED and buzzer connectors.

3. LCD WAVEFORM

In order to drive the liquid-crystal elements by the 1/32 duty line-sequential drive method, the LCD of Model 100 makes sequential selection of the 32 scanning electrodes. For each dot, the display signal passes through the signal electrodes and is applied 32 times for one display. At this point the signal is necessary at each dot only one time, and the signals for the other 31 times correspond to other dots on the same signal electrode.

Because liquid-crystal elements have a cumulative response characteristic (a response characteristic corresponding to the sum total of the effective voltages of the voltage pulses applied for some tens of msec to some hundreds of msec), the voltage applied for 32 times is all applied as effective voltage, so that the content (the ON or OFF contrast) of the dot in question is affected by crosstalk (display information) from other dots on the same display line.

In order to suppress such crosstalk, it is necessary that the voltage applied as effective voltage to the liquid-crystal in question be maintained at a constant level for each dot on the matrix regardless of whether the signals of the other dots (applied 32-1) are ON or OFF, so that a voltage average is realized through a combination of voltage levels when the scanning signal and display signal are selected and not selected.

An appropriate algebraic method for each condition can be used to determine the voltage combinations applied to the element (the voltage averaging method) in order to obtain the maximum display contrast while suppressing crosstalk between the liquid-crystal elements. The combination of the liquid-crystal elements and the combination of the two types of non-applied voltages and the resulting potential difference actually applied to the liquid-crystal are shown in (a) and (b) of table 1.

Signal electrode		Selection	Non-selection
Scanning electrode		0	$2V_0/a$
		Selection V_0	$(1 - 2/a)V_0$
Non-selection V_0/a		$+ V_0/a$	$- V_0/a$

(a)

Signal electrode		Selection	Non-selection
Scanning electrode		V_0	$(1 - 2/a)V_0$
		Selection 0	$- (1 - 2/a)V_0$
Non-selection $(1-1/a)V_0$		$- V_0/a$	$+ V_0/a$

(b)

Table 1: Liquid-crystal voltages and voltages applied to each electrode by the voltage averaging method

As can be understood by studying Table 1, the voltages applied to the liquid-crystal (32-1 time for non-selection) are averaged to $\pm V_0/a$ regardless of whether the signal voltage is selected (other segments are ON) or not selected (other segments are OFF).

In addition, the waveform is inverted, resulting in alternating drive, by alternating the (a) and (b) applied voltages.

Here V_0 represents the maximum voltage applied to the scanning electrode and signal electrode, and, for Model 100, is the potential difference between V_1 and V_2 .

In addition, a is the bias coefficient which determines, from the stand point of contrast, the maximum ratio between the illumination voltage and the non-illumination voltage.

When that ratio is greatest in relation to the effective ON and OFF voltages, $a = 6.66$.

Thus, for V_1 , V_2 , V_3 , V_4 , V_5 and V_6 :

$$V_1 =$$

$$V_2 = V$$

$$V_3 = 2/aV$$

$$V_4 = (1 - 2/a)V$$

$$V_5 = (1 - 1/a)V$$

$$V_6 = a/aV$$

The following figures show the drive waveform for illumination and non-illumination.

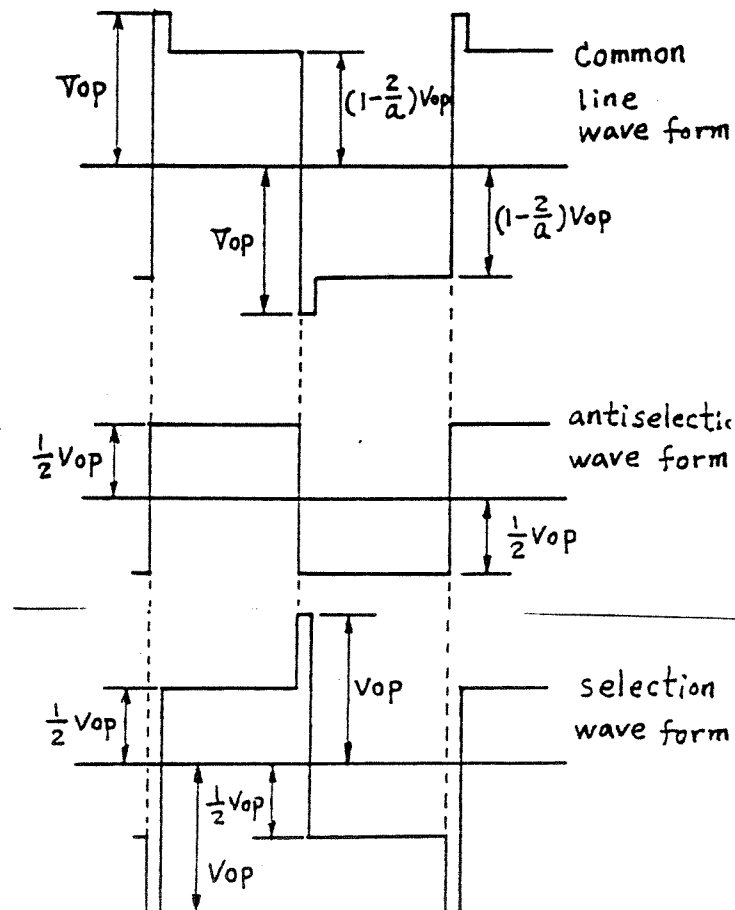


Fig 7

LCD P.W.B ASSY PASRTS LIST(cont'd)

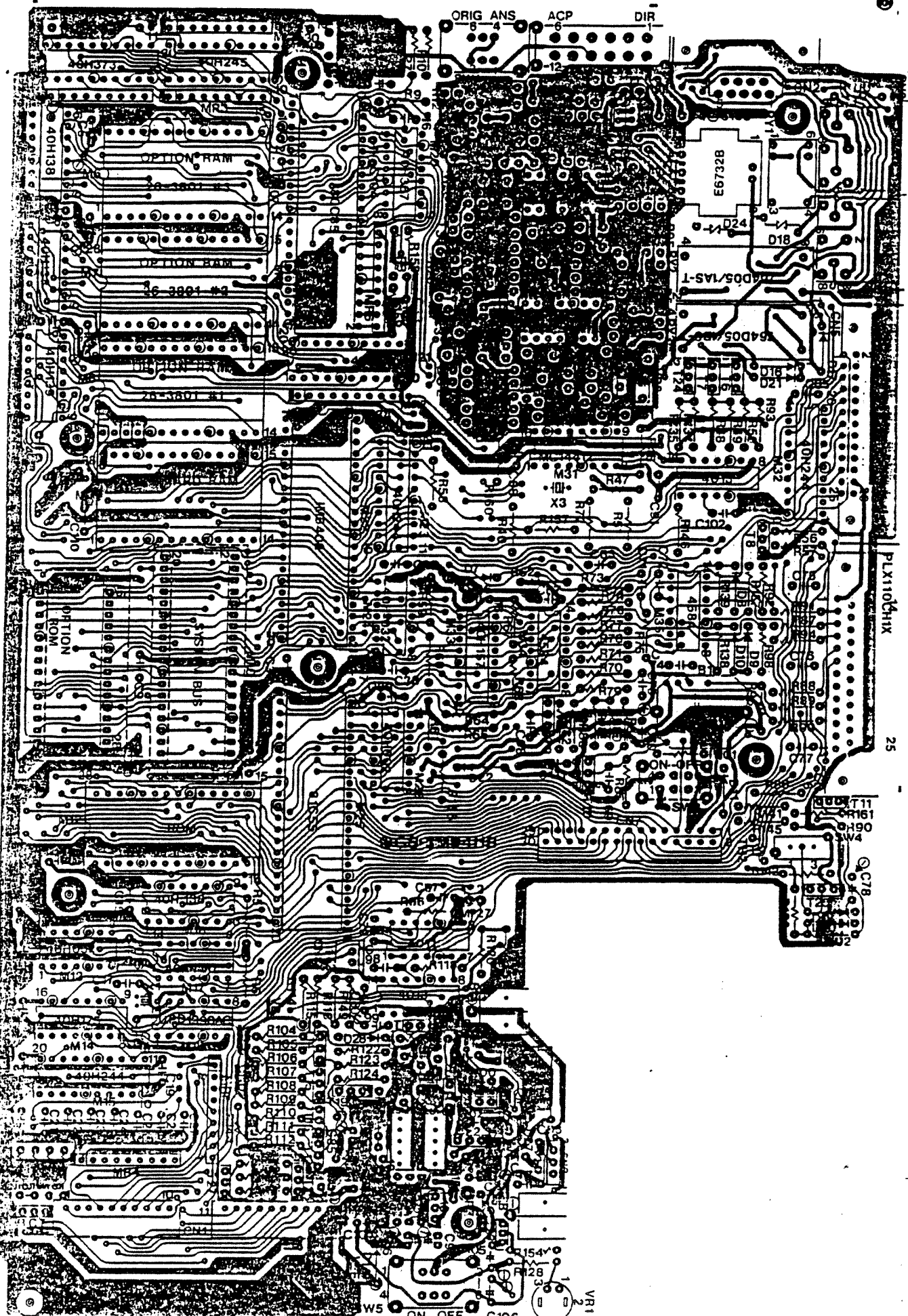
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SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
M1	HD44102B L.C.D DRIVER IC	QQ044102AB	
	↓	↓	
M10	HD44102B L.C.D DRIVER IC	QQ044102AB	
M11	HD44103B L.C.D DRIVER IC	QQ044103AB	
M12	HD44103B L.C.D DRIVER IC	QQ044103AB	
M13	HA17902P O.P AMP	QQM17902PB	
R1	10K 1/8W 2% CHIP RESISTOR	RJ8AMG1002	
R2	10K 1/8W 2% CHIP RESISTOR	RJ8AMG1002	
R3	26.5K 1/8W 2% CHIP RESISTOR	RJ8AMG2652	
R4	10K 1/8W 2% CHIP RESISTOR	RJ8AMG1002	
R5	10K 1/8W 2% CHIP RESISTOR	RJ8AMG1002	
R6	100K 1/8W 5% CHIP RESISTOR	RJ8AMJ104X	
	↓	↓	
R10	100K 1/8W 5% CHIP RESISTOR	RJ8AMJ104X	
R11	220 OHM 1/8W 5% CHIP RESISTOR	RJ8AMJ221X	
R12	220 OHM 1/8W 5% CHIP RESISTOR	RJ8AMJ221X	
R13	100 OHM 1/4W 5% CARBON FILM	RD25TJ101X	
C1	0.1uF 25V CHIP CAPACITOR	CFFC104ZFX	
	↓	↓	
C4	0.1uF 25V CHIP CAPACITOR	CFFC104ZFX	
C5	18pF 25V CHIP CAPACITOR	CCFC180MCX	
C6	0.1uF 25V CHIP CAPACITOR	CFFC104ZFX	
	↓	↓	
C10	0.1uF 25V CHIP CAPACITOR	CFFC104ZFX	
	LR202-C L.C.D	ZXLR202CXB	
	L.C.D CONNECTOR	VQ811RX001	
	L.C.D HOLDER	MB861SF001	
	SLP-135B L.E.D	QL1SP135BC	
	CONNECTOR ASSY	ACCN812GEA	
	5267-02A CONNECTOR	YJF02S054Z	
	BUZZER KBS-27DB-3AU	ZYED100005	
	HOUSING 5264-02	YJF02S057Z	
	CONN TERMINAL5263-BT	YTP01S002Z	

SECTION VII

DIAGRAMS

ORIG ANS ACP DIR
6 4 6 12



PLX110CH1X

25

T11
R191
R190
W4

C78

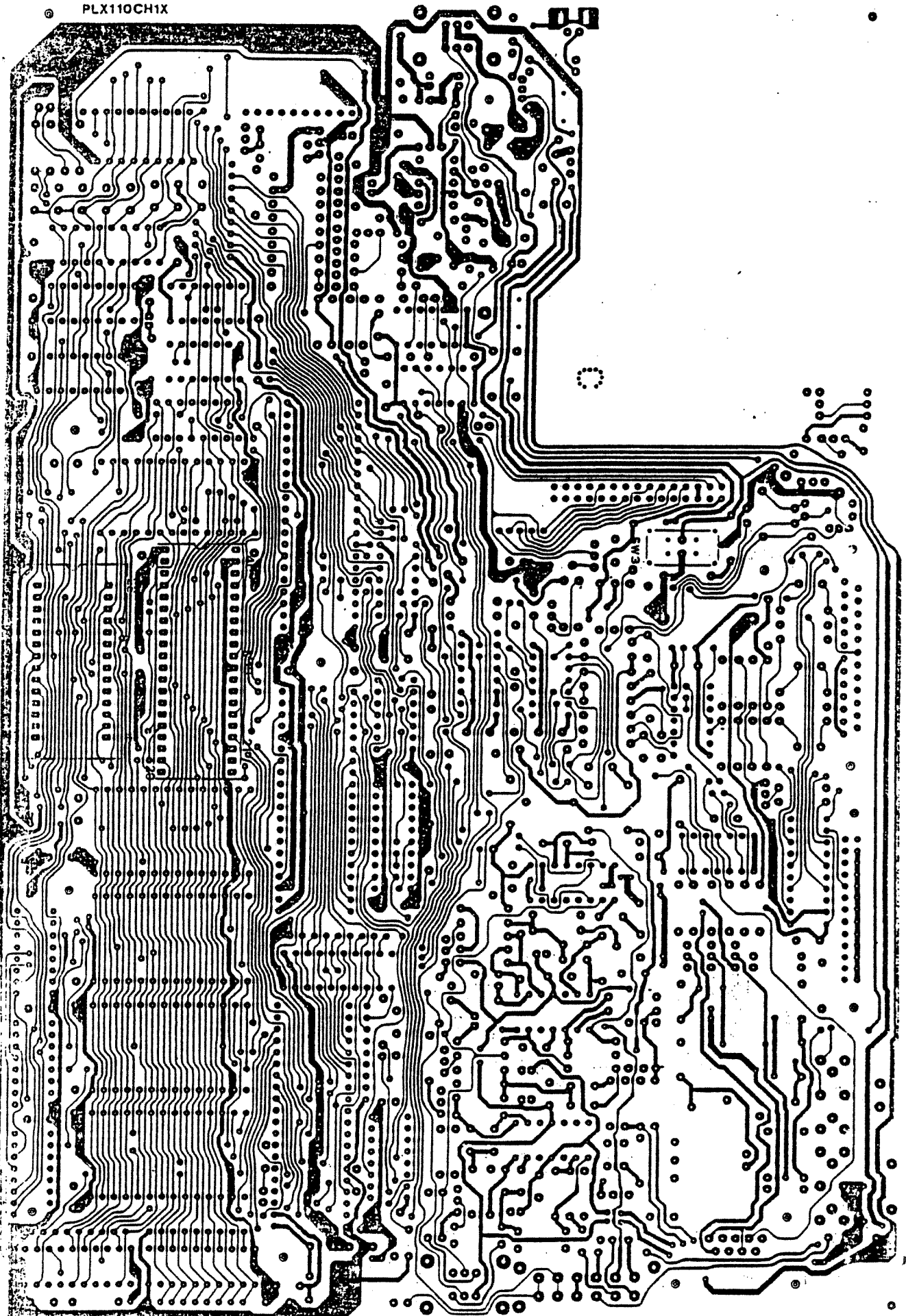
R104
R105
R106
R107
R108
R109
R110
R111
R112

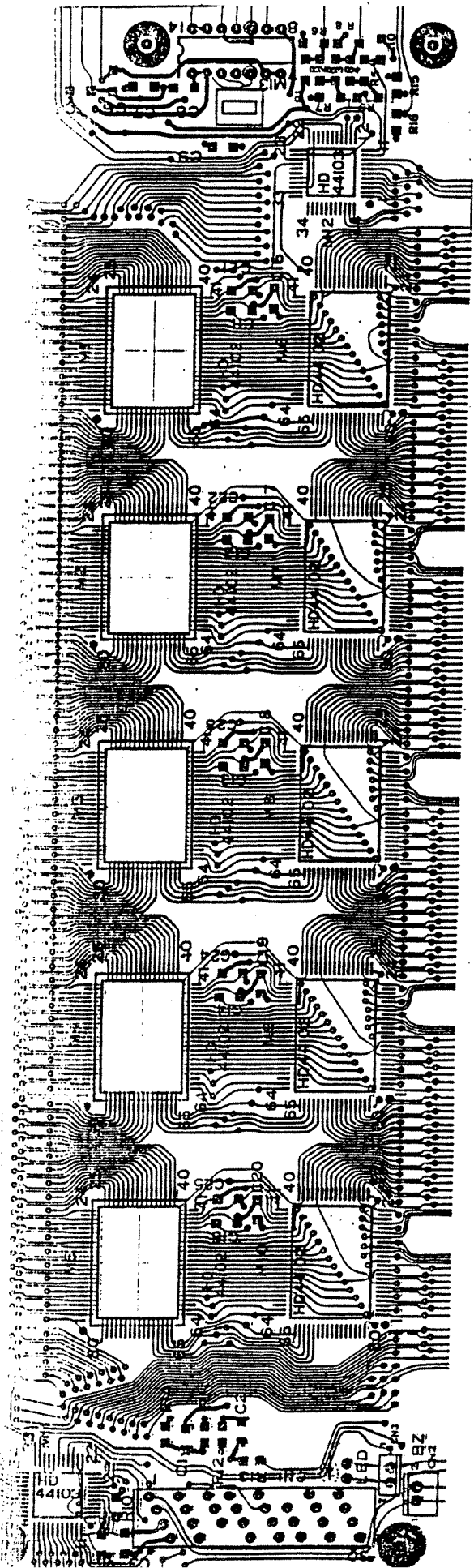
D28
R122
R123
R124

154V
R126
C106
ON OFF
VR1

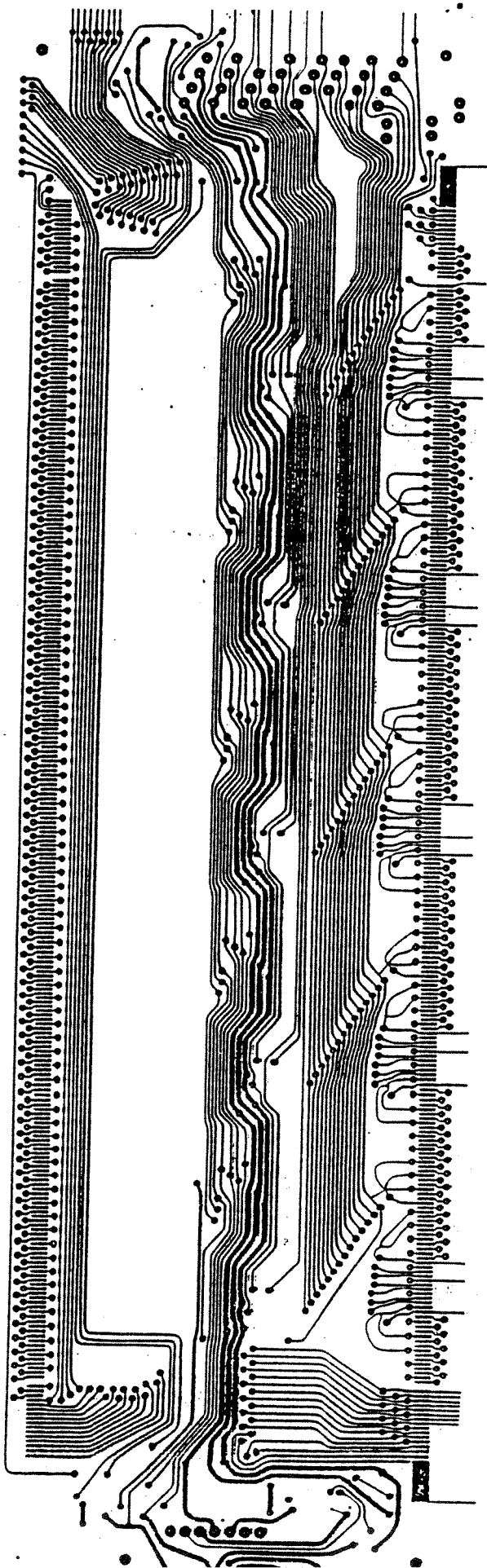
100-100000

PLX110CH1X





LSI SIDE





M25 (State New) Functions

1. e s To LED LIVES
 2. CLK TO UNIT
 3. DATA PROCESSOR
 4. PROGRAMS ARE OK
 5. AND SPURIOUS TRUNC-
 6. BURNS BURGER
- (NOTE THIS ARE NOT KNOWLEDGE OF GROUP
PUT THIS OTHER UNIT DOWN)
7. STORIES TO LIVE

NOT THAT YOU CAN SEE THE LIGHT

NOTE STORIES OF THE OTHER LEVER
DO/AND FOR THE ONE OF THE
PLEASE USE FEEDBACK

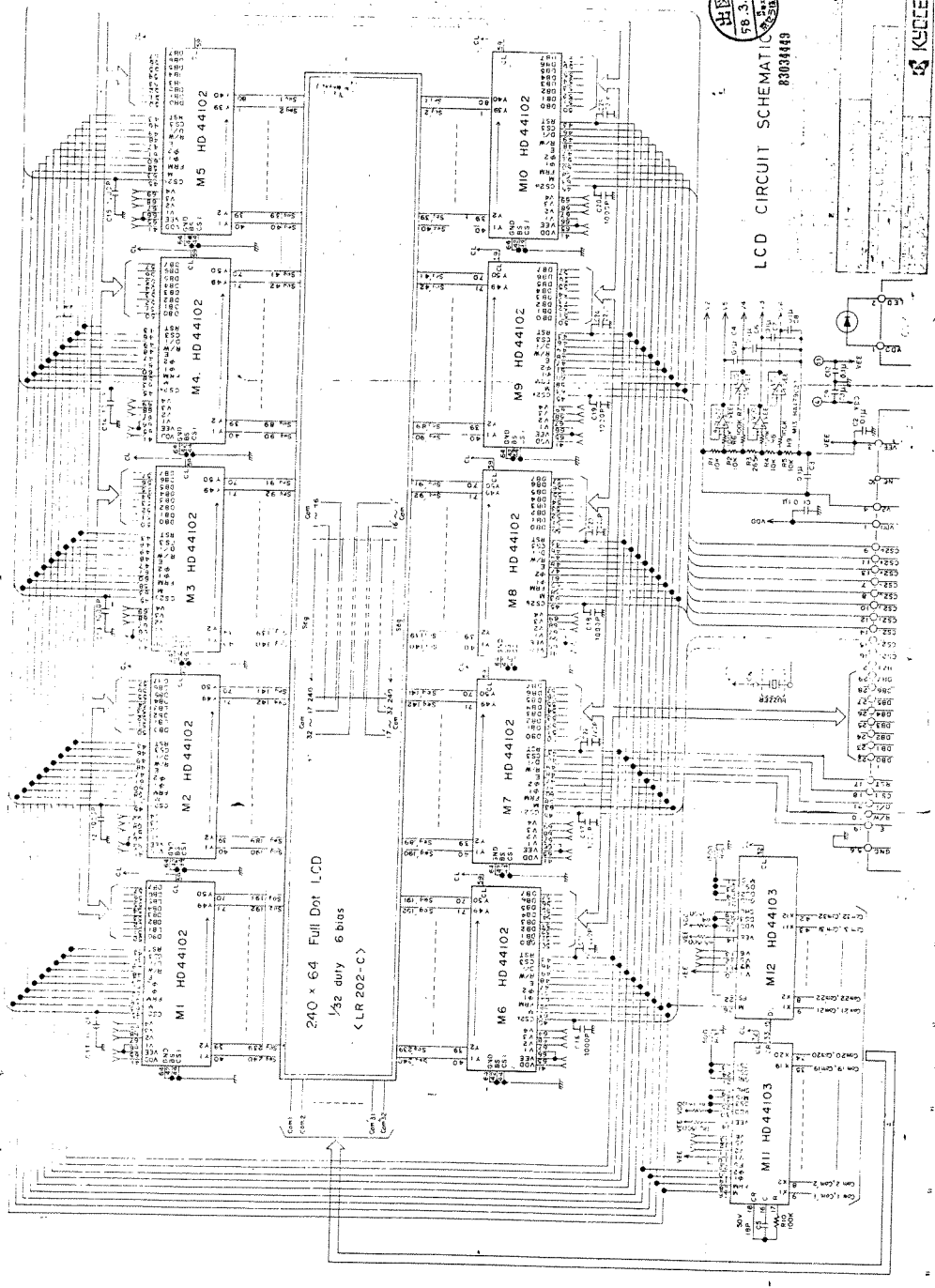
PLEASE READ THE UNIT

PLEASE OBSERVE THE STATE UNIT



LCD CIRCUIT SCHEMATIC
8303443

KUCC103







Model 100
Preliminary Diagnostics



MEMORY DIAGNOSTICS

Description

Model 100 Memory Diagnostics consists of two machine level programs and is designed to test the ROM and RAM of the TRS-80 Model 100 Portable Computer.

Quick Reference

IMPORTANT NOTE: ALL USER FILES WILL BE DELETED FROM THE MODEL 100 MEMORY BY THE USE OF THESE PROGRAMS. IF THERE ARE ANY FILES THAT YOU WISH TO RETAIN, SAVE THEM FIRST !!!!!.

- 1) Prepare cassette player and cassette tape
- 2) Power up the Model 100
- 3) At the Model 100 power-up menu type 'BASIC <ENTER>' OR position the cursor over the word 'BASIC' and press <ENTER>
- 4) In BASIC type 'POWER CONT <ENTER>'
- 5) Type 'CLEAR 200, 60000 <ENTER>'
- 6) Type 'CLOADM "MEMLO" <ENTER>'
- 7) Once the program loads without error, type 'CALL 61440 <ENTER>'
- 8) At the Model 100 Memory Diagnostics title page, press any key
- 9) The menu will then appear on the display; Type '1' to execute the ROM CRC Check or type '2' to execute the RAM Check
- 10) For the ROM CRC Check, the current CRC is A2D4
New checksums can be listed here: _____
- 11) After completing the tests, press <CTRL><BREAK> and the reset switch simultaneously
- 12) Repeat steps 3-11 above using the following changes for steps 5, 6 and 7:
 - 5) Type 'CLEAR 200, 59000 <ENTER>'
 - 6) Type 'CLOADM "MEMHI" <ENTER>'
 - 7) Once the program loads without error, type 'CALL 59136 <ENTER>'



The Programs

Model 100 Memory Diagnostics consists of two programs called MEMLO and MEMHI. The only functional difference between the programs is the area of RAM which they test. The only visible difference is in the version numbers; MEMLO is version 1.0.0 LO and MEMHI is version 1.0.0 HI. MEMLO checks RAM beginning at the first available RAM location and ending at EFFF hex. MEMHI checks RAM beginning at EB76 hex and ending at F5F0 hex. Note that F5F1 hex through FFFF hex is not checked under this software.

The following directions apply to either program, except where specified.

IMPORTANT NOTE: ALL USER FILES WILL BE DELETED FROM THE MODEL 100 MEMORY BY THE USE OF THESE PROGRAMS. IF THERE ARE ANY FILES THAT YOU WISH TO RETAIN, SAVE THEM FIRST !!!!!.

Loading and Executing

- 1) Prepare cassette player and cassette tape
- 2) Power up the Model 100
- 3) At the Model 100 power-up menu type 'BASIC <ENTER>' OR position the cursor over the word 'BASIC' and press <ENTER>
- 4) In BASIC type 'POWER CONT <ENTER>'
- 5) Type 'CLEAR 200, 59000 <ENTER>'
- 6) Type 'CLOADM "MEMLO" <ENTER>' to load MEMLO or type 'CLOADM "MEMHI" <ENTER>' to load MEMHI
- 7) Once the program loads without error, type 'CALL 61440 <ENTER>' to execute MEMLO or type 'CALL 59136 <ENTER>' to execute MEMHI

The Menu

After executing the program program, the screen will display the program name, the program version number, the copyright date, and the amount of RAM available to the system. To proceed to the menu, press any key. At this point press '1' to perform the ROM CRC Check or press '2' to perform the RAM Check. You can exit the program at any time by pressing <CTRL><BREAK> and the reset switch simultaneously.



ROM CRC Check

After pressing the '1' key at the menu, the program will display 'CRC =' and pause for a few seconds before displaying the ROM CRC. Once the test is complete, press any key to return to the menu.

The CRC generated by this test is a simple 16 bit sum of all the bytes of ROM (from 0000 hex through 7FFF hex).

The current ROM CRC value is A2D4

New Checksums can be listed here: _____

RAM Check

After selecting option '2' from the menu, the program will clear the screen and display the RAM test as they are executed. There are three tests that are performed, the first of which is the 00 Fill. This test fills the section of RAM being tested with zeros and then read the RAM to make sure that the zeros were written. The second test is the FF Fill and operates in the same manner, except that it uses FF hex to fill memory instead of zero.

The last test is the Rotating fill. This tests fills RAM with a sequential pattern from 01-FF hex until all RAM that is being tested is filled and the checks to see that the same sequence is read back from the RAM. It makes 255 passes, each pass beginning the sequence with a different value. (The first pass will begin the sequence with 1,2,3,4,5...; The second pass will begin the sequence with 2,3,4,5,6..., etc.).

The following table shows the amount of time that each RAM Check will take for each RAM size available for Model 100.

<u>Program</u>	<u>8K</u>	<u>16K</u>	<u>24K</u>	<u>32K</u>
MEMLO	2.1 min.	4.2 min.	6.3 min.	9.4 min.
MEMHI	3 min.	3 min.	3 min.	3 min.

All times are approximate



MODEL 100 BASIC Test

Overview

The Model 100 BASIC test program is an automated test that automatically test each subsection of the machine except for the expansion buss and the RAM. Use the MEMLO and MEMHI programs for RAM test. Most of the test are in BASIC and are simple to modify or to write into another test program for exersizing a specific area of the machine. Some of the test are machine code routines that are called from the BASIC program.

Loading

Turn on the power to the Model 100 and make sure the standard menu is displayed. BASIC should be in the top left corner of the menu. Use the arrow keys to insure the the cursor is positioned over the word BASIC and hit the <ENTER> key.

If the main menu is NOT displayed, try pressing <F8>. This should return you to the menu. If not, you may have to press <RESET> on the back panel of the machine.

Once in BASIC, prepare the MODEL 100 TEST TAPE and a tape recorder. Type CLOAD<ENTER> and the program should begin loading. If the machine finds the program, it will display:

```
Found:TEST  
OK
```

DO NOT REMOVE THE CASSETTE FROM THE PLAYER. If there were any errors, try adjusting the volume control.

After loading successfully, type RUN<ENTER>. The program will then load the machine code routines from the cassette. At the completion of loading, a menu will appear and the cassette may now be removed.



Running the test

The menu will look like the following:

1-ALL	5-SOUND TEST
2-CHECK SUM	6-RS232C TEST
3-LCD TEST	7-PRINTER TEST
4-CLOCK TEST	8-BAR CODE READER

0-ABORT (RETURN TO BASIC)

Hitting the <1> key will cause all the test to executed sequentially. As a general rule, hitting the <SPACE BAR> will exit most test and continue with the next test in the AUTO mode.

If you do not have all the equipment necessary for an AUTO test, you may want to run the tests individually.

CHECK SUM #2

This test does a quick check sum of the ROM. If in doubt, or if there is a ROM revision, use the check sum test on the MEMHI / MEMLO tape.

LCD TEST #3

This test puts patterns into the LCD display memory. This just verifies that every dot can be turned on. If in doubt, try directly addressing a point on the screen with your own BASIC program.

CLOCK TEST #4

Displays the time and beeps every second. Hit the <SPACE BAR> to exit

SOUND TEST #5

This test produces notes in an ascending scale and then a descending scale on the buzzer.

RS232C TEST #6

This checks the RS232C port by looping at 19200, 9600, and 75 Baud. The loopback connector must be installed. If there is no RTS-CTS loop, the test will halt, the buzzer will sound, and a message: RTS-CTS NG! Will be displayed. If there is a DATA error, The baud rate at which the test failed will be displayed. Hit the <SPACE BAR> to exit.

The loopback connector is a DB-25 connector with pins 2-3 connected (the data) and pins 4-5 connected (RTS-CTS)



PRINTER TEST #7

This sends a stream of characters to the printer. Printer must be ONLINE and READY.

BAR CODE READER #8

This test displays number patterns that the bar code reader is being swept over properly. Make sure that the wand is moved smoothly over the pattern and check the number displayed with what the pattern should be.

