PRELIMINARY

WD1002-WX2 Winchester Disk Controller

FEATURES

- IBM XT WINCHESTER CONTROLLER EMULATION, IBM PC HOST INTERFACE
- BUILT-IN DATA SEPARATOR, WRITE PRECOMPENSATION LOGIC
- DATA RATES UP TO 5 MBITS/SEC
- CONTROLS UP TO 2 DRIVES USING SEAGATE TECHNOLOGY ST506
- SUPPORTS DRIVES OF ANY CONFIGURATION UP TO 1024 CYLINDERS AND 8 R/W HEADS
- THE CONTROLLED DRIVES NEED NOT BE OF THE SAME CAPACITY OR CONFIGURATION
- ERROR CORRECTION ON DATA FIELD ERRORS, CRC ID FIELD VERIFICATION
- 32 BIT ECC POLYNOMIAL FOR ERROR DETECTION AND CORRECTION
- DIAGNOSTIC READS AND WRITES FOR CHECKING ERROR CORRECTION
- SELECTABLE AUTOMATIC RETRIES ON ALL ERRORS
- AUTOMATIC RESTORE AND RE-SEEK ON ALL SEEK ERRORS
- AUTOMATIC FORMATTING
- 512 BYTES PER SECTOR
- SECTOR INTERLEAVE CAPABILITY
- MULTIPLE SECTOR READS AND WRITES
- OVERLAPPED SEEK CAPABILITY ON BUFFERED-STEP DRIVES
- SUPPORTS IMPLIED SEEKS ON ALL COMMANDS
- INTERNAL DIAGNOSTICS
- DMA TRANSFER CAPABILITY
- SUPPORTS INTERRUPTS, INTERRUPT REQUESTS, AND DMA REQUEST SHARING
- INCLUDES SOCKET FOR USER SUPPLIED 2716, 2732, OR 2764 ROM
- BIOS AVAILABLE

DESCRIPTION

The WD1002-WX2 Winchester Controller is an IBM XT compatible Winchester Controller board designed to interface up to two drives. The drive interface is based upon the Seagate Technology ST506 interface. The drives need not be of the same capacity or configuration. All necessary receivers and drivers are included on the board to allow direct connection to the drive(s).

The WD1002-WX2 interfaces directly with the Host I/O bus via several interface buses. Data transfer to or from the Controller can be either programmed I/O or DMA.

ARCHITECTURE

The WD1002-WX2 is based on the WD1010-05 Winchester Controller/Formatter, the WD1015-14 Control Processor, the WD1100-13 ECC Support Device, and on-board data separation and Write Precompensation circuitry (Figure 1).

The WD1002-WX2 has four on-board interface connectors (there is a factory test connector and burn-in connector on the board that should not be used). The four connectors consist of the following: a 62-pin card edge connector (P1) for interface with the Host (pins A1 thru A31 are on the component side of the board and pins B1 thru B31 are on the conductor side of the board), a 34-pin drive control connector (J1) allowing up to two drives to be daisy chained, with the last drive being terminated with a standard 220/330 ohm termination, and two 20-pin drive data connectors (J2 and J3) allowing direct connection of the controller to each drive.

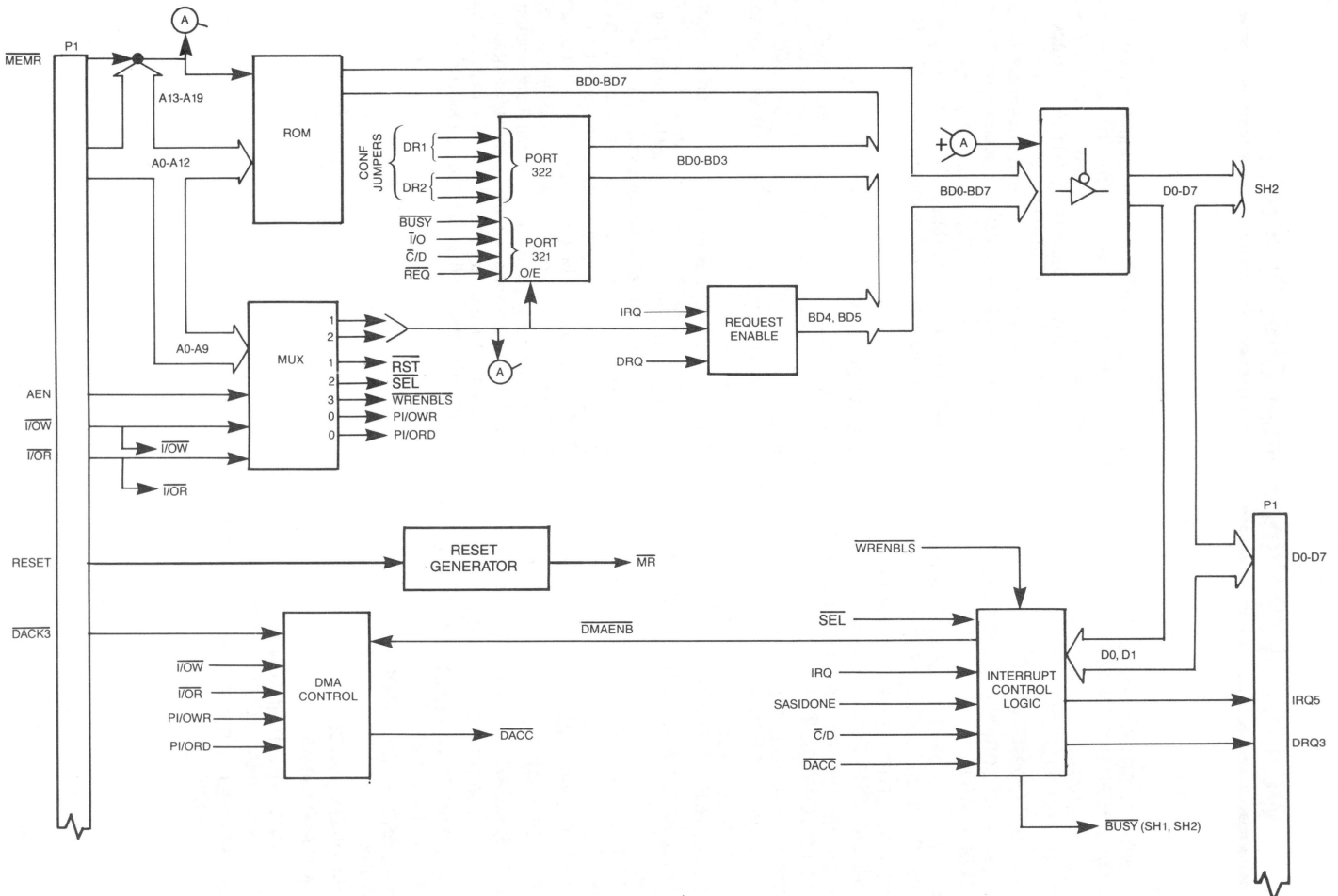


FIGURE 1. WD1002-WX2 FUNCTIONAL BLOCK DIAGRAM (SH1 OF 2)

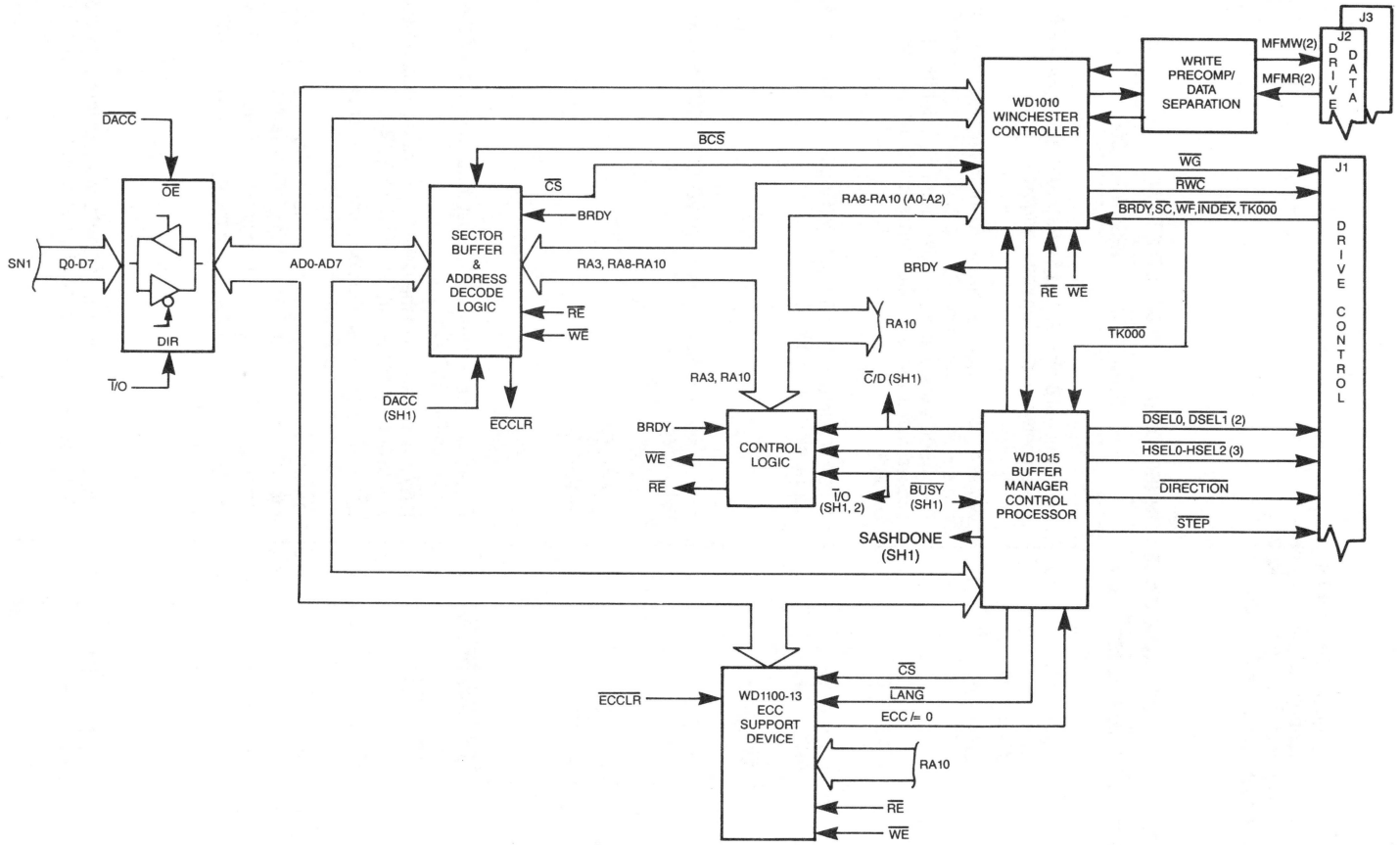


FIGURE 1. WD1002-WX2 FUNCTIONAL BLOCK DIAGRAM (SH2 OF 2)

DRIVE INTERFACES

CONNECTORS

Table 1 describes the pin designations for Host Interface Connector P1, Table 2 describes the pin designations for Drive Control Connector J1, and Table 3 describes the pin designations for Drive Data Connectors J2 and J3.

TABLE 1. HOST INTERFACE CONNECTOR (P1) PIN DESCRIPTION

PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTIONAL DESCRIPTION
A1, A10	NC			
A2 thru A9	D7 thru D0	DATA BIT 7 thru DATA BIT 0	I/O	Bi-directional 8-bit data bus for data and status communication between the Controller and Host.
A11	AEN	ADDRESS ENABLE	I	When AEN is asserted, the DMA Controller takes control of the Host Address bus, Control bus, and Data bus. I/O Port Addresses are no longer generated for I/O Port access. In this mode, the I/O Port is selected by asserting DACK3.
A12 thru A31	A19 thru A0	ADDRESS BITS A 19 thru A0	I	A 20-bit address bus for I/O Port and on-board ROM addressing by the Host.
B1, B10, B31	GND	GROUND		
B2	RST	RESET	I	When asserted, RST forces the WD1002-WX2 to its initial power-up state.
B2, B29	+5VDC	+5VDC		+5VDC
B7	−12VDC	−12VDC		−12VDC
B9	+12VDC	+12VDC		+12VDC
B4, B5, B6, B8, B11		NC		
B12	$\overline{\text{MEMR}}$	$\overline{\text{MEMORY READ}}$	I	$\overline{\text{MEMR}}$ is asserted when the Host reads a byte from the on-board BIOS ROM.
B13	$\overline{\text{IOW}}$	$\overline{\text{I/O WRITE}}$	I	$\overline{\text{IOW}}$ is asserted when the DMA Controller or Host writes a data or control byte to the WD1002-WX2.
B14	$\overline{\text{IOR}}$	$\overline{\text{I/O READ}}$	I	$\overline{\text{IOR}}$ is asserted when the DMA Controller or Host reads a data or status byte from the WD1002-WX2.
B15	$\overline{\text{DACK3}}$	$\overline{\text{DMA ACK}}$	I	$\overline{\text{DACK3}}$ is asserted in response to a DMA request from the WD1002-WX2 providing the I/O Port select function.
B16	DRQ3	DMA REQUEST	O	DRQ3 is asserted by the WD1002-WX2 whenever data is available for transfer to or from the WD1002-WX2 under DMA control.
B17 thru B22	NC			
B23	IRRQ5	INTERRUPT REQUEST	O	IRQ5 is asserted by the WD1002-WX2 to interrupt the Host upon the completion of a command.
B24 thru B28, B30	NC			

TABLE 2. DRIVE CONTROL CONNECTOR (J1) PIN DESCRIPTION

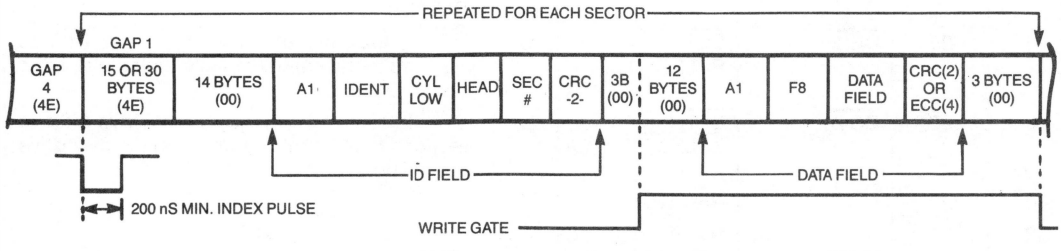
PIN	GND	MNEMONIC	SIGNAL NAME	I/O	FUNCTIONAL DESCRIPTION
2	1	RWC	REDUCED WRITE CURRENT	O	When asserted with WG, RWC reduces the Write Current to the drives for writing on inner disk surfaces.
2	3	HS 2	HEAD SELECT 2	O	HS 2 is the most significant bit of the binary coded Head Select address.
6	5	WG	WRITE GATE	O	When asserted, WG allows Write Data to be written to the disk.
8	7	SC	SEEK COMPLETE	I	SC is asserted when the heads have settled on the final track at the end of a Seek.
10	9	TK000	TRACK 000	I	TK000 is asserted when the heads are positioned on cylinder 0.
12	11	WF	WRITE FAULT	I	WF is asserted to prohibit writing to the disk when a condition exists that would cause improper writing on the disk.
14	13	HS 0	HEAD SELECT 0	O	HS 0 is the least significant bit of the binary coded Head Select address.
16	15		Reserved		
18	17	HS 1	HEAD SELECT 1	O	HS 0 is the middle bit of the binary coded Head Select address.
20	19	INDEX	INDEX	I	INDEX is asserted once per disk revolution, indicating the beginning of a track.
22	21	RDY	READY	I	When asserted with SC, RDY indicates when the selected drive is ready to perform a Read, Write, or Seek command.
24	23	STEP	STEP	O	When asserted, STEP causes the selected head to move in or out based on the state of DIRIN.
26	25	DS 1	DRIVE SELECT 1	O	DS 1 is asserted to indicate that Drive #1 is to respond to the control signals on the disk drive control bus.
28	27	DS 2	DRIVE SELECT 2	O	DS 2 is asserted to indicate that Drive #2 is to respond to the control signals on the disk drive control bus.
30	29		Reserved		
32	31		Reserved		
34	33	DIRIN	DIRECTION IN	O	DIRIN indicates which direction the heads move during a Seek Command (asserted = in, deasserted = out).

TABLE 3. DRIVE DATA CONNECTORS (J2 AND J3) PIN DESCRIPTIONS

PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTIONAL DESCRIPTION
1	DSEL	DRIVE SELECT		Not used.
2, 4, 6, 8, 11, 12, 15 16, 19, and 20	GND	GROUND		Ground.
3, 5, 7, 9, and 10				Spares
13	+ MFMWD	+ MFM WRITE DATA	O	+ MFMWD is MFM encoded Write Data to be written to the disk. This data is precompensated for inner disk cylinders. The beginning cylinder for Write Precompensation is programmable. The amount of precompensation for both EARLY and LATE bits is 12 nsec. This line is Tri-stated except when writing.
14	– MFMWD	– MFM WRITE DATA	O	– MFMWD is MFM encoded Write Data to be written to the disk. – MFMWD is an inverted copy of + MFMWD.
17	+ MFMRD	+ MFM READ DATA	I	+ MFMRD is MFM encoded Read Data from the disk.
18	– MFMRD	– MFM READ DATA	I	– MFMRD is MFM encoded Read Data from the disk. – MFMRD is an inverted copy of + MFMRD.

FORMAT

Figure 2 illustrates the format used in formatting the tracks on Winchester disks. The Format Command initializes the ID and data fields on a particular disk.



ID FIELD

A1 = A1 hex with 0A hex clock
IDENT = 2 L.S.B. = Cylinder High
FE = 0-255 Cylinders
FF = 256-511 Cylinders
FC = 512-767 Cylinders
FD = 768-1023 Cylinders
HEAD = Bits 0, 1, 2 = Head Number
Bits 3, 4 = 0
Bits 5, 6 = Sector Size
Bit 7 = Bad Block Mark
Sec # = Logical Sector Number

DATA FIELD

A1 = A1 hex with 0A hex Clock
F8 = Data Address Mark; Normal Clock
USER = Data Field 128 to 1024 Bytes

NOTES:

1. GAP1 and 3 length determined by sector number register contents during formatting.
2. If EXT bit in SDH register is set to 1 then an additional 7 data bytes are written, no CRC bytes are written.

FIGURE 2. WINCHESTER DISK FORMAT

SECTOR INTERLEAVING

The WD1002-WX2 accepts any interleave value between zero and the number of sectors per track minus one. The interleave value tells the Controller where the next logical sector is located in relation to the current sector. For example, an interleave value of one specifies that the next logical sector is physically the next sector on the track. An interleave of two specifies that the next logical sector is two sectors ahead of the current sector, so there is one sector between any two consecutive logical sectors. Thus, the number of physical sectors between any adjacent logical sectors is the interleave value minus one. Any out-of-range interleave results in an interleave of one.

CONTROLLER PROGRAMMING INFORMATION

I/O PORT DESCRIPTIONS

The WD1002-WX2 is configured as a contiguous block of four I/O addresses, beginning at address 320 Hex. Each of the I/O ports is bi-directional (i.e., both read and write operations can be performed at each of the four addresses). The functions of the four ports in both the read and write modes are listed in Table 4. These ports are used for all communication between the Host and Controller.

TABLE 4. I/O PORT DESCRIPTIONS

ADDRESS	READ PORT FUNCTION	WRITE PORT FUNCTION
320	Read Data, WD1002-WX2 to Host	Write Data, Host to WD1002-WX2
321	Read WD1002-WX2 HRDWR Status	WD1002-WX2 Reset
322	Read Drive Configuration Info	WD1002-WX2 Select
323	Not Used	Write DMA and Interrupt Mask Register

Port 320 is a bi-directional data path over which commands, parameters, and status are passed.

Read port 321 contains the Controller hardware status. This byte of status can be read at any time, including command execution. Bits in this port have the following definitions:

BIT							
7	6	5	4	3	2	1	0
d	d	IRQ	DRQ	BSY	C/$\overline{D}$	I/$\overline{O}$	REQ

IRQ Interrupt Request. Signifies that an interrupt is pending.

DRQ DMA request bit, Signals that the Controller is ready for a DMA transfer to take place. The direction of the transfer is defined by the I/O bit.

BUSY Busy bit. Signals that the Controller is busy executing a command and is unavailable to accept another command.

C/$\overline{D}$ Command/$\overline{Data}$. Tells the Host which type of transfer the Controller is expecting either a command or status byte, C (C/$\overline{D}$) being asserted, or data, $\overline{D}$ (C/$\overline{D}$) being asserted.

I/$\overline{O}$ Input/$\overline{Output}$. Defines the direction for transfers between Host and Controller. The terms input and output, in this case, are from the Host's point of view.

REQ Request bit. One of the handshake signal for transfers between Host and Controller. When transferring data to or from the Controller by the Host, this bit being asserted informs the Host that the Controller is ready for the transfer.

d Don't care bits. Unused.

Reading port 322 returns, in bit positions 0 through 3, a 4-bit code that tells the Host the configurations of the drive(s) attached. The two least significant bits correspond to drive 0 and the two most significant bits correspond to drive 1. The Controller provides jumpers that allow setting these drive configuration bits as desired. The factory setting for the jumpers is all ones.

Writing to port 321 generates a hardware reset on the Controller. When writing to port 321, the data byte is ignored.

Writing to port 322 when the Controller is not busy selects the Controller and prepares it to receive a command. The Controller responds to selection by setting the Busy bit in the status register. When writing to port 322, the data byte is ignored.

Port 323 contains two bits which enable or disable the interrupt and DMA request lines to the Host. Bits in this port have the following definitions:

BIT							
7	6	5	4	3	2	1	0
d	d	d	d	d	d	IRQEN	DRQEN

IRQEN Interrupt Request Enable. When set, this bit enables interrupts to the Host.

DRQEN DMA Request Enable. When set, this bit enables DMA requests to the Host.

d don't care bit.

COMMAND INFORMATION

The Controller firmware driver routines reside in a ROM which can be directly addressed by the Host, and are located starting at address CB000 (Hex) in the Host Memory Address space. The Controller provides a 28 pin DIP socket, wired to accommodate a 4K (2732) or 8K (2764) JEDEC ROM. Figure 3 illustrates the standard connections for the 2732 or 2764 EPROM, which can be modified to support a 2716 EPROM by cutting the etch between pads E4 and E2, and jumpering E4 to E3.

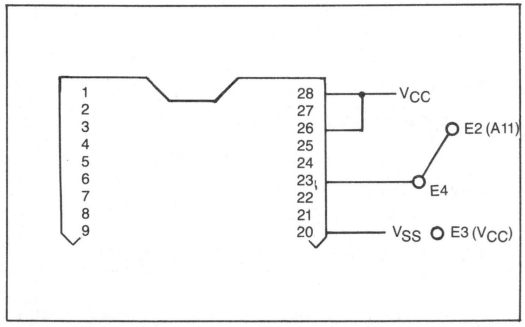


FIGURE 3. EPROM SOCKET CONFIGURATIONS

The Host issues commands to the Controller by first selecting the Controller with a Write Port 322. The Controller then sets the Busy and Request bits in the status register. When REQ is asserted, the Host outputs a 6-byte Command Block to the Controller which contains the command and necessary parameters the Host wants the Controller to execute. The bytes in the Command Block are defined in Figure 4.

Two retry disable bits are defined in the Command Block; one (R1) disabling the general disk retries and a second (R2) disabling the retry of data ECC errors. The Data Retry bit (R2), when set, disables the one automatic retry that is performed when a data ECC error is encountered. When any other type of error condition occurs, the Controller examines the general retry disable bit (R1) to determine the retry method to use. If the bit is set, the Controller does not retry the operation, but aborts the command and reports the error to the Host via the Error bit in the Status Register. If R1 is reset, the Controller retries the operation ten times before aborting the command and reporting the error to the Host. In the case of an ID Not Found error, after the first ten retries, the Controller seeks to Track 0 on the drive, then seeks back to the target track, and retries up to ten more times before aborting the command and reporting the error to the Host.

	BITS							
BYTE	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Command Class			OP Code				
1	0	0	D	Head Number				
2	Cyl Number MSB			Sector Number				
3	Cylinder Number LSB							
4	Block Count or Interleave							
5	R1	R2	0	0	0	SP	SP	SP

LEGEND:

D Drive Number
R1 Retry Disable Bit 1, General Disk Retries
R2 Retry Disable Bit 2, Data ECC Retries
SP Step Pulse Timing Code for Seeks

FIGURE 4. COMMAND BLOCK DESCRIPTION

The Step Pulse Code is used to select the rate at which step pulses are issued to the drives. Table 5 defines the rates corresponding to each step pulse code.

TABLE 5. STEPPING RATE CODES

BITS			
2	**1**	**0**	**STEPPING RATE**
0	0	0	3 Milliseconds per Step*
0	0	1	Not Used (3 Milliseconds per Step)
0	1	0	Not Used (3 Milliseconds per Step)
0	1	1	Not Used (3 Milliseconds per Step)
1	0	0	200 Microseconds per Step
1	0	1	70 Microseconds per Step
1	1	0	3 Milliseconds per Step
1	1	1	3 Milliseconds per Step

*This is the preferred 3 msec. step code.

Once the Command Block has been received, the Controller executes the command, requesting DMA service if required, by setting the DRQ line on the bus (Read Port 321). If programmed I/O is desired, REQ, I/O, and C/D qualify the transfer. When the command is complete, the Controller signals the Host by resetting the Busy bit and generating an interrupt, if interrupts are enabled. Once the command is completed, the Controller makes the Command Completion byte available at port 320. This byte verifies to the Host the number of the drive just completing activity and whether or not an error occurred. The format of this byte is shown below.

BIT							
7	6	5	4	3	2	1	0
0	0	D	0	0	0	E	0

D — Number of the drive for which completion status is valid.
E — Error bit. If set, the command completed with an error.

COMMAND DESCRIPTION

The following is a list of the commands supported by the WD1002-WX2:

TEST DRIVE READY
RECALIBRATE
READ STATUS OF LAST DISK OPERATION
FORMAT DRIVE STARTING AT DESIRED TRACK
VERIFY SECTORS
FORMAT TRACK
FORMAT BAD TRACK
READ SECTOR BUFFER
WRITE SECTOR BUFFER
SEEK
INITIALIZE DRIVE PARAMETERS
READ ECC BURST ERROR LENGTH
READ SECTORS
WRITE SECTORS
EXECUTE CONTROLLER SECTOR BUFFER DIAGNOSTIC
EXECUTE DRIVE DIAGNOSTIC
EXECUTE CONTROLLER DIAGNOSTIC
READ LONG
WRITE LONG

The format for the various fields in the Command Block for each of these commands is shown in Table 6. If the block count is set to zero in commands which require a block count, the number of blocks transferred is 256.

TABLE 6. WD1002-WX2 COMMAND SUMMARY

COMMAND	CLASS/ OP CODE	BITS							
		DRV	HD	CYL	SEC	BLK/INT	R1	R2	STEP
Test Drive Ready	00	V	d	d	d	d	d	d	d
Recalibrate	01	V	d	d	d	d	V	d	d
Read Status of Last Operation	03	V	d	d	d	d	d	d	d
Format Drive	04	V	V	V	DR	V(INT)	V	d	V
Verify Sectors	05	V	V	V	V	V(BLK)	V	V	V
Format Track	06	V	V	V	DR	V(INT)	V	d	V
Format Bad Track	07	V	V	V	DR	V(INT)	V	d	V
Read Sectors	08	V	V	V	V	V(BLK)	V	V	V
Write Sectors	0A	V	V	V	V	V(BLK)	V	d	V
Seek	0B	V	V	V	DR	d	V	d	V
Initialize Drive Parameters	0C	V	d	d	d	d	d	d	d
Read ECC Burst Error Length	0D	V	d	d	d	d	d	d	d
Read Sector BFFR	0E	d	d	d	d	d	d	d	d
Write Sector BFFR	0F	d	d	d	d	d	d	d	d
Execute Sector Buffer Diagnostic	E0	d	d	d	d	d	d	d	d
Execute Drive Diagnostic	E3	V	d	d	d	d	V	d	V
Execute Controller Diagnostic	E4	d	d	d	d	d	d	d	d
Read Long	E5	V	V	V	V	V(BLK)	V	d	V
Write Long	E6	V	V	V	V	V(BLK)	V	d	V

LEGEND:

V Must be a valid parameter
DR Don't care within valid parameter range
d Don't care (should be 0 for future compatibility)
INT Interleave
BLK Block Count

TEST DRIVE READY (00)

This command selects the drive specified and interrogates the hardware status bits returned by that drive. If all status bits are in the correct state and the drive is idle, the command does not return an error code. If the drive status is not OK, or the drive is active, the command returns an error code, usually Drive Not Ready, or Drive Still Seeking.

RECALIBRATE (01)

This command moves the Read/Write heads to the track 0 position. If the general retry disable bit (R1) is reset, the Controller recalibrates automatically in case of error. The difference between this command and a direct seek to track 0 is this command steps the drive one cylinder at a time looking for $\overline{TK000}$ from the drive being asserted. The step rate is determined by the seek complete time from the drive. A direct seek to Track 0 is faster because the Controller steps the drive at the programmed step rate.

READ STATUS OF LAST DISK OPERATION (03)

The status reported by this command corresponds to the drive specified in the command. Status is updated after each command, so status clarifying an error previously reported to the Host can be read before the next command is issued to the same drive. When this command is issued, the Controller returns 4 status bytes read from port 320, which are defined as follows:

	BITS							
BYTE	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	AV	0	Error Code					
1	0	0	D	Head Number				
2	Cyl Number MSB		Sector Number					
3	Cylinder Number LSB							

LEGEND:

AV Address valid bit. Signifies that the last command issued required a disk address.

All other bits are the same as those defined in the command block definitions.

When an error occurs on a multiple sector data transfer (read or write), this command returns the address of the failing sector. If the Read Status Command is issued after any of the format commands or the Verify Desired Sectors command, the address returned by the Controller points one sector beyond the last track formatted or checked if there was no error. If there was an error, then the address returned points to the track in error. Table 7 lists the error codes returned by this command.

FORMAT DRIVE STARTING AT DESIRED TRACK (04)

This command recalibrates the drive, then seeks to the desired track and writes out address marks, header fields, and data fields for all sectors. The logical sector layout is specified by the interleave value included with the command. The data pattern is defaulted to that data currently residing in the Sector Buffer. If a hard error occurs while formatting a track, the format operation can then be continued at the beginning of the next track. The format operation always starts at the first sector of the track.

VERIFY SECTORS (05)

This command reads from 1 to 256 sectors as specified, beginning at the desired sector. If an error occurs during a multiple sector read, the Seek operation terminates at the sector where the error occurs. The Host may then issue a Read Status of Last Disk Operation Command to determine what error has occurred. To continue the operation, the Host calculates the difference between the number of sectors desired and the number of sectors completed and issues another Seek Command to access the remaining sectors.

FORMAT TRACK (06)

This command recalibrates the drive, seeks to the target track, and writes the ID and data fields with the interleave value specified. This command can be used to clear the bad track flag, or to reformat individual tracks. The data pattern is defaulted to that data currently residing in the Sector Buffer.

FORMAT BAD TRACK (07)

This command is the same as the Format Track Command except the bad track flag is set in the ID field.

READ SECTORS (08)

This command reads from 1 to 256 sectors as specified, beginning at the desired sector. If an error occurs during a multiple sector read, the read terminates at the sector where the error occurs. The Host may then issue a Read Status of Last Disk Operation command to determine what error has occurred. To continue the operation, the Host calculates the difference between the number of sectors desired and the number of sectors completed and issues another Read Command to access the remaining sectors.

WRITE SECTORS (0A)

This command writes from 1 to 256 sectors as specified. The multiple sector transfer scheme works the same as the read command.

SEEK (0B)

This command initiates a seek to the track and selects the head number specified in the command. The drive must be formatted. For drives employing buffered step seeks, step pulses can be issued at high speed, freeing the Controller for other operations. After the Controller issues a Buffered Seek to the drive, it returns a completion status, not waiting for the drive to complete the seek. If the return status shows no error, then the seek was issued correctly. If there is an error, then the seek was not issued. After transferring the status, another

TABLE 7. CONTROLLER RETURNED ERROR CODES

HEX CODE	DEFINITION
00	No error detected.
03	Write Fault signal received from the drive. This error should be reported if the Controller detects Write Fault being asserted from the drive either at the completion of a Sector Data Transfer or initially after a successful drive select and the drive indicates ready.
04	Drive Not Ready. This error should be reported if the Controller fails to receive DSEL from the drive, or the drive indicates not ready after selection.
06	Track 0 Not Found. After stepping the drive 200 more steps than the number of cylinders in the drive, TK000 was not received from the drive. This error is reported during a recalibrate command.
08	Drive Still Seeking. This status should be returned in response to a Test Drive Ready Command if a buffered step seek was issued to a drive and the drive has not asserted SC.
11	Uncorrectable Data Error In The Data Field. The Controller detected a data error that could not be corrected.
12	Sector Address Mark Not Found. The Controller did not detect a Data Address Mark from the drive within its timing window.
15	Seek Error. After a seek, the target disk address did not match the ID address read from the disk. Either the ID field did not match or there was a bad CRC.
18	Correctable Data Error. The Controller detected a media error while reading that was corrected by ECC. This error code informs the Host software that error correction has taken place.
19	Track Is Flagged Bad. The last data transfer command encountered a track that was flagged defective using the Format Bad Track Command. No retries are attempted in response to this error.
20	Invalid Command. The Controller has received an invalid command from the Host.
21	Illegal Disk Address. The Controller has received a disk address that is beyond the maximum range for this drive.
30	Sector Buffer Error. The Controller detected a data error during Sector Buffer Diagnostics.
31	Controller ROM checksum Error. A ROM checksum error was detected during the Controller Diagnostic Command.
32	ECC Polynomial Error. During the Controller Diagnostic Command, the hardware ECC generator failed its test.

command can be issued to either drive. If a new command is received for a drive with an outstanding seek, then the Controller waits, with BUSY asserted, for the seek to complete before executing the new command, unless the command is a Test Drive Ready, in which case the Controller returns a drive still seeking error. There is no timeout condition in the Controller waiting for buffered step seeks to complete.

The Controller can be programmed for the step pulse rate to use for this drive. Buffered step drives are supported at 70, or 200 usecs. per step. After the Controller stops sending the drive step pulses, the drive seeks based on its own stepping algorithm. This scheme allows the Controller to finish the command without having to process the physical seek operation, thus making overlapped seeks possible. There is also a fixed step rate of 3 msec. per step.

INITIALIZE DRIVE PARAMETERS (0C)

This command enables the Host to configure the Controller to work with drives that have different capacities and characteristics. Drive 1 and Drive 0 can be initialized for different drive parameters. After the Host sends the command to the Controller, it then sends an 8-byte block of data that contains the drive parameters. The parameters are listed below:

Maximum Number of Cylinders (2 bytes, 1024 max.)
Maximum Number of Heads (8 max.)
Starting Reduced Write Current Cylinder (2 bytes, 1024 max.)
Starting Write Precompensation Cylinder (2 bytes, 1024 max.)
Maximum ECC Data Burst Length (1 byte, 11 max.)

If the Initialize Drrive Parameters command is not issued, the Controller defaults to the following: 306 cylinders, 4 heads, Reduced Write Current and Write Precompensation beginning at cylinder 153, and an 11-bit burst error length (Western Digital Corp. recommends using a maximum ECC burst length of five or less to ensure optimum integrity of data recovered.)

READ ECC BURST ERROR LENGTH (0D)

This command is only valid following a correctable data error. It transfers one byte to the Host indicating the length of the error corrected. The error length is determined by counting the number of bits between the first and the last bit in the error, including the first and last bits.

READ SECTOR BUFFER (0E)

This command transfers the 512 bytes of data currently residing in the Sector Buffer to the Host.

WRITE SECTOR BUFFER (0F)

This command writes 512 bytes of data from the Host into the Controller Sector Buffer.

EXECUTE SECTOR BUFFER DIAGNOSTIC (E0)

This command executes a 9-pass test that uses a 9-byte pattern (0, 1, 2, 4, 8, 10, 20, 40, and 80 hex) that is written to the Sector buffer, then read back. After each successful completion, the whole pattern is shifted one byte position and repeated.

EXECUTE DRIVE DIAGNOSTIC (E3)

This command tests both the drive and the drive-to-Controller interface. The Controller sends Recalibrate and Seek commands to the selected drive and reads sector 0 of each track to verify that both ID and data fields are correct. The Controller does not perform any Write operations during this command, making the assumption that the disk has been previously formatted.

EXECUTE CONTROLLER DIAGNOSTIC (E4)

This command performs a Controller ROM checksum, a Controller RAM diagnostic (similar to the one done on the Sector Buffer), a Sector Buffer diagnostic, an ECC chip diagnostic, and a WD1010 diagnostic.

READ LONG (E5)

This command returns both the data and ECC bytes contained in the data field of the desired sector. When the Host issues a Write Command to the Controller, the Controller writes to the disk the 512 bytes sent by the Host and appends the 4 bytes generated by the ECC device. During a normal Read Command, the Controller reads the 512 data bytes from the disk to the Sector Buffer and verifies the 4 ECC bytes. During a Read Long Command, the Host reads the 512 data bytes plus the 4 ECC bytes into the Sector Buffer.

WRITE LONG (E6)

When this command is used, the Host supplies the four bytes of ECC following the 512 bytes of data. This command can be used to test the Controller's ECC circuitry.

SPECIFICATIONS

PARAMETERS	CHARACTERISTIC
Host Interface:	IBM PC
Encoding Method:	MFM
Cylinders per Track:	Up to 1024
Sectors per Track:	17
Heads:	8
Drive Selects:	2
Step Rate:	70 μS, 200 μS, 3 mS
Data Transfer Rate:	5 Mbits/Sec (ST506)
Write Precomp Time:	12 nsec
CRC Polynomial:	$X^{16} + X^{12} + X^5 + 1$
ECC Polynomial:	$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^6 + X^2 + 1$
Recip ECC Polynomial:	$X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^6 + X^4 + 1$
Miscorrection Prob:	5 bit correction = <1.6 E-5
Non-detection Prob:	~2.3 E-10
Correction Span:	Up to 11-bit burst
Sectoring:	Soft
Drive Cable Length:	10 ft. (3 meters) max.
Power Requirements:	+5V ± 5%, 2.0 A max. ± 12V ± 10%, 175 mA max.
Ambient Operating Temp:	0°C to 50°C (32°F to 122°F)
Relative Humidity:	20% to 80% non-condensing
MTBF:	10,000 POH
MTTR:	30 minutes
Form Factor:	IBM PC
Dimensions:	
Length:	13.1 inches
Width:	3.85 inches
Height:	0.5 inches
Air Flow at 0.5" from Component Surfaces:	100 Linear Feet per minute

TIMING

Timing diagrams are shown in Figure 5 thru 8 and their values are listed in Tables 8 thru 11 respectively. Since the Controller I/O ports can be accessed by either the Host system DMA Controller or the Host processor, timings are given for both cases. The processor executes I/O and memory reads from the ports and the on-board BIOS ROM, and writes to the ports. The DMA is used for data transfers between the data I/O port and the Host RAM:

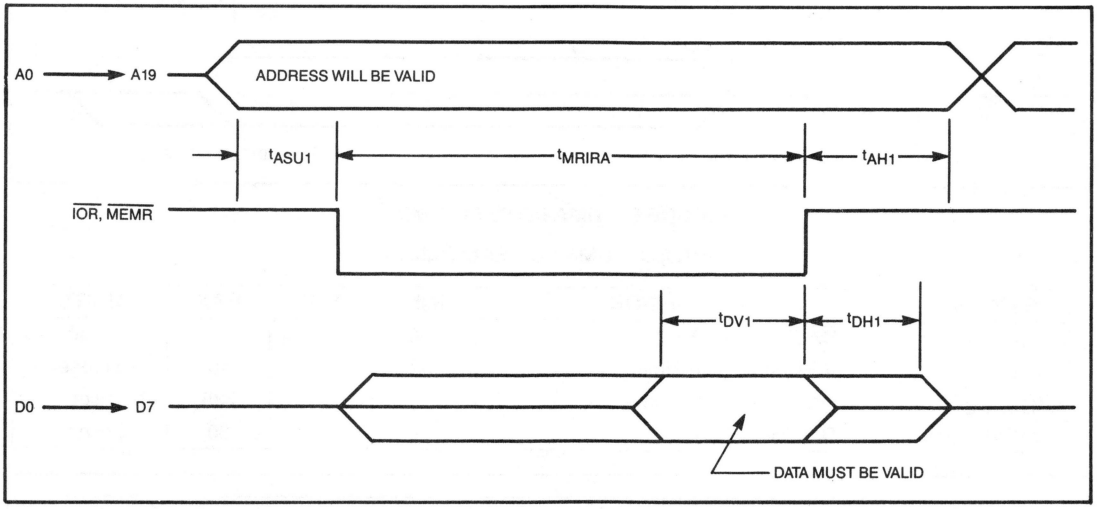


FIGURE 5. HOST I/O OR MEMORY READ TIMING

TABLE 8. HOST I/O OR MEMORY READ TIMING

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ASU1}	Address Setup Time	80			nsec
t_{MRIRA}	Read Active Time:				
	Memory Read	360			nsec
	I/O Read	570			nsec
t_{AH1}	Address Hold Time	140			nsec
t_{DV1}	Data Valid Time	120			nsec
t_{DH1}	Data Hold Time	0		60	nsec

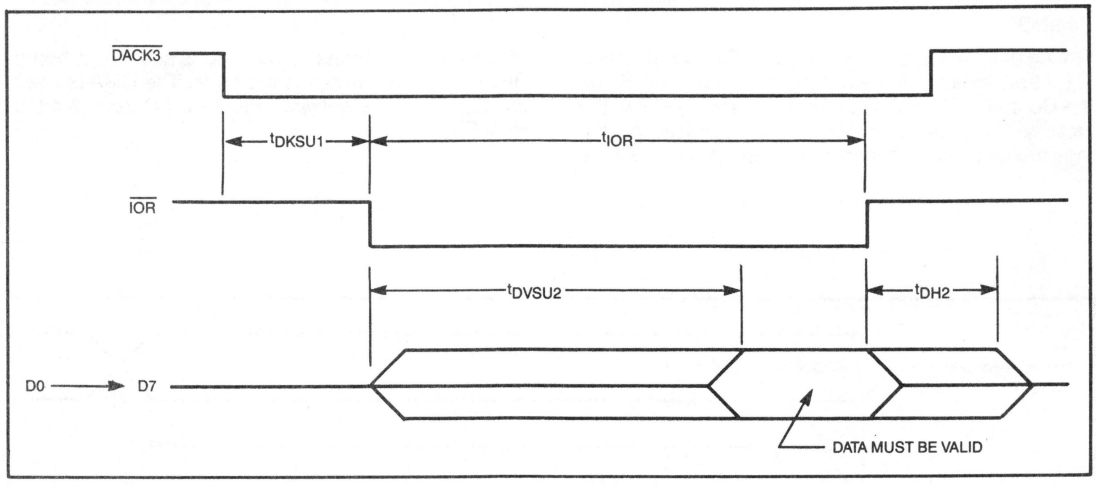


FIGURE 6. DMA I/O READ TIMING

TABLE 9. DMA I/O READ TIMING

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{DKSU1}	$\overline{DACK3}$ Setup Time	50			nsec
t_{IOR}	I/O Read Active Time	.52		10	microsec
t_{DVSU2}	Data Valid Setup Time			235	nsec
t_{DH2}	Data Hold Time	0		60	nsec

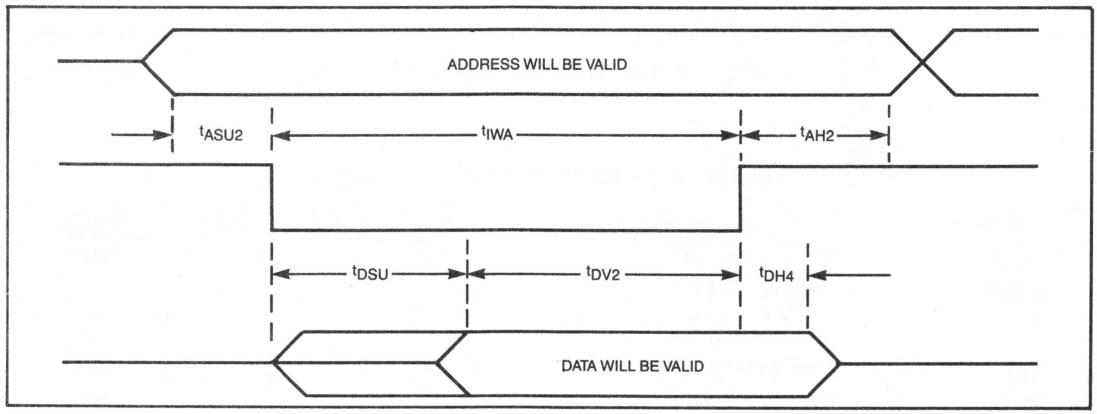


FIGURE 7. HOST I/O WRITE TIMING

TABLE 10. HOST I/O WRITE TIMING

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ASU2}	Address Setup Time	80			nsec
t_{IWA}	I/O Write Active Time	570			nsec
t_{AH2}	Address Hold Time	140			nsec
t_{DSU}	Data Setup Time	170			nsec
t_{DV2}	Data Valid Time	400			nsec
t_{DH4}	Data Hold Time	110			nsec

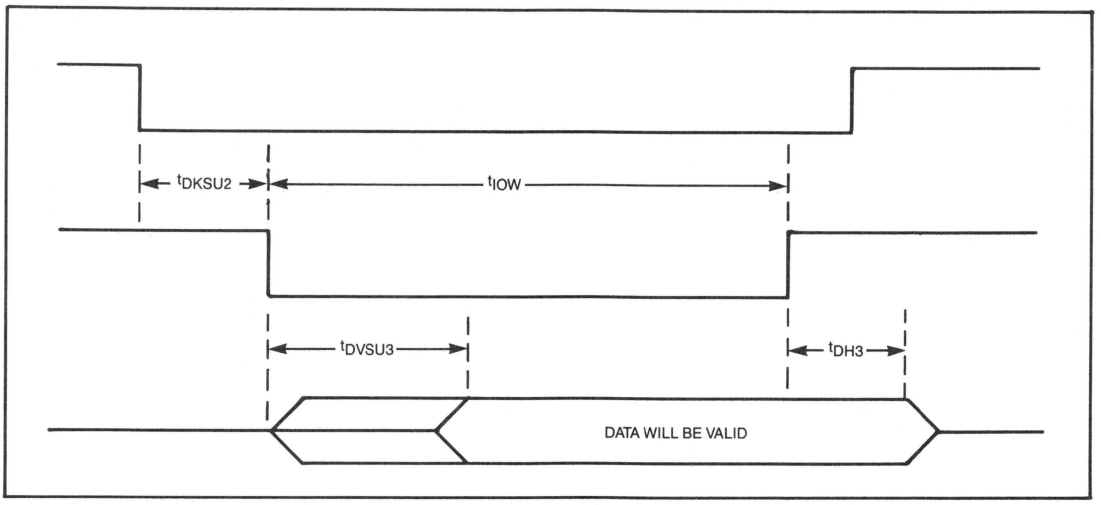


FIGURE 8. DMA I/O WRITE TIMING

TABLE 11. DMA I/O WRITE TIMING

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{DKSU2}	$\overline{DACK3}$ Setup Time	360			nsec
t_{IOW}	I/O Write Pulse Width	280			nsec
t_{DVSU3}	Data Valid Setup Time			75	nsec
t_{DH3}	Data Hold Time	30			nsec